The design of synchronisation and tracking loops for spread-spectrum communication systems.

Al-Rawas, Layth Abdul-Adheem

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THE DESIGN OF SYNCHRONISATION AND TRACKING LOOPS FOR SPREAD-SPECTRUM COMMUNICATION SYSTEMS

submitted by

LAYTH ABDUL-ADHEEM AL-RAWAS B.Sc., M.Phil.

for the degree of Ph.D.

of the University of Bath

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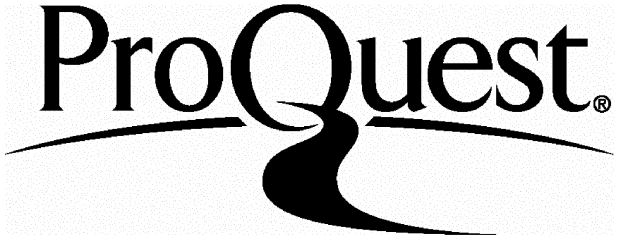

To My Parents, Wife and Children

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CONTENTS

SUMMARY

The work reported in this thesis deals with aspects of synchronisation and tracking in direct sequence spread spectrum systems used in ranging and communications applications. This is regarded as a major design problem in such systems and several novel solutions are presented. Three main problem areas have been defined: i) reduction of the acquisition time of code sychronisation in the spread spectrum receiver; ii) reduction of the receiver complexity; iii) improvement of the signal to noise ratio performance of the system by better utilisation of the power spectrum in the main lobe of the transmitted signal. Greater tolerance to Doppler shift effects is also important.

A general review of the spread spectrum concept and past work is first given in Chapter One, and common methods of synchronisation and tracking are reviewed in Chapter Two. There, current performance limitations are also included.

In Chapter Three a novel method is given for increasing the speed of synchronisation between locally generated and received codes, using a technique of controlling the loop's error curve during acquisition. This method is applied to different width (Δ) delay lock loops, and a significant increase in maximum search rate is obtained. The effect of the width of the discriminator characteristics and damping ratio on the maximum search rate are also examined. The technique is applied to data modulated spread spectrum systems which use either synchronous or asynchronous data communication systems. All methods have been tested experimentally and found to perform as predicted theoretically.

Several novel spread sprectrum configurations are given in Chapter Four which employ multi-level sequences. Some configurations have reduced the complexity and cost of the spread spectrum receivers. Others show some improvement in the maximum search rate as well as the signal to noise ratio performance. Some of these configurations have been implemented experimentally.

In Chapter Five, the generation and properties of the composite (Kronecker) sequences are explained. Several types of component sequences are examined. And the reception of these composite sequences are discussed. In particular, a technique is introduced for achieving a rapid acquisition of phase synchronisation using these codes.

The effect of white Gaussian noise on the acquisition performance of the delay lock loop is given in Chapter Six. Experimental results are obtained for both digital and analogue correlators.

Chapter Seven gives a final summary of the conclusions, and further work suggestions.

CHAPTER ONE

THE SPREAD SPECTRUM CONCEPT

1.1 INTRODUCTION

In the past few decades there has been a tremendous growth in the use of radio communications to provide a wide variety of services now required by modern civilisation. This growth has resulted in almost full utilisation of existing radio frequency channel allocations to cope with these services, particularly in high population density urban environments. This heavy usage has led to problems of interference and "spectrum pollution". Yet, there is still a demand for more widespread use of radio communications to handle the increasing traffic of information from computer networks, and particularly for communications from mobile users of the telephone system. Allocation of new frequency channels is now limited. In the United Kingdom the major new allocation of spectrum has been the re-allocation of band III of the old 405 line TV transmission to primarily mobile radio usage.

Two main techniques are being considered to increase the number of users sharing the frequency spectrum. One, is to use narrowband modulation techniques such as single side band modulation (SSB). However, this has not met with widespread adoption, although the technical problems associated with SSB, particularly for mobile applications are being overcome. The second is to use frequency re-use techniques in which the same frequency channel is re-used in two geographical locations which are spaced sufficiently far apart that there is very little mutual interference between users at each site. This approach forms the basis of cellular mobile radio schemes.

In general, there has also been a trend towards higher operating frequencies (→1GHz), where the number of current users is somewhat less. However, such schemes tend to be costly, requiring high technology components and circuitry, and for wide area coverage these frequency bands are not the most appropriate.

As a consequence, multiplexing techniques other than frequency division multiplexing have been proposed in an attempt to achieve improved spectrum utilisation or improved protection from interference [1-3]. "Spread Spectrum" techniques, using code division multiplexing, have been proposed as an alternative method of sending many messages simultaneously over a common channel, and these techniques also have many interesting interference rejection properties. Furthermore, these techniques are finding widespread use in military and aerospace applications where their special properties can be utilised to good effect.

In this chapter a description of code division multiplexed, or multi-access spread-spectrum systems will be given as well as some of its advantages, when compared with other types of multiplexing.

1.2 FEATURES OF MULTIPLE ACCESS SYSTEMS

Mutliplexing is the means by which more than one signal may be transmitted simultaneously between two points, using one channel, and it allows each signal to be separated at the receiving end. The following represent three main forms of multiplexing [4,5]:

a) **Frequency-division multiplexing (FDM)**

In this technique the bandwidth available is divided into independent channels, each of which has an assigned portion of the

frequency allocation. All channels can be transmitted simultaneously, and the number of independent users sharing the frequency allocation depends upon the bandwidth required by each message after modulation to the frequency of allowed channel. This type of multiplexing is employed in most radio communication systems and also in multiplexing telephone channels. An obvious reason for the popularity of this type of multiplexing is the availability of frequency selective filters which are highly efficient at rejecting the interference that would be caused by transmissions on adjacent channels. Co-channel interference can be minimised by ensuring that the co-channel transmitters are sited sufficiently far apart geographically. If the channel has a linear amplitude transfer characteristic the whole bandwidth can be employed. However, if the channel is non-linear a much larger bandwidth is needed due to the generation of intermodulation products which would act as adjacent channel interference if a guard band frequency allocation were not used. Usually most transmission channels, or the method of modulation, have some degree of non-linearity, and unused guard-band allocations must be used reducing the efficiency of the occupancy of the band.

b) Time division multiplexing (TDM)

The essence of time division multiplexing is that it takes a representative sample of several signals in strict sequence, and transmits the 'sample' of each signal sequentially along a common channel. Sampling of each signal must be conducted at a rate which is sufficiently high to preserve fidelity of each signal. This is determined by the Nyquist rate, such that the sampling frequency, f_s

is given by:

$$f_s \geq 2\ f_{max} \qquad 1.1$$

where f_{max} is the highest frequency component in the signal to be sampled. This is generally defined by low pass filtering the signal with a high order filter. The period between samples of each signal is just $1/f_s$ and the duration of each sample must be $< 1/Nf_s$, where N is the number of signals being transmitted down the channel.

The amplitude of the signal sample may be represented simply as an analogue sample amplitude, as in pulse amplitude modulation (P.A.M.) or by some other method which defines the amplitude as an equivalent quantity. Maximum advantage can be obtained if the resulting pulse or pulses are binary because this can improve signal recovery when the channel is noisy. One method is to convert the sample amplitude into the equivalent width of a binary pulse (Pulse Width Modulation (PWM)) or as a relative starting position of a fixed width pulse (PPM) or by a series of pulses representing the amplitude as a binary code (PCM).

The samples of each signal are transmitted in "time slots" delayed by fixed periods from a reference or synchronisation slot. The composite signal is demultiplexed at the receiver by ensuring careful synchronisation of the demultiplexer or data selector switch, and each signal is recovered from its respective sequence of samples by a sample and hold and filtering process. To achieve a larger number of simultaneous users each sample duration must be short and this demands that the channel must have a very wide bandwidth. Each signal utilises this wide bandwidth, unlike FDM systems where each signal has a relatively narrow bandwidth.

In a TDM system the principal source of interference is due to synchronisation errors, such as intersymbol interference, where due to synchronisation mis-timing, there is an overlap of adjacent time slots representing two different signals. If the samples are represented as binary sequences, coding can be used to offset the problems of intersymbol interference. Another main form of interference is due to aliasing. This is largely due to having signal filters which do not have a high roll off of f_{max}, such that there are significant signal components at frequencies $> f_s/2$.

c) **Code Division Multiple Access Multiplexing (CDMA)**

Like TDM, code division multiple access multiplexing is an inherently broadband technique, and each message is transmitted simultaneously over a common bandwidth allocation. Each message occupies the same bandwidth, however, unlike TDM systems each message is not split into time slots, and a strict synchronisation of the entire system via a central controller is not required. This obviously simplifies design of the multiple access system, although individual users generally require complex synchronisation systems. The technique has the advantage that it can also be used in applications where the signal to be transmitted must be protected from unauthorised detection and demodulation, corruption from high levels of interference, or deliberate acts of jamming interference.

The method used in the CDMA technique is to spread the signal to be transmitted by means of some high speed code or spreading function to a much wider bandwidth. Several methods of modulation exist and this defines the type of spread-spectrum system being used. Each user is modulated by a different code, and all the spread signals are

transmitted over a common bandwidth. Addressing of each signal is implicit in the code used, and recovery of each signal is by some form of correlation of the wanted signal with a replica sequence of that used in the appropriate transmitter. All the users on the channel act as a source of interference to each other user and this is removed, to some extent, by the cross-correlation performance of the codes used. In some cases matched filtering may be used to extract the wanted message. The filter is matched to the spreading sequence, and its ability to reject the interference of other messages is dictated by the convolution of the filter with the other sequences. This type of system will be considered in greater detail in a later section.

It is convenient to analyse the above three types of multiplexing systems in more detail by means of orthogonal functions. A system f(i, x), of real and almost everywhere non vanishing functions of f(0, x), f(1, x), f(2,x), ... is called orthogonal in the interval $x_o \leqslant x \leqslant x_1$, if the following conditions hold true [6].

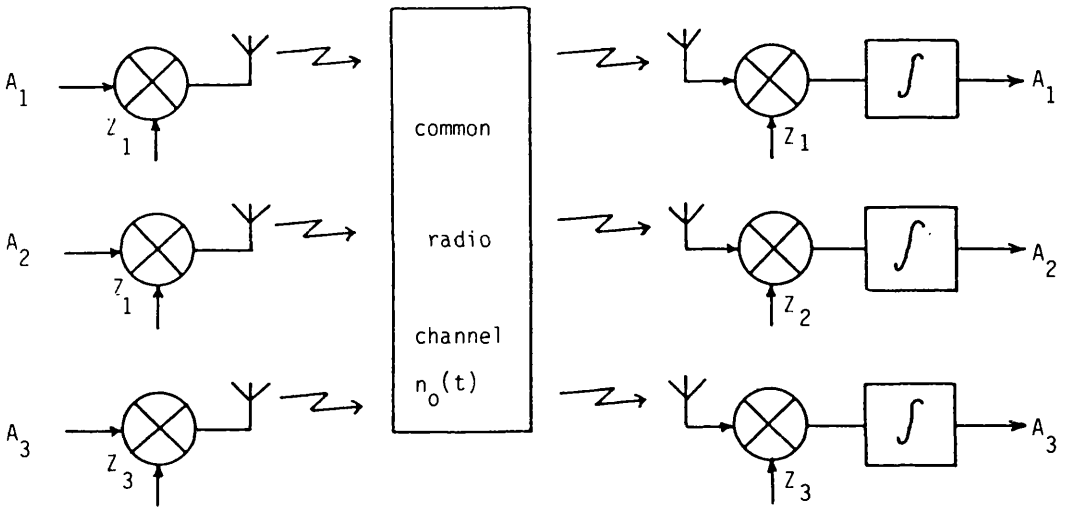
$$\int_{x_0}^{x_1} f(i,x)f(j,x)dx = x_i\delta_{ij} \qquad 1.2$$

$\delta_{ij} = 1$ for $i = j$

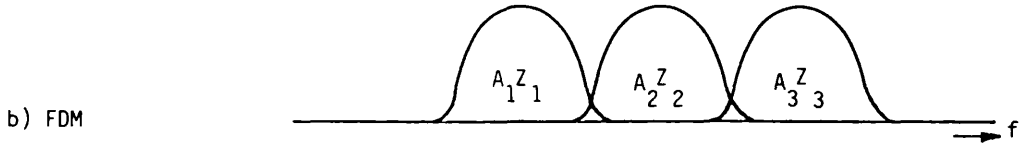
$\delta_{ij} = 0$ for $i \neq j$

the functions are called orthogonal and normalised if the constant x_i is equal to 1.

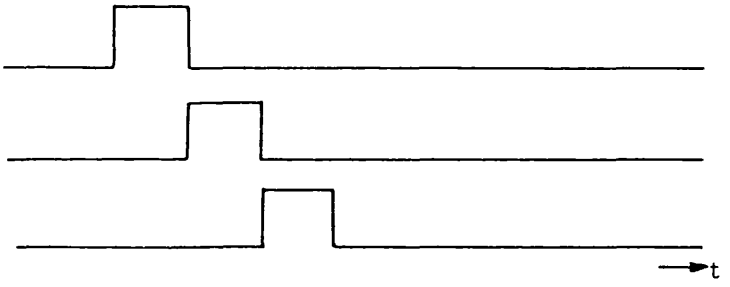
Consider a multiplexing system such as that shown in Figure 1.1 (a). Such a system could be used for FDM, TDM, or CDM systems. One channel is used to carry the three transmitted signals A_1Z_1, A_2Z_2 and



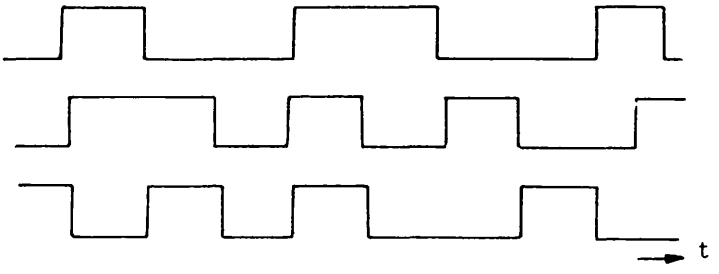
a) transmitter channel receiver



b) FDM



c) TDM



d) SP
or
CDM

Figure 1.1. General forms of multiplexing systems.

A_3Z_3 where A_1, A_2 and A_3 are the data to be transmitted and Z_1, Z_2 and Z_3 are the carrier signals. In the receiver any of the data $\hat{A}_j$ could be recovered as follows:

$$\hat{A}_j = \int Z_j(t) \cdot [n_o(t) + \sum_{j=1}^{n} A_j Z_j(t)]dt \qquad 1.3$$

To recover the data A_1 for example using any form of multiplexing shown in Figure 1.1 (b, c or d), the received signal is multiplied by Z_1.

$$\hat{A}_1 = \int Z_1(t)n_o(t)dt + \int A_1Z_1(t)Z_1(t)dt +$$
$$\int A_2Z_2(t)Z_1(t)dt + \int A_3Z_3(t)Z_1(t)dt \qquad 1.4$$

By considering the orthogonal function definition, equation 1.2, the terms

$$\begin{aligned}
\int Z_1(t)n_o(t)dt &= \delta_{10} = 0 \\
\int A_2Z_2(t)Z_1(t)dt &= A_2\,\delta_{21} = 0 \\
\int A_3Z_3(t)Z_1(t)dt &= A_3\,\delta_{31} = 0 \qquad 1.5 \\
\int A_1Z_1(t)Z_1(t)dt &= A_1\,\delta_{11} = A_1
\end{aligned}$$

$\therefore \hat{A}_1 = A1$

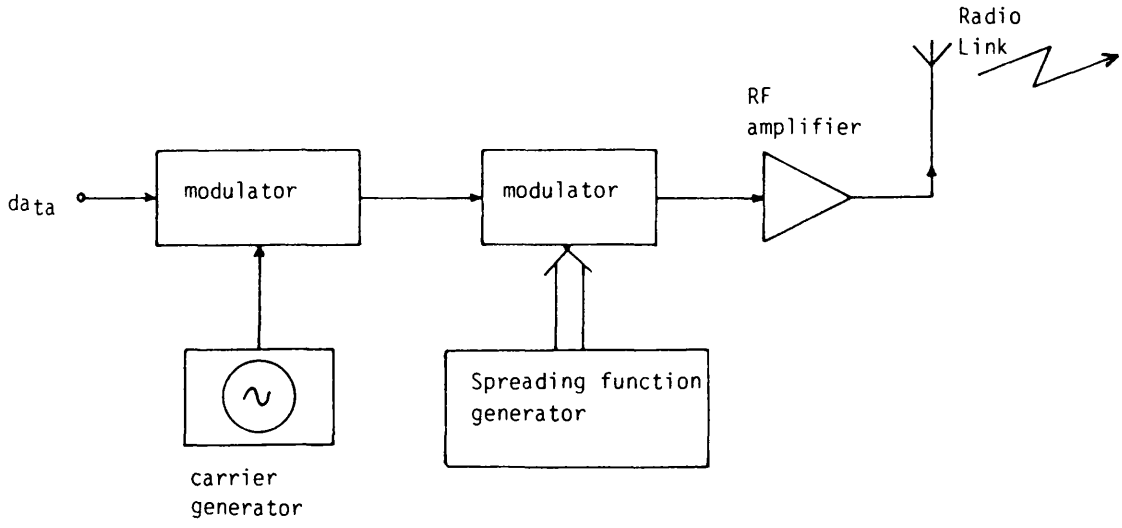
In the same way, $\hat{A}_2$ or $\hat{A}_3$ could be recovered by multiplying the received signal by Z_2 and Z_3 respectively. It will be shown later that a spread-sprectrum system uses the orthagonality, or quasi-orthogonality, properties of certain types of binary sequence to allow several users of a common channel to be extracted on the basis of equation 1.5.

1.3 SPREAD-SPECTRUM SYSTEMS

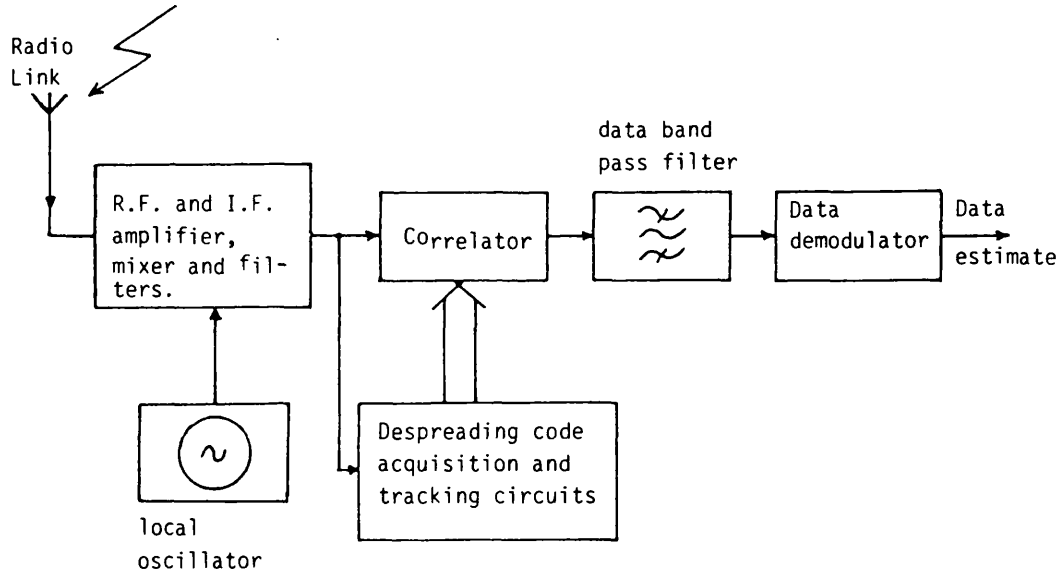
A spread-spectrum system is one in which a spreading function is used to expand the bandwidth of a data modulated carrier so that the transmission bandwidth is much wider than the information rate (by typically x 10^3). A general block diagram of a spread-spectrum transmitter and receiver is shown in Figure 1.2. This may be compared with "narrowband" techniques, such as, single sideband modulation (SSB) where the bandwidth of the transmitted signal is close to the bandwidth of the information to be sent (allowing for a small guard band), or even double sideband amplitude modulation, where the transmission bandwidth is just twice the information bandwidth.

In one form of spread-spectrum system, for example, data clocked at a rate of only a few k bits^{-1} may be expanded to a code stream clocked at 50 - 100 M bits^{-1}, with a corresponding increase in the bandwidth. This bandwidth expansion is well beyond that required to define the digits in a TDM system using PCM, for example. It is this bandwidth expansion which gives the spread-spectrum system so-called process gain for signal processing [7,8].

Over the last decade spread-spectrum techniques have been applied widely in communication, navigation and test systems. They have made possible adequate or improved communications under conditions which would not have been possible using conventional modulation schemes because of extreme noise or jamming interference. In terms of an RF communication system or navigation system, the cost and complexity of this high technology orientated system has tended to limit its use to military and aerospace applications, where cost and complexity are tolerated more than in the highly competitive markets of low cost, consumer orientated mobile radio. The



a) Transmitter



b) Receiver

Figure 1.2. General block diagram for a spread spectrum.
a) Transmitter, b) Receiver.

advantages shown by spread-spectrum methods for military and aerospace applications have previously caused designers to struggle without the advantage of high technology devices and/or high component density integrated circuits. However, as specialist integrated circuits become available, these problems of cost and complexity will be eased significantly and the arguments against spread-spectrum on the basis of complexity will not necessarily hold. Many other radio systems, such as mobile radio might now profit by looking at spread-spectrum techniques [9,12] and the special properties which they offer. It is also true that the techniques embodied in various types of spread-spectrum systems will find continued widespread use in instrumentation, secure data transmission systems and radar systems as well as normal communications systems. It is likely that as new types of network are developed for communications spread-spectrum techniques may show advantages not previously considered possible (e.g. local area networks operating without a central controller or cellular coverage schemes for mobile radio telephone systems) and continued development of the spread spectrum technology should help to stimulate its more widespread adoption.

In defining a spread-spectrum system it is general to apply the following two criteria:

a) The transmitted bandwidth is much greater than the signal bandwidth or the rate of information transfer.

b) Some function, other than that used to modulate the signal onto the r.f. carrier must be used to determine the resulting bandwidth of the transmitted signal.

Thus, wideband F.M., which may be considered to be a wide band technique, cannot be considered as a spread-spectrum technique because bandwidth spreading is achieved only by the modulator, not by a spreading function. Similarly, TDM systems are inherently broadband, but do not fall into the category of spread spectrum.

The bandwidth expansion process can be considered as a mapping process in which the spectral components are mapped into a new spectrum allocation prior to transmission. To receive the original signal it is necessary to remap, or de-spread, the received spread-spectrum signal back to its original form by using some inverse spreading function in the receiver. If the spread-despread operation is linear, as it often is, then there is of course no intrinsic improvement in the signal to noise ratio when the original unmodulated signal of bandwidth, B_s, is compared with the received de-spread signal over the same bandwidth, B_s. In fact the spread-despread operation will tend to worsen the signal to noise ratio because of noise in the amplifiers and mixers. The apparent improvement in signal to noise ratio arises when one considers the signal to noise ratio at the input to the receiver where the signal power spectrum density is low and the bandwidth wide with the output of the receiver where the bandwidth of the signal has been compressed back to the original signal bandwidths, B_s.

Nevertheless, this type of approach can enable the spread-spectrum system to be more tolerant of certain types of noise or interference which may be present over the channel.

The de-spread operation requires that certain information about the spreading function must be known at the receiver, **a priori**, in

order to detect and demodulate the signal [13]. This information includes:

1. The existence of the signal buried in noise.
2. The carrier frequency of the signal being transmitted.
3. The type of modulation (i.e. PSK, FSK).
4. The key to the spreading function and the rate of the spreading function code.
5. The method by which the data is modulated by the spreading function (i.e. SIK, frequency hopped etc.).
6. The relative phase of the spreading function.

Although some of these requirements are common to all communications systems, points 4 to 6 are requirements special to spread-sprectrum systems.

The action of spreading the transmission bandwidth of a signal enables the spread-spectrum system to have several special properties. Depending upon how the spreading function is used to modulate the data (i.e. point 5. above) dictates what sort of spread-spectrum system is produced. The following list of special properties is a collective list, and not all types of spread-spectrum system will have all these properties.

1. Interference rejection and anti-jamming capability.
2. Low density power spectrum for signal hiding in noise.
3. Message screening from eavesdroppers.
4. High resolution ranging.
5. Code division multiplexing for multiple access.
6. Selective addressing capability.

7. Resistance to co-channel interference.
8. Some resistance to frequency selective fading and multipath fading.

These properties arise as a result of the coded signal format in the spreading process. Often, attempting to achieve one of the above properties occurs at the expense of one or more of the others, even though they may involve similar sorts of signal processing operation. For example, a system designed to extract a signal which is buried or hidden in large densities of white noise may not work very efficiently when the signal is being jammed with CW interference - and vice versa.

The ability of a spread-sprectrum system to extract a signal from noise is an excellent illustration of Shannon's First Law expressed in the form of channel capacity [14].

$$C = W \log_2 (1 + S/N) \qquad 1.6$$

where C = information capacity as an equivalent number of digits/seconds

W = bandwidth (Hz)

N = white noise power in the channel (watts)

S = average signal power (watts).

The equation gives the relationship between the ability of a channel to transfer error-free information, compared with the signal to noise ratio, S/N, in the channel and the bandwidth needed to transmit the information

$$\text{or } \frac{C}{W} = 1.44 \log_e (1 + S/N) \qquad 1.7$$

When working under noisy conditions, such that S/N <<1 then $\log_e$ (1 + S/N) $\approx$ S/N

and [9]

$$C/W \approx 1.44\ S/N \qquad 1.8$$

It can be seen, therefore, that for any signal to noise ratio in the channel for S/N << 1 one can transmit error free information by increasing the transmission bandwidth, **pro rata.** Thus two channels having the same value of C have the same capacity for transmitting information even though the quantities W, S and N may be different. Thus, very crudely expressed, Shannon's Law states that one can accommodate noise in the channel by trading it off with the ratio between the required information rate and the transmission bandwidth. This law is fundamental to all the spread-spectrum schemes and introduces, quite generally the concept of the "process gain".

Generally, a spread-spectrum system develops its process gain by increasing the transmission bandwidth. The spread-spectrum technique will only 'remove' noise introduced in the channel, as specified in equation 1.8, and as explained earlier occurs because of the difference in bandwidth over which the white noise is measured.

1.3.1 Types of Spread-Spectrum Systems

There are several basic methods of spreading the baseband signal bandwidth [15-18].

a) Direct Sequence Systems

In this technique the data to be transmitted is first modulated onto a digital code sequence whose bit rate is much higher than the data rate. This expands the bandwidth of the signal. The code

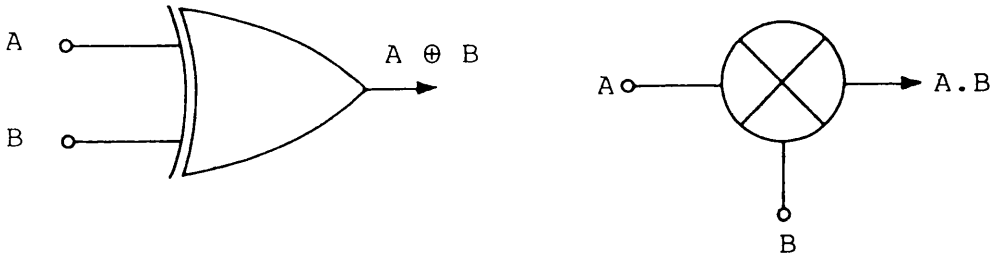
modulated data can then be used to modulate the r.f. carrier signal using any of the conventional techniques such as am, fm or phase modulation. Often, biphase phase shift keying is used to produce double sideband suppressed carrier transmission. The data may be analogue or digital, and modulation by the high speed sequence is generally via a multiplier (d.s.b.s.c. modulation) or in the case of digital data modulo-2 addition in an EX-OR gate, as shown in Figure 1.3.

b) Frequency Hopping

The data is modulated onto a carrier frequency whose frequency varies with time in discrete jumps. The frequency is controlled by the value of the n'tuple word produced by a sequence generator. The order of frequency jumps is set by the code sequences. The transmission bandwidth is also dictated by the sequence and the frequency synthesiser, although the actual amount of the bandwidth used at each frequency is always the data bandwidth, which is a small fraction of the bounds of the band.

c) Time Hopping

In this system the spreading sequence may be used to control the duration of the transmission. The transmitter output is keyed on and off at a time determined by the sequence. Generally, the transmitter is switched on for a much shorter period than it is off. This, together with the randomness with which the transmitter is keyed on, is a useful technique for reducing the detectability of a transmission (i.e. message hiding) so that direction finding equipment is less effective in locating the transmitter.



A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

A	B	C
1	1	1
1	-1	-1
-1	1	-1
-1	-1	1

Figure 1.3. Comparison of EX-OR gate and multiplier's operation

Synchronisation of the receiver, so that it is only switched on when the signal is transmitted, is particularly important, and this is the method by which noise reduction is achieved.

d) Chirp or Pulsed fm

This is a pulse compression technique in which the frequency of the carrier is swept over quite a wide range during the duration of the pulse. Chirp systems are useful for recovering pulse information from noise, however, they are not code addressable in their simplest forms and are not usually found in multiple-access spread-spectrum systems.

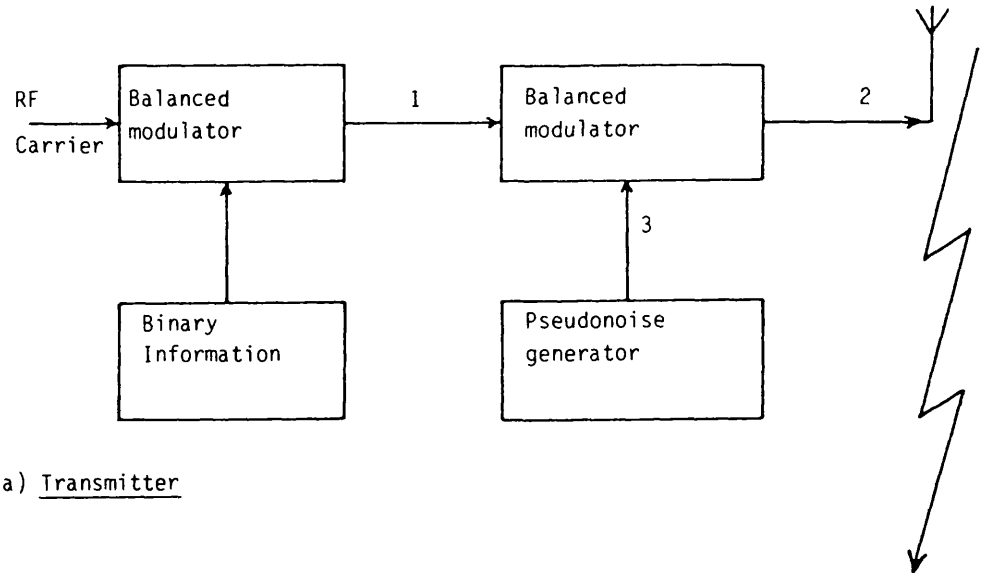
Combinations of two or more of these basic spread-spectrum modulation techniques may also be used to form hybrid systems [19-21]. For example, the combination of frequency hopped and time hopped systems forms the basis of a time hopped multiple access system.

In the following sections of this chapter the reception and demodulation of data spread using direct-sequence and frequency hopped techniques will be considered further.

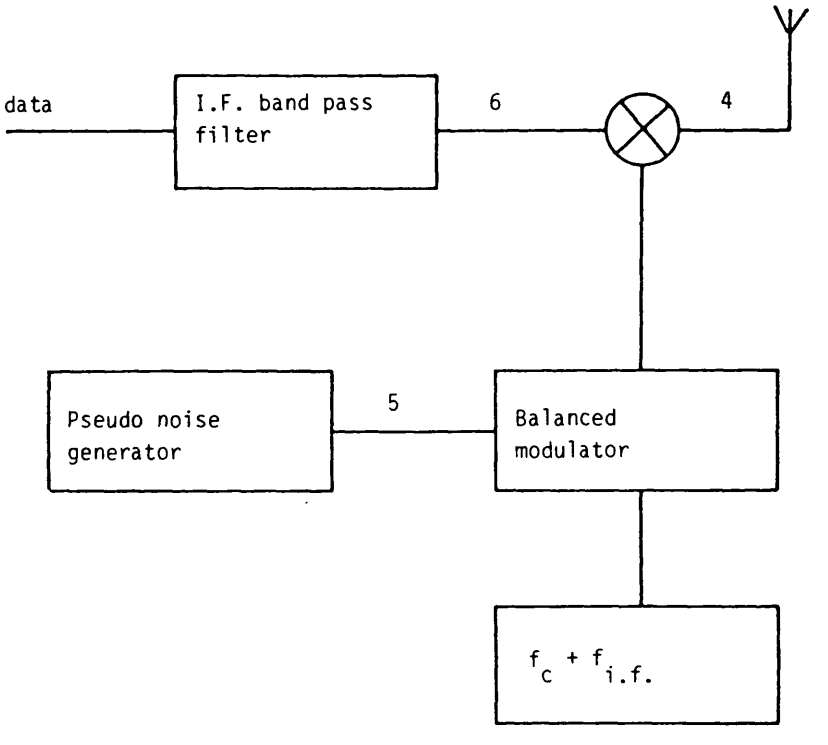
1.4 PRINCIPLES OF OPERATION OF SPREAD-SPECTRUM SYSTEMS

1.4.1 Direct Sequence Systems

In this section the operating principles of spread-spectrum systems are considered in greater depth, in particular the ability of the spread-spectrum receiver to reject interference. Figure 1.4 shows a simplified block diagram of a direct sequence spread-spectrum system. The source of information is assumed to be digital. The purpose of this phase-shift-keying (psk) modulator is to modulate the



a) Transmitter



b) Receiver

Figure 1.4(a). Block diagram of direct sequence system and its waveforms.

c) Ideal Waveforms.

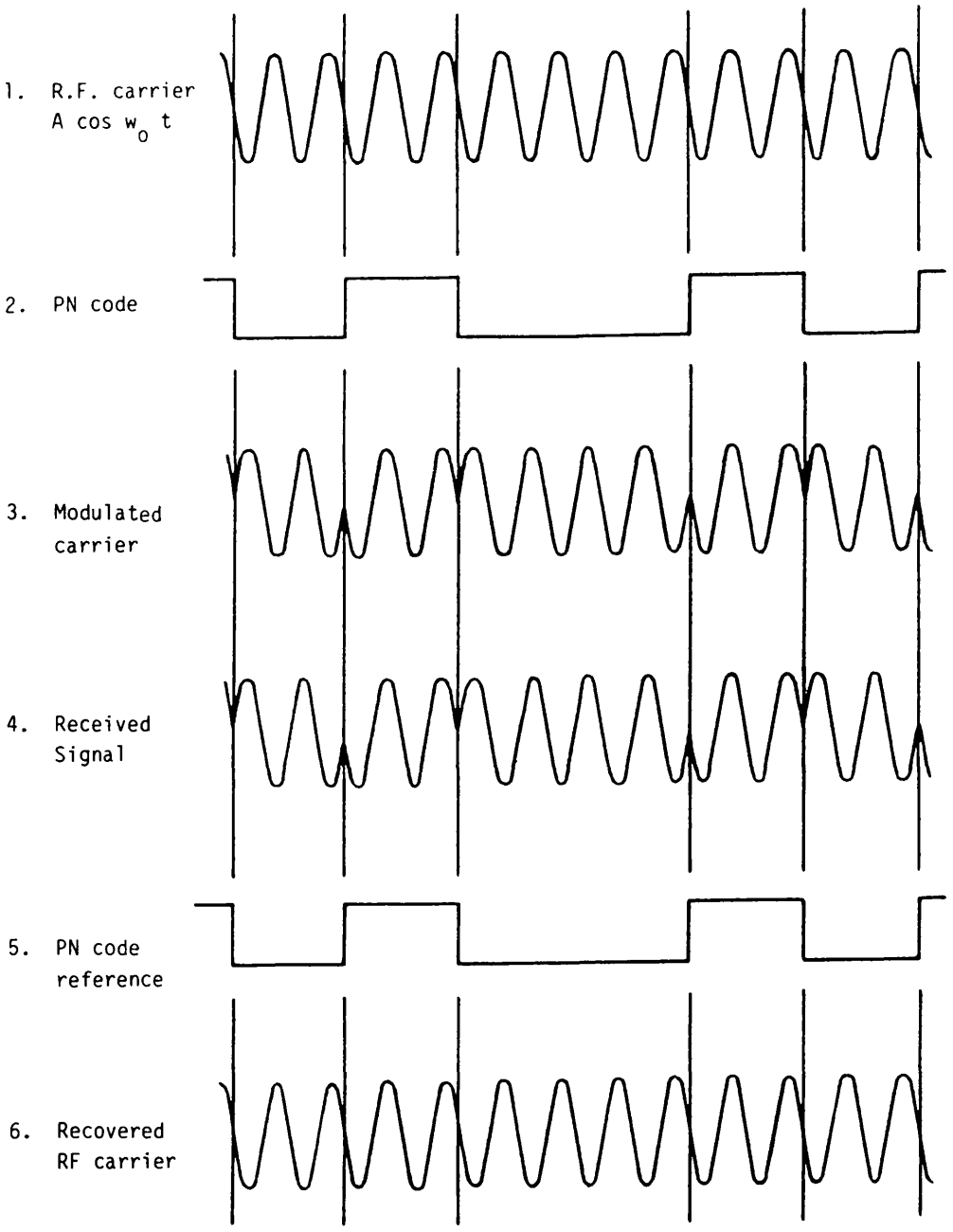


Figure 1.4(b) (Continued).

data onto the r.f. carrier. If the data changes from a 0 to a 1 the effect is to change the phase of the carrier by 180° for the duration of the data bit. Although not the only method of modulating data onto the carrier, it is a common and convenient method which provides double sideband suppressed carrier modulation.

The phase modulated carrier is then passed to a second psk modulator, where it is modulated by a high speed pseudo-noise code whose bit rate is much higher than the information rate. The purpose of this modulator is to spread the modulated carrier signal energy over a very much wider bandwidth. Most of the signal power is confined to a bandwidth roughly equal to twice the bit rate of the pseudo-noise code, and at the same time the peak power-spectral density is considerably reduced by spreading. The pseudo-noise code used for the spreading function is generally a binary sequence, the choice being made on the basis of the auto and cross-correlation performance of the codes.

An alternative form of direct sequence spread-spectrum system is illustrated in Figure 1.5. Here signal spreading takes place at base band. In the case of digital signals the modulator may be replaced by an Exclusive OR gate.

1.4.1.1 Frequency Spectrum of a Direct Sequence System

It is instructive, at this stage to consider the spectrum of the transmitted signal. The power spectrum, assuming bi-phase shift keying of the sequence onto the r.f. carrier, can be found by considering the baseband spectrum of the spreading function. The power spectrum of the spreading function can be found by utilising the Wiener-Khintchine relationships:

$$\Psi(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S(\omega)\ e^{j\omega\tau}\ d\omega$$

$$S(\omega) = \int_{-\infty}^{\infty} \Psi(\tau)\ e^{-j\omega\tau}\ d\tau \qquad 1.9$$

From these Fourier transforms it is seen that the power spectrum, $S(\omega)$ is simply the Fourier transform of the autocorrelation function $\Psi(\tau)$. The power spectrum is very strongly dependent upon $\Psi(\tau)$, and this is determined by the structure of the spreading function. An idealised spreading function, which can be closely approximated in practice, is a random binary sequence.

The autocorrelation function is defined as:

$$\Psi(\tau)_{auto} = \int_{-\infty}^{\infty} f(t)f(t-\tau)dt \qquad 1.10$$

For the case of random sequence the autocorrelation has the form shown in Figure 1.6. It has a triangular function over the range of delay $-\Delta < \tau < \Delta$

where Δ is the chip width = $1/f_c$

and 0 elsewhere.

As a consequence the power spectrum can be easily calculated from the fourier transform.

$$\Psi(\tau) = 1 + \tau/\Delta \text{ for } -\Delta \leq \tau \leq 0$$

$$\Psi(\tau) = 1 - \tau/\Delta \text{ for } 0 \leq \tau \leq \Delta$$

and the power spectrum is:

$$S(\omega) = \int_{-\Delta}^{0} [1 + \tau/t_c]e^{-j\omega\tau}\ d\tau + \int_{0}^{\Delta} [1 - \tau/t_c]e^{-j\omega\tau}\ d\tau \qquad 1.11$$

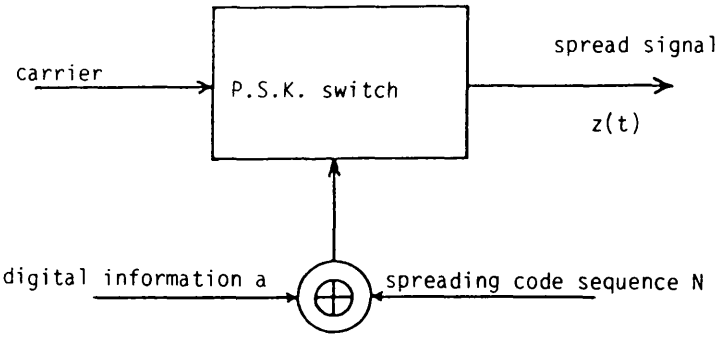


Figure 1.5. Simplified spread spectrum transmitter.

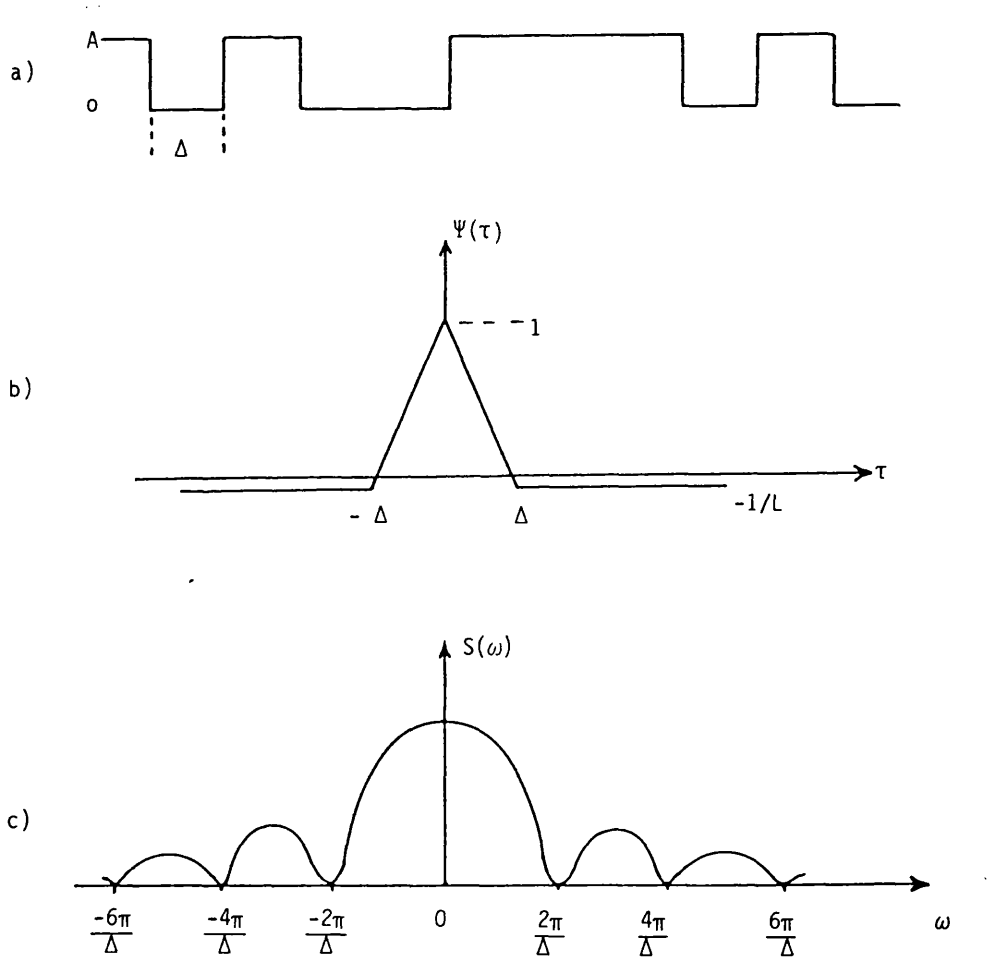


Figure 1.6. Auto-correlation function and power spectral density of binary code. a) maximal length sequence, b) auto-correlation function, c) power spectral density.

The double side spectrum is thus:-

$$S(\omega) = \frac{\Delta}{2}\left[\frac{\text{Sin}\ \frac{\omega\Delta}{2}}{\frac{\omega\Delta}{2}}\right]^2 \qquad 1.12$$

For the case of bpsk rf carrier modulation the spectrum is also double sided and shifted by the carrier frequency $\pm\ \omega_o$.

Figure 1.6 sketches the ideal spectrum of the transmitted signal. The double sided spectrum of the main lobe extends over $\pm\ 1/\Delta = \pm\ f_c$ Hz and has nulls at $\pm\ n\ f_c$, where n = 1, 2, 3, 4, ...

A random signal is not truly representative of the type of signal used in a spread spectrum system and some of the important detail is lost.

An important type of spreading function, which is discussed in Section 1.3 is a pseudo-random maximal length sequence, and this will be considered as a typical spreading function. This is a periodic sequence of length L code epochs before the sequence repeats. The autocorrelation function of this type of sequence has been found to be of the type shown in Figure 1.6. This may be expressed as:

$$\Psi(\tau) = L - \frac{\tau(L+1)}{\Delta} \quad \text{for } 0 \leq |\tau| \leq \Delta \qquad 1.13$$

$$\psi(\tau) = -1 \qquad \text{for } \Delta \leq |\tau| \qquad 1.14$$

Since the autocorrelation function is periodic with period $T=L\Delta$ the Fourier transform must be replaced by the Fourier series form of the Wiener-Khintchine relationship, i.e.:

$$S(\omega) = \frac{a_o}{T} + \frac{2}{T}\sum_{n=1}^{\infty} a_n \text{ Cos}(n\ \omega_o\ \tau) + b_n \text{ Sin } (n\omega_o\ \tau) \qquad 1.15$$

where

$$a_o = \int_{-\Delta}^{T-\Delta} \Psi(\tau)\ d\tau \qquad 1.16$$

$$a_n = \int_{-\Delta}^{T-\Delta} \Psi(\tau) \text{ Cos } (n\ \omega_o\ \tau) d\tau \qquad 1.17$$

$$b_n = \int_{-\Delta}^{T-\Delta} \Psi(\tau) \text{ Sin } (n\ \omega_o \tau) d\tau \qquad 1.18$$

and $\omega_o = \frac{1}{T} = \frac{1}{L\Delta}$

The power spectrum is now found to be a line spectrum wih a spacing between spectral lines of $1/2\pi T$ Hz and envelope

$$S(\omega) = \frac{1}{L} + \frac{2(L+1)}{L} \sum_{n=1}^{\infty} \frac{\text{Sin}^2\ (n\pi/L)}{(n\pi/L)^2}$$

This has the envelope of the random signal given earlier but there is also a dc term of value 1/L due to the finite correlation for:

$|\tau| > \Delta$

The resulting spectrum is shown in Figure 1.7 for a sequence of length L = 15 bits.

The spectrum of the ideal spread-spectrum system thus extends to $\pm\infty$. Clearly this is undesirable. However, it is interesting to note

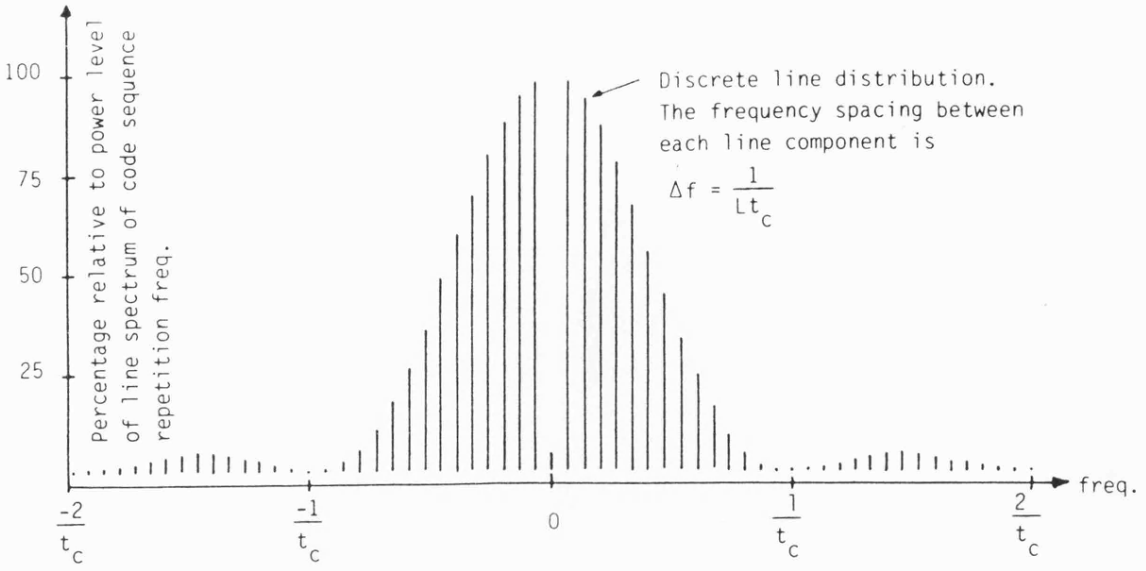


Figure 1.7. Two sided power spectral distribution for a 15 bit length sequence code. The code clock frequency is $f_c = \frac{1}{t_c}$

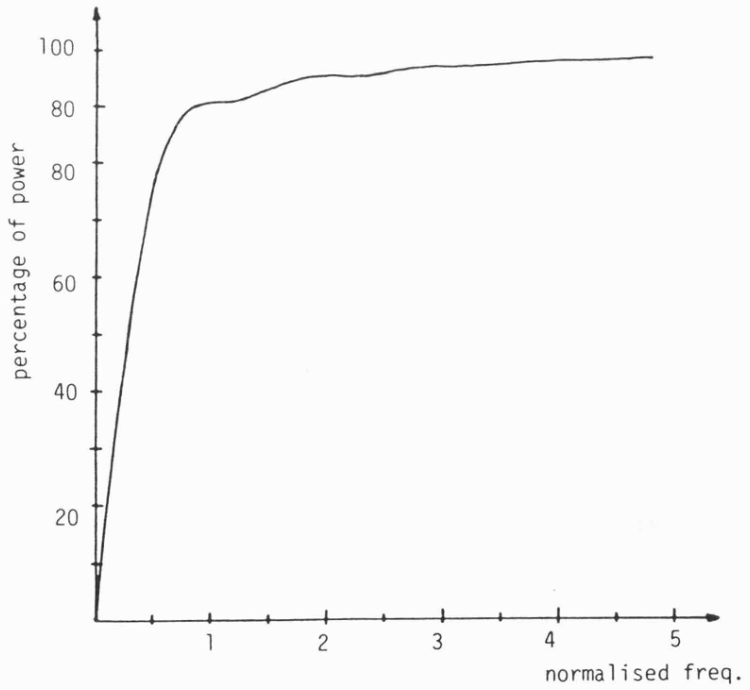


Figure 1.8. Power distribution in $\left[\frac{\sin X}{X}\right]^2$ spectrum.

that most of the power is contained in the main lobe. It is usual to filter the spread spectrum signal prior to transmission to minimise spectral pollution. Figure 1.8 shows the percentage power contained in the transmitted signal as a function of the transmission bandwidth. It is clear from this graph, that for a maximal sequence over 90% of the total power is contained in the main lobe. Filtering to the main lobe causes some distortion of the signal, but in terms of power loss the distortion caused is more than worthwhile.

The spectrum of other spreading functions will be given in Section 1.4.1.1.

1.4.2 Direct Sequence Receiver

At the receiver, the received signal consists of the desired transmitted signal, interference signals from other man made sources, such as co-channel interference and "other-user" noise and atmospheric noise. The wanted signal is extracted from the noise using one of the three similar techniques, namely: i) active correlation, ii) convolution, and iii) matched filtering. All three techniques are analogous and give similar theoretical performance. However, cost and versatility are the main deciding features. Active correlation, which uses a locally generated replica sequence is inherently addressable, simply by changing the local code, and very easy to implement, except that it requires complex phase synchronisation in the receiver. This technique will be considered first.

In all the methods it is assumed that the received signal has been translated to an appropriate IF frequency or is a baseband model.

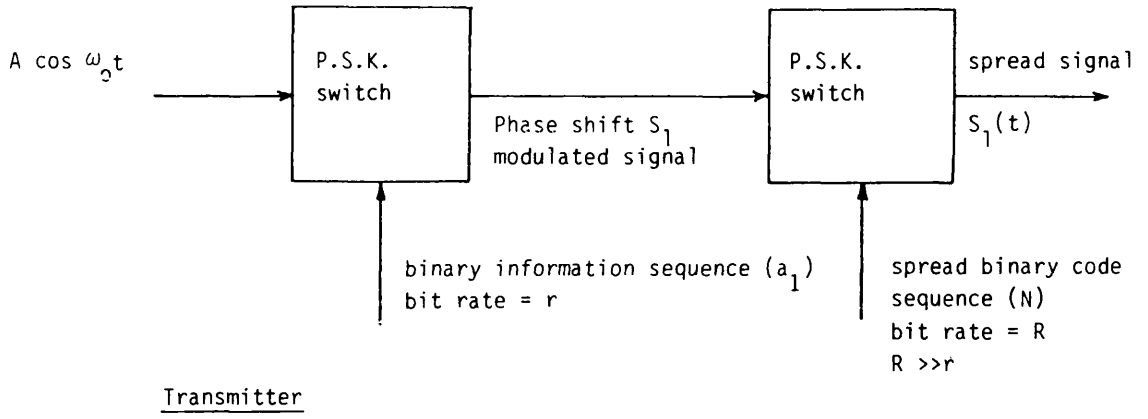
1.4.2.1 Active Correlation

Assume that all processing occurs at baseband. If the transmitted sequence is represented by $S_1(t)$ and the input to the receiver correlation and the replica sequence is $S_2(t)$, the output from an active correlator is:

$$r(\tau) = \int_{-\infty}^{\infty} S_1(t)\ S_2(t-\tau)dt \qquad 1.19$$

If the two sequences are frequency locked and $S_2(t)$ is a true replica of $S_1(t)$ equation 1.19 is simply an autocorrelation function of the spreading function with τ being the time delay between two sequences. The long term integration is often approximated by a low pass filter, or an integrate and dump filter which gives marginally improved performance. Figure 1.9 shows a block diagram of a direct-sequence receiver using active correlation. Low pass filtering is used to achieve the correlation where the data is asynchronously modulated onto the spreading sequence, and the bandwidth is set to be equal to the bandwidth of the original data. Clearly, to optimise the correlation performance the data rate must be much lower than the chip rate of the PN sequence. If the data is synchronously modulated onto the PN sequence, such that one data bit lasts for precisely an entire code sequence, integrate and dump filtering is used. The integrate and dump periods are synchronised to the start and finish of the PN sequence.

For optimum output the relative delay between $S_1(t)$ and $S_2(t)$ must be close to 0. The action of the correlator may also be viewed as a synchronous demodulator, in which all the frequency components



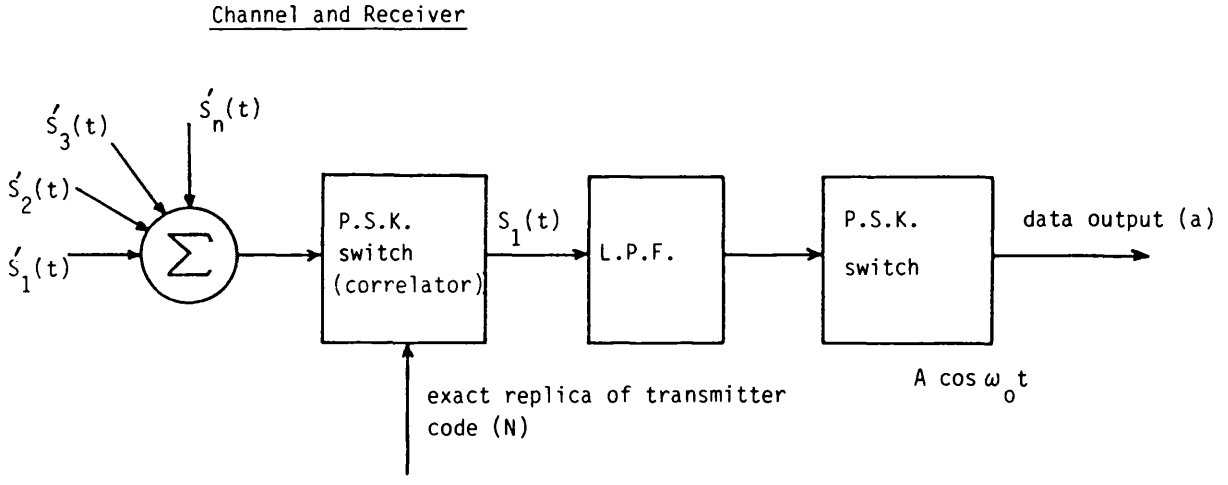
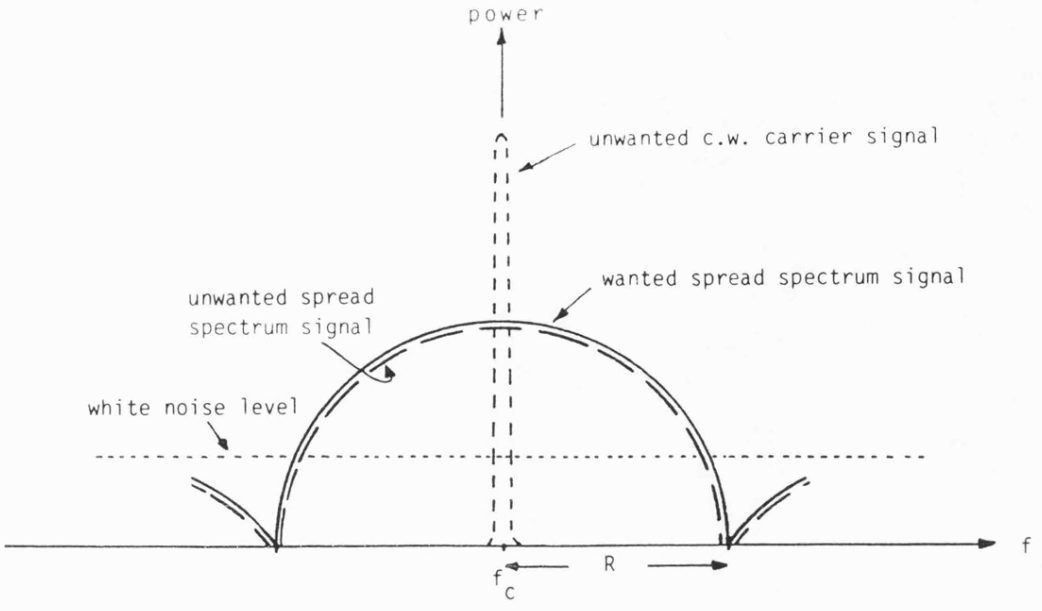


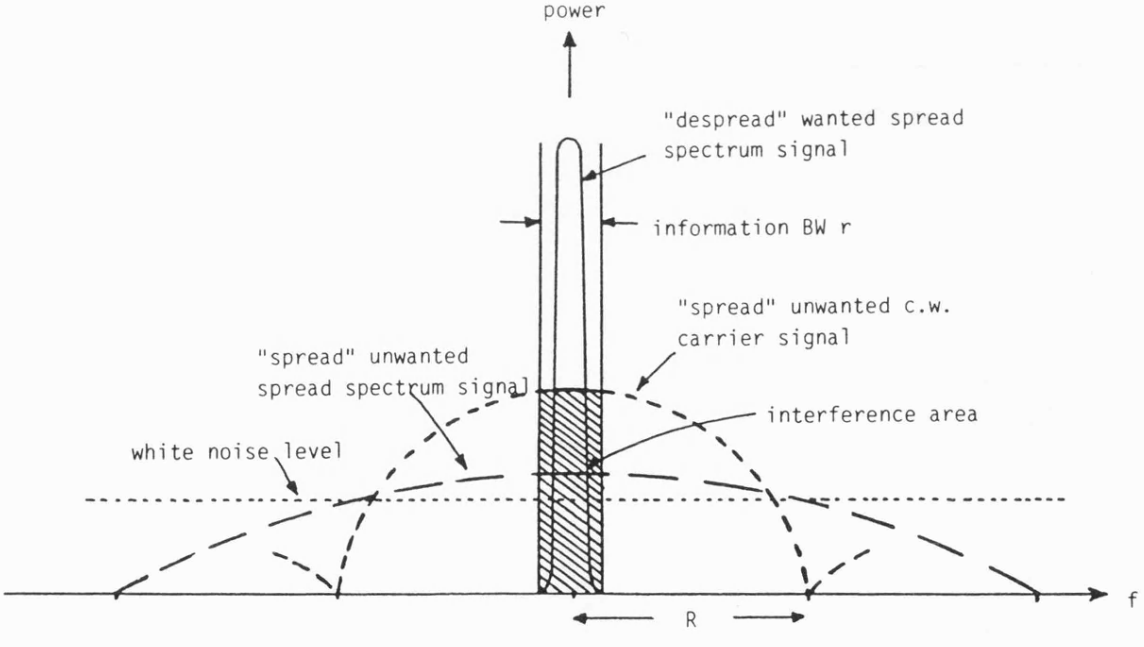
Figure 1.9(a). A practical spread spectrum system using direct code modulation.

$S_1(t) = A \text{ Cos } (\omega_o t + a\pi)$ a = 0 or 1

$S'_1(t) = A \text{ Cos } (\omega_o t + a\pi + N\pi)$, N = 0 or 1



Spectra of input signal



Spectra after correlator

Figure 1.9(b). Spectra of different signals before and after correlation.

of the received signal are translated back by the spectral components in the replica sequence to reveal the data modulation on the received signal.

Noise and interference from other users with different PN sequences are rejected by the correlator to a degree given by their correlation with the replica sequence. White noise, for example is not strongly correlated with the replica sequence, and the noise output from the correlator is determined by the low pass filter bandwidth, or the period of integration in the case of the integrate and dump filter [22]. C.W. narrowband interference, however, does have a measure of correlation and the output from the mixer of the correlator is a signal with a power spectrum

$$\frac{\mathrm{Sin}^2\left(\frac{n\omega_o t}{2}\right)}{\left(\frac{n\omega_o t}{2}\right)^2} \approx G(\omega)$$

Only a small percentage of this wide band signal passes through the post correlation filter, and thus some measure of interference rejection is obtained. Clearly, the so called "process gain" of the system must be dependent upon the type of interference signal. It is also clear that the greater the difference between the bit rate, R, of the PN sequence and the information rate, r, the greater the reduction of the effect of the interference on the wanted signal. There is, however, an optimum bit rate for the PN sequence, under specific types of interference, for which further increases do not result in further improvements in output SNR, and because the input bandwidth is being increased actually makes it more susceptible to white noise interference.

1.4.2.2 Passive Correlation - Matched Filtering and Convolution

The convolution, y(t) between two signals f(t) and g(t) is given by:

$$y(t) = f(t)*g(t) = \int_{-\infty}^{\infty} f(\tau).g(t-\tau)d\tau \qquad 1.20$$

This has a broadly similar type of function to the correlation function discussed earlier.

To achieve analogous operation to the correlator $g(t-\tau)$ is replaced by $f(t-\tau)$. This is not a replica sequence but a **time reversed** sequence.

The action of a matched filter is very similar. If y(t) is the output of the filter of impulse response h(t) subject to an input f(t) then:

$$y(t) = f(t)*h(t) = \int_{-\infty}^{\infty} f(\tau)h(t-\tau)d\tau \qquad 1.21$$

To achieve identical behaviour to the convolver or correlator the transfer functions of the filter must be matched to the input signal f(t). To do this it is necessary to design a filter which has an impulse response which is identical to the time reversed signal. In this case equation 1.20 and equation 1.21 become identical.

Note that the convolver or filter equations require integration with respect to the time delay variable, τ, rather than the time variable, t. This requires special hardware implementations.

Two devices which have been used for convolution and matched filtering operations in spread-spectrum receivers are surface acoustic wave devices (SAW) and charge coupled devices (CCDs).

Figure 1.10 shows an SAW convolver. The SAW device uses

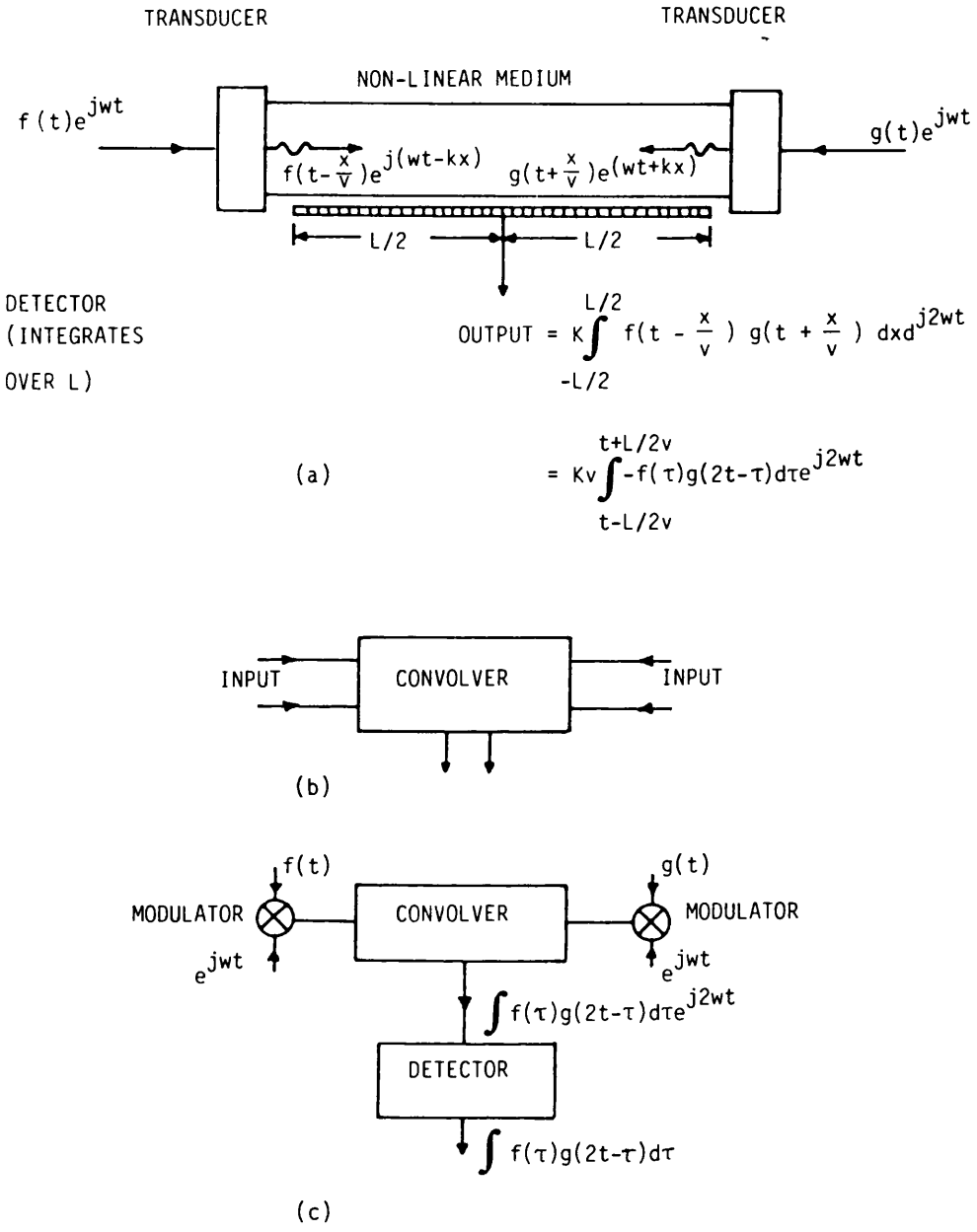


Figure 1.10. Real-time analog convolver using non-linear wave interaction [23].

Rayleigh wave propagation on a crystal of lithium niobate ($LiNbO_3$) or quartz. Both these materials are strongly piezo electric and non linear. Two surface acoustic waves f(t) and g(t) are launched into each end of the SAW device. Mixing of the acoustic wave signals occurs over the length of the device because of the non-linearity and an electrical signal produced from the piezo-electrical effect is developed on an electrode. The length of the electrode effectively determines the integration limits.

The output of the convolver is found to be [23].

$$y(t) = k\int_{-L/2}^{L/2} f(t-x/v) \cdot g(t+x/v)dx \qquad 1.22$$

Here time delay τ is replaced by the time delay of the travelling surface acoustic wave $\tau=x/v$ where v is the wave velocity.

putting $T = [t - x/v]$

and $\frac{dx}{dT} = -v$

gives $y(t) = -k.v \int_{t+L/2v}^{t-L/2v} f(t) \cdot g(2t-T)dT$

i.e. identical in form to the convolution of equation 1.19. This type of device is inherently programmable to any type of binary sequence, and is thus very useful in multiple access systems.

It is also possible to use SAW devices as a matched filter structure [24]. Unfortunately, this type of device is not easily fabricated to be a programmable filter and so it is used in special single user applications such as ranging receivers. This type of filter will not be discussed further.

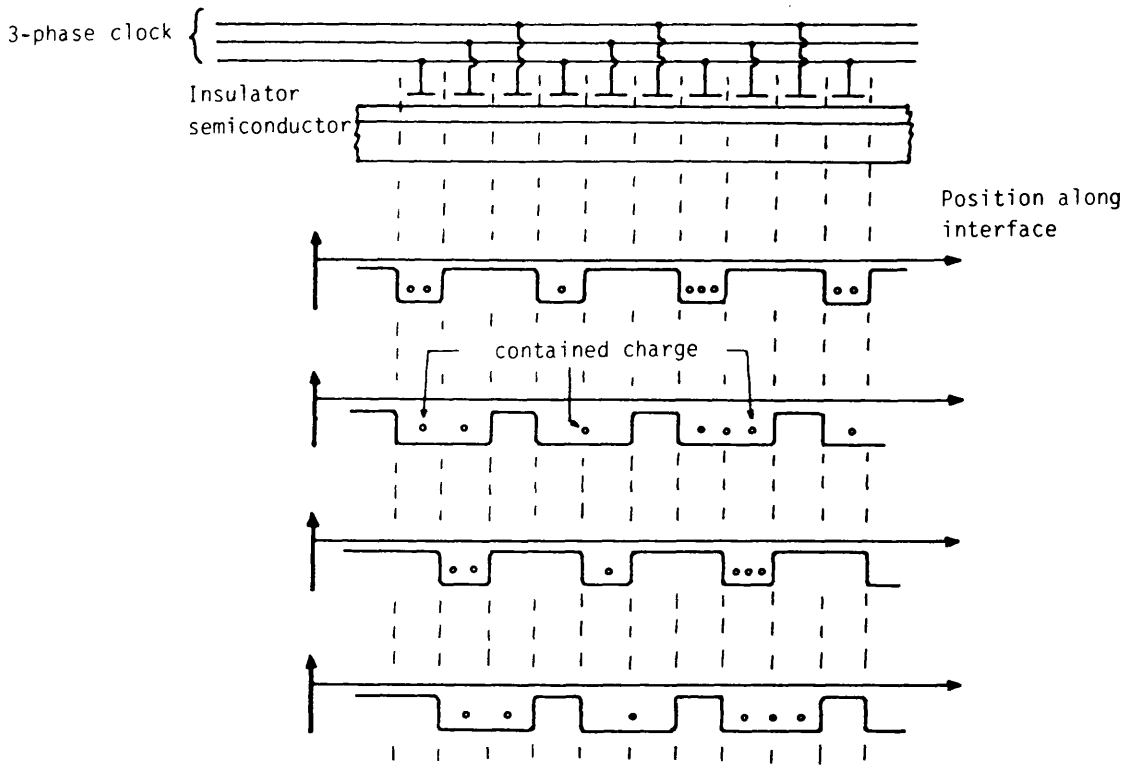
CCD's can be used to make digital filters whose impulse response can be tailored to create matched filters using non-recursive

transversal structures. Like SAW devices [25] CCD's can be used to make analogue delay lines. Figure 1.11(a) illustrates the operation of a CCD. Charge from the input signal sample is trapped in the potential well beneath a MOS structure. By using a 3-phase clock system an alternative electrode, as shown, the potential well, and the charge it contains can be made to move along the device at the clock rate of the filter. It is possible to sense the level of charge beneath any potential well via "taps", and thus these parallel delayed versions of the input signal may be weighted and summed to give the appropriate non-recursive digital filter relationship. A typical matched digital filter realisation of a short code is given in Figure 1.11 (b). The number of tap weights required to make the matched filter equal the length of the sequence, so for long sequences the interconnections become extremely complex. This type of filter is also non-programmable.

1.4.3 System Process Gain

One of the major concerns in spread spectrum systems is the amount of interference rejection possible. The most widely accepted measure of this quantity, termed the system processing gain G_p, is generally given by the ratio of radio frequency bandwidth to the information bandwidth B_R/B_r. Typical processing gains for spread spectrum systems vary from 20 to 60 dB[26]. But in fact this processing gain depends on the technique used and also on the interfering signal stucture.

An idea of the "processing gain" can be obtained by considering the following general argument. Consider that data of bandwidth B_r is uniformly spread to a transmission bandwidth of B_R. The power



a) The three phase charge-transfer process

b) A 13 chip Barker code and a representation of its CCD matched filter.

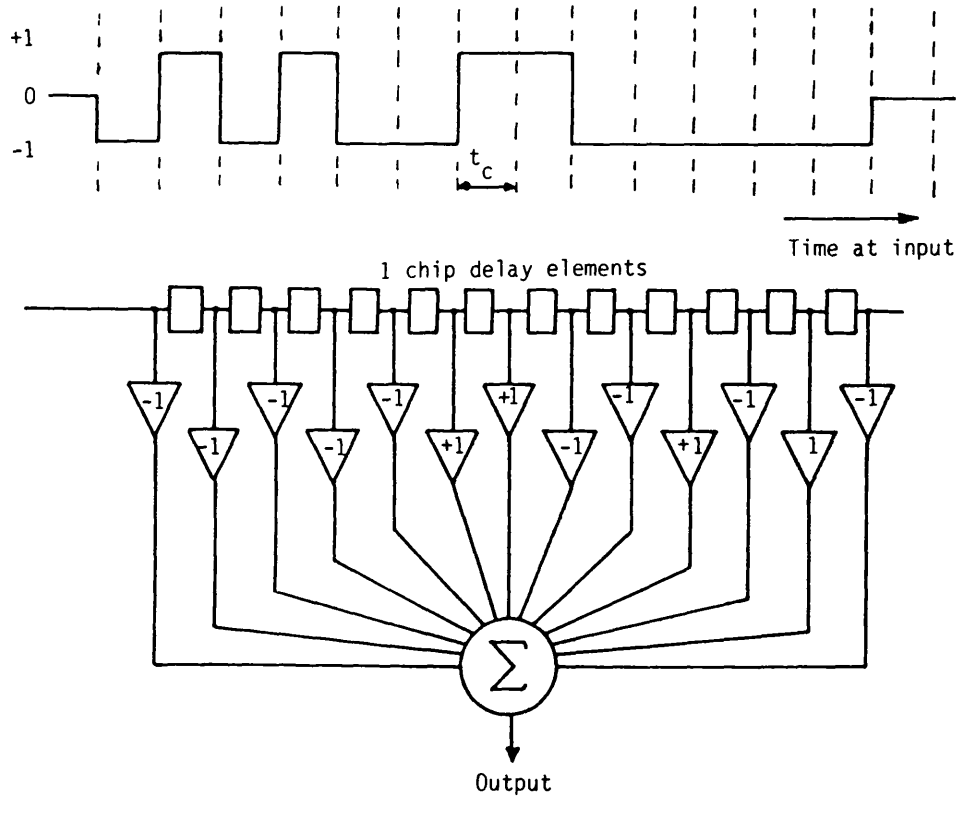


Figure 1.11. Operation of charge couple device [44].

spectral density prior to spreading is P_r over bandwidth B_r so that after spreading the new power spectral density is $P_R = P_r B_r / B_R$ assuming lossless spreading as shown in Figure 1.12. Assuming that this signal is transmitted in a channel which has additive white noise, of noise power spectral density N_o watts/Hz, the incoming signal to noise ratio at the receiver input is thus:

$$\frac{P_R \; B_R}{N_o \; B_R} = \frac{P_r \; B_r}{N_o \; B_R}$$

For an ideal, noiseless, receiver using perfect correlation the required signal will have a power, P_r, as shown earlier in Figure 1.12. The white noise does not correlate with the local sequence and remains at the output of the correlator as noise of power spectral density of N_o watts/Hz. However, after the correlator, a low pass filter of bandwidth B_r can be used to recover all the P_r of the wanted signal. As a consequence, the noise power at the input of the data demodulator is thus now:

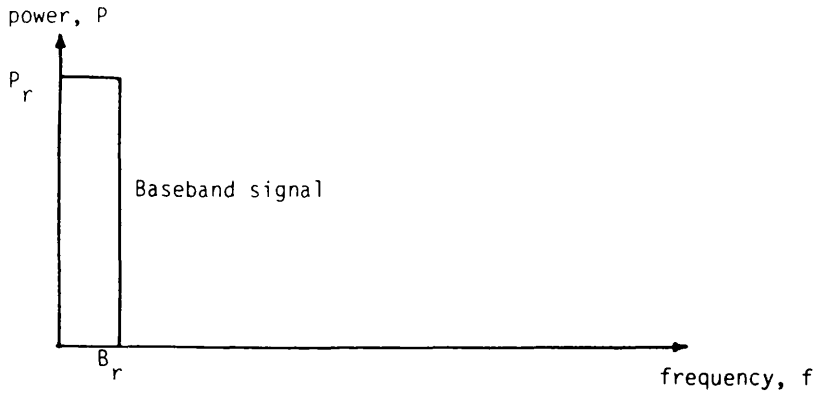
$N_o \; B_r$ watts.

Therefore the signal to noise improvement is

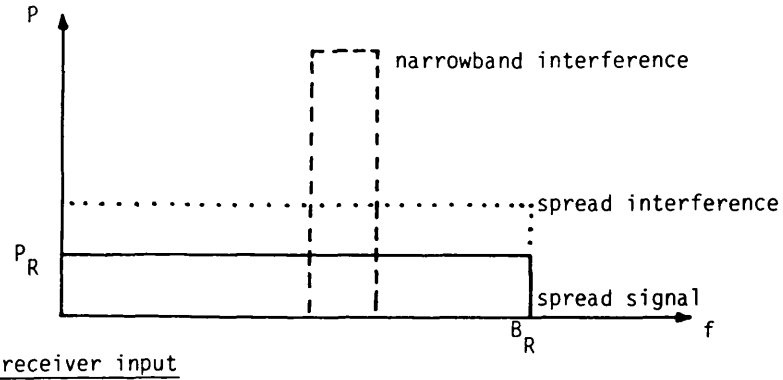
$$\frac{\text{(SNR) receiver correlator output}}{\text{(SNR) receiver input}} = \frac{P_r B_r / N_o B_r}{P_r B_r / N_o B_R}$$

$$G_p = \frac{B_R}{B_r} \qquad 1.23$$

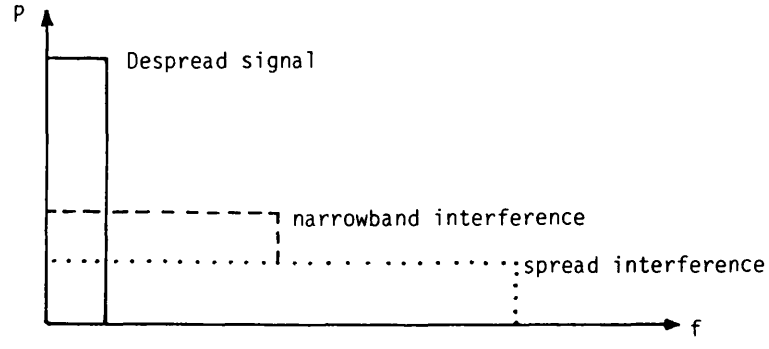
This is a very crude definition, applicable only for uniform spreading in a Gausian broadband environment.



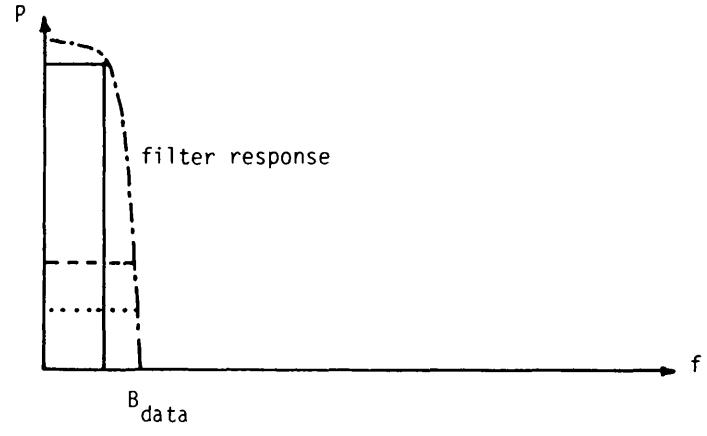
Original signal



At receiver input



At multiplication by despreading signal



After lowpass filter

Figure 1.12. Spectra in a direct sequence S.S. system.

For the case of sinusoidal interference signal, as shown in Figure 1.9(b) the effect of the local spreading code is to spread the power, I, in the sinusoidal signal over the bandwidth of the spreading sequence, B_R. Assuming a flat distribution of the interference, over the bandwidth B_r, the reduction in interference power during the correlation operation is:

$$G_p = \frac{P_r B_r B_R / I B_r}{P_r B_r B_R / I B_R} = \frac{B_R}{B_r} \qquad 1.24$$

In the case where the receiver operates in a multiuser environment, the process gain is slightly different from the earlier two cases. Consider a signal from other spread spectrum users having the same carrier frequency and also code rate as the wanted signal (which is also considered to be the worst case). The interference signal of spectral density I, is spread over a wide bandwidth by the effect of the local code sequence and appears at the correlator output. Assuming a uniform spreading of the spectrum. It has been found [27] that the effective interference power of the post correlation filter has a spectral density of

$$\frac{2}{3}\frac{IB_r}{B_R}$$

so the process gain is

$$G_p = \frac{3}{2}\frac{P_r B_r B_R / 2IB_r}{B_R P_r B_r / IB_R} = \frac{3}{2}\frac{B_R}{B_r} \qquad 1.25$$

To explain the process gain in a numerical example, consider the case in which a certain system operates beneath the atmospheric white noise floor by 25 dBs, and it is required that the signal to noise

ratio to the input of the data demodulator is to be +15 dB for acceptable error rate. The aim is to determine the maximum data rate and the process gain. First, at the receiver, the noise bandwidth must be limited to B_R by RF filtering. So:

Noise power at input = $N_O B_R$

Signal power at input = $P_R B_R = P_r$

$$\therefore (SNR)_{\text{receiver input}} = \frac{P_r}{N_o B_R}$$

$$(SNR)_{\text{of correlator filter}} = \frac{P_R}{N_o B_r}$$

$$\therefore 10 \log_{10} \frac{P_R}{B_r N_o} = +15\text{dB}$$

$$10 \log_{10} \frac{P_r}{B_R N_o} = -25\text{dB}$$

Therefore a process gain of 40 dB is necessary. For uniform spreading, this may be achieved by having a uniform bandwidth spreading ratio of:

$$\frac{B_R}{B_r} = 10000$$

This means that the information rate must be 1/10000 of the total transmission bandwidth. For 10 k bits per sec. data rate, the transmission bandwidth is equal to 100 M bits per sec., which is quite possible using current technology. Assuming that the maximum signal to noise ratio anywhere from the transmitter to the receiver is -10 dB, and the signal to noise ratio prior to demodulator is +15 dB. This means that the lowest allowable signal to noise ratio at the receiver input (after radio frequency filtering) is -35 dB, which allows for a 25 dB fall in signal stength, assuming, that noise floor

is uniform as a function of range.

Sometimes it is possible to relate the process gain to the code sequence length, L, used as a spreading code to the data signal. If the data rate is equal to the code sequence rate the data bandwidth:

$$B_r = \frac{B_R}{L} \text{ Hz}$$

under this condition the process gain is given by:

$$G_p = \frac{B_R}{B_R/L} = L = 2^n - 1$$

For example a 10 stage feedback shift register generator generates a code of length $2^{10}-1 = 1023$, which gives a process gain of $G_p = 30.1$ dB.

1.4.4 Frequency Hopping Systems

Instead of using a fixed carrier frequency, a technique often used to overcome CW jamming is to vary the carrier frequency periodically over a wide frequency band (although the actual bandwidth occupied at any of the carrier frequencies is always the same). In a frequency hopped system a sequence of digital words of n bits/word, of length L words is used to control the frequency of a frequency synthesiser, as shown in the block diagram of Figure 1.13. The rate at which the sequence is clocked determines the rate at which the frequency is hopped. This may be as low as 10-100 hops/second in a slow frequency hopping system to as high as 10,000-100,000 hops/second in a high speed hopping system. The hop rate does not significantly expand the transmission bandwidth. This is set purely by the deviation of the frequency synthesiser, under the control of the code. If the code used is a pseudo-random sequence

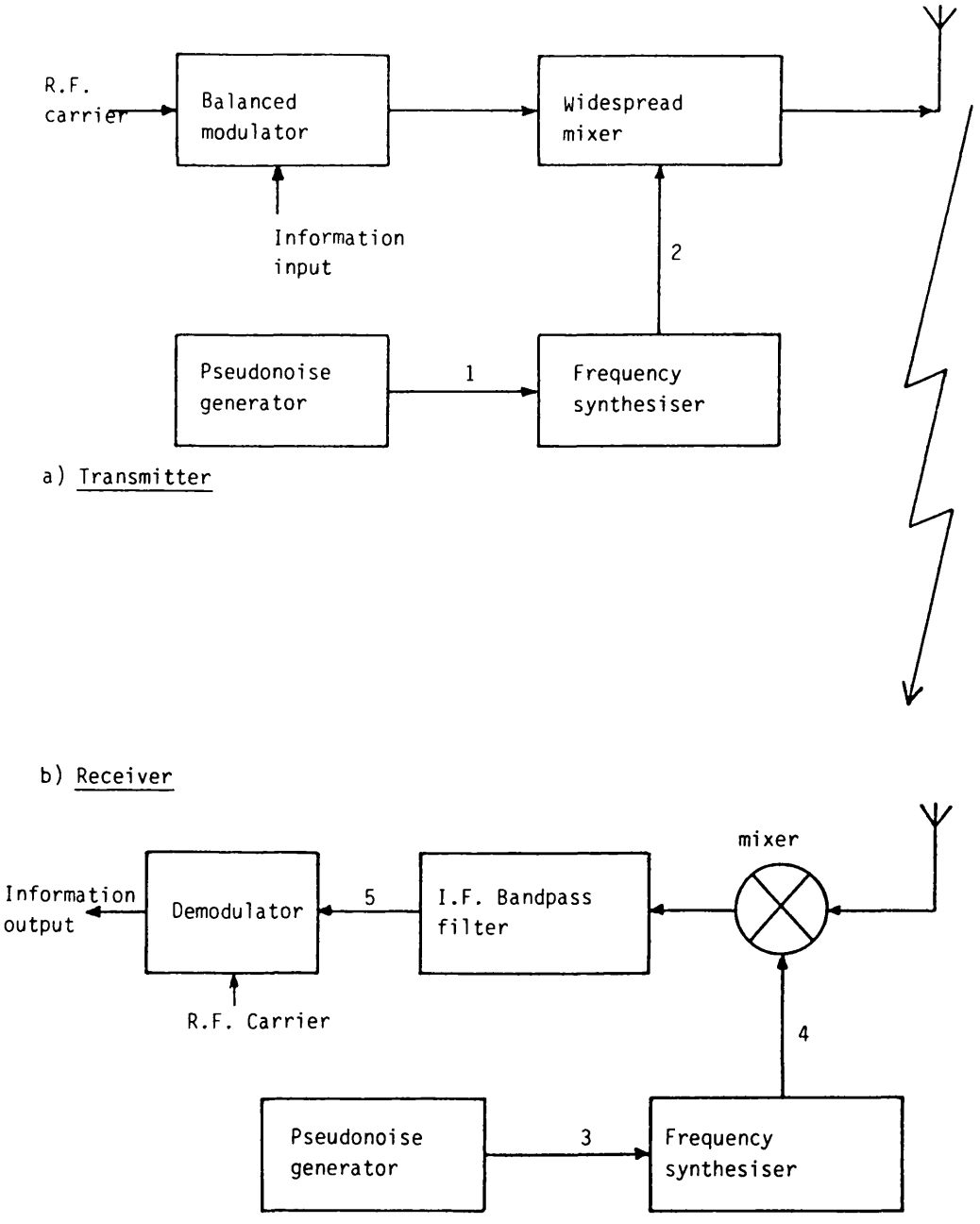
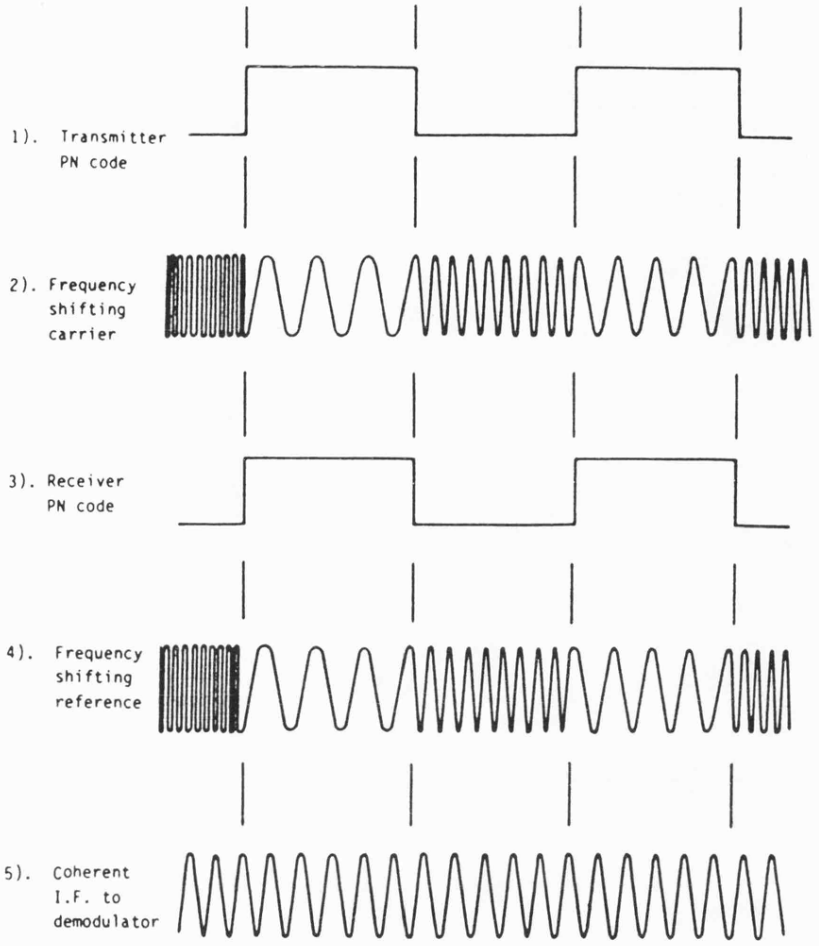
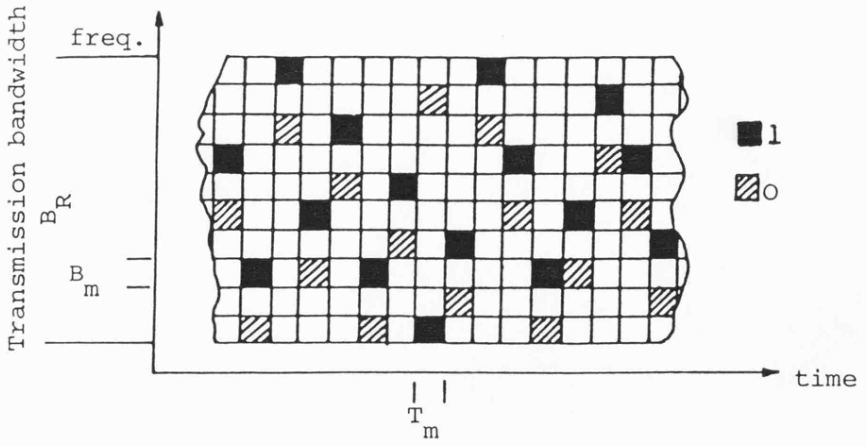


Figure 1.13. Basic frequency hopping system and its waveforms.





c) Typical frequency-time pattern and associated waveforms.

Figure 1.13 (Continued).

the carrier also hops over the allotted bandwidth pseudo-randomly. This can be used to advantage to prevent eavesdropping by tuned receivers, and to minimise the effects of CW jamming. The number of different frequencies used in the hopping system is L, the length of the sequence and, in fact one real frequency hopping system [28] has $\approx 10^6$ discrete frequency choices.

The data to be transmitted may be modulated onto the hopping carrier using any of the conventional methods, such as am or fm. A common technique is to use frequency shift keying in which logic 1 or logic 0 for the data is allocated one of two frequency offsets from the nominal carrier frequency. A typical time-frequency pattern of a frequency hopped system is shown in Figure 1.13(c). The heart of the frequency hopping transmitter is thus a very agile digitally controlled frequency synthesiser. For slow hopping systems this may use a phase lock loop in the synthesiser, in the normal way. However, for fast hop systems it is necessary to use direct synthesis of the frequency. This involves generating a large number of frequencies from a single source using counter circuits, and mixing the appropriate frequency components together via a D type bistable to achieve other frequencies in the set. This approach is very fast, as it only requires data selector gates to be switched, but because many frequency components are generated in parallel it is obviously very costly. The latter method of generating frequency components can also be useful in reducing spectral pollution, and optimising the SNR in the receiver. Considering the first, it is necessary to minimise sudden phase changes when each new frequency is selected. Instantaneous changes in phase produce a wide spread of frequency components. It is thus necessary for there to be a

coherent transition from one frequency to the next to minimise phase noise. Appropriate gating of the direct synthesiser can achieve this.

The design of the frequency hopped transmitter should be such that its tranmission is distributed evenly over every available frequency "slot" in the band and that it transmits as much of the power in each channel as possible. This means that the transition from one frequency to another must not only be coherent but must take a very small fraction of the time actually spent at that frequency, otherwise power in the recovered signal is lost during the transition.

A block diagram of the receiver of a frequency hopped system is shown in Figure 1.13(b). The heart of the receiver is also a frequency synthesiser controlled by a replica sequence to the transmitted sequence. All frequency slots in the receiver are offset by a fixed IF frequency. However, if the two sequences are correctly phase synchronised, the received signal is always translated back to the same IF frequency, irrespective of the actual instantaneous frequency. The signal at the IF will in fact be either an amplitude modulated signal, or an fsk signal, depending on the original modulation and this can be recovered in the normal way.

In a common channel multi-user system each user has a unique sequence. Consequently the transmitters hop from one frequency to another within the allocated bandwidth. The various transmitters may operate synchronously [29] (controlled via a separate synchronising channel) or asynchronously. In the latter case there is a probability that two transmitters will simultaneously transmit on the same frequency. This can act as interference, however, because both

sequences are different the interference only exists from that interferer for the one chip period of the sequence. Averaged over a long period the interference is given by the cross-correlation between the two sequences for the given phase offset in a similar way to a direct sequence system.

In the case where the channels of the frequency hopping system are contiguous, the process gain is identical to that of a direct sequence system, in its general form given by:

$$G_p = \frac{B_{R.F.}}{B_{infor.}} \qquad 1.26$$

However, when the channels are not contiguous, the process gain is better determined by the number of available frequency choices, and clearly it is not dependent on the clock rate of the pseudo noise sequence. This indicates that a lower clock rate can be used in the frequency hopping system and this has no effect on the bandwidth of the transmitted signal.

In the receiver, it is the type of signal produced in the intermediate frequency bandwidth which determines the quality of the reception. Hence, whenever any frequency component of the dehopped undesired signal falls in its intermediate frequency bandwidth, interference is produced, and this will take place in these two cases. The first one is where the frequency synthesiser in the receiver is producing frequencies which are non-ideal and contains frequency shift components that correspond to that contained within the undesired signal. It can be said that the extend to which this will take place depends upon the degree of correlation between the codes of desired and undesired signals. The second case is where

the intermodulation between two or more interference signals results in an intermodulation product, which can match frequencies generated by the frequency synthesiser in the receiver.

The interference contribution in frequency hopping systems depends mainly on hopping rate. For a high hopping rate the interference appears to be small and continuous because it is noise like, and spread in a $(\sin x/x)^2$ fashion by an amount roughly equal to the hopping rate and this spread will exceed the information bandwidth, whereas, for low hopping rates, for example 10 or 20 hops per second, the occurrence of interference is high but intermittent with periods of one hop duration suffering heavy interference separated by long periods of interference free reception. Thus in the design of frequency hopping system a choice has to be made between which kind of interference is acceptable and preferred. If a high frequency hopping rate than the information rate is incorporated in the design, there is a problem that only a few thousands of hops per second are produced by the frequency synthesiser. The second problem is that of avoiding the individual dehopped unwanted components when the synthesiser jumps from one frequency to another [30].

For the potential eavesdropper, if the hopping rate is quite fast relative to the data bandwidth and the hopping range is very large as well as large changes in frequency on each hop, then it is very difficult for him to asynchronously change his local oscillator frequency and therefore cannot obtain a coherent version of the data. The eavesdropper knows the existence of the signal but cannot capitalise on it, or a jamming attempt on one frequency will leave thousands of other frequencies unjammed because without prior

knowledge of the spacing of the frequency components and the number of the spectrum this may be impossible even with a very high spectrum analyser. However, the receiver of the wanted signal has the advantage of knowing which frequency is coming next since it knows which code is being used.

If the spread spectrum system is subject to narrowband interference or CW jamming the recovered data may be corrupted by the interference, for the duration of one hop. For all other hop frequencies the CW signal will be mixed to a frequency outside the IF bandwidth of the receiver, and will thus have no effect. If this CW interference is large the data may be wrongly decoded. If there are L frequencies to which the carrier may hop the probability of the data being corrupted is:

$$p(E) = \frac{1}{L}$$

This assumes that the interfering signal is much larger in amplitude than the frequency hopped signal. Unless L is large the probability of a data error can be unacceptably large. To improve matters coding of the original data to incorporate error correcting codes must be used, but this reduces the actual data rate.

If the interference is white Gaussian noise it is unlikely that the power in the noise over a bandwidth B_M will be greater than the transmitted signal, and so the frequency hopped signal is relatively immune to white noise. Interestingly, the direct sequence system tends to be more tolerant of CW interference rather than white noise. We see that the effects of interference are reduced if the noise is different from the type of signal used i.e. CW interference compared

with a broadband direct sequence system or white noise compared with a narrowband frequency hopped system.

Multipath signals do not create any interference provided that the propagation delay of the reflected signal is greater than $1/f_n$ where f_n is the hop frequency. If the propagation delay is less than this, frequency selective fading will occur in the usual way. Clearly the use of frequency hopped systems to overcome rapid fading is not possible unless the hop rate is relatively high, in excess of 10kHz.

1.4.5 Time Hopping Systems

In frequency hopping systems the code sequence is used to control the frequency of transmission. On the other hand, time hopping uses this to control the transmission time period.

The construction of time hopping systems is normally very simple and as such they have found application in multiple access and particularly ranging. Basically, time hopping incorporates conventional pulse modulation, where a pseudo noise code sequence turns the transmitter ON and OFF in a pseudorandom manner.

Thus in practice an average transmit duty cycle of nearly 50% is obtained due to the number of ones and zeros in the pseudo noise code sequence being nearly equal. A block diagram of the time hopping system is shown in Figure 1.14. The modulator operates in a simple fashion being able to accept any pulse modulatable signal source which is capable of following code waveforms. An N-input gate could easily act as a keying control. This would sense some previously chosen state of a shift register and hence turn to control the output signal of the transmitter.

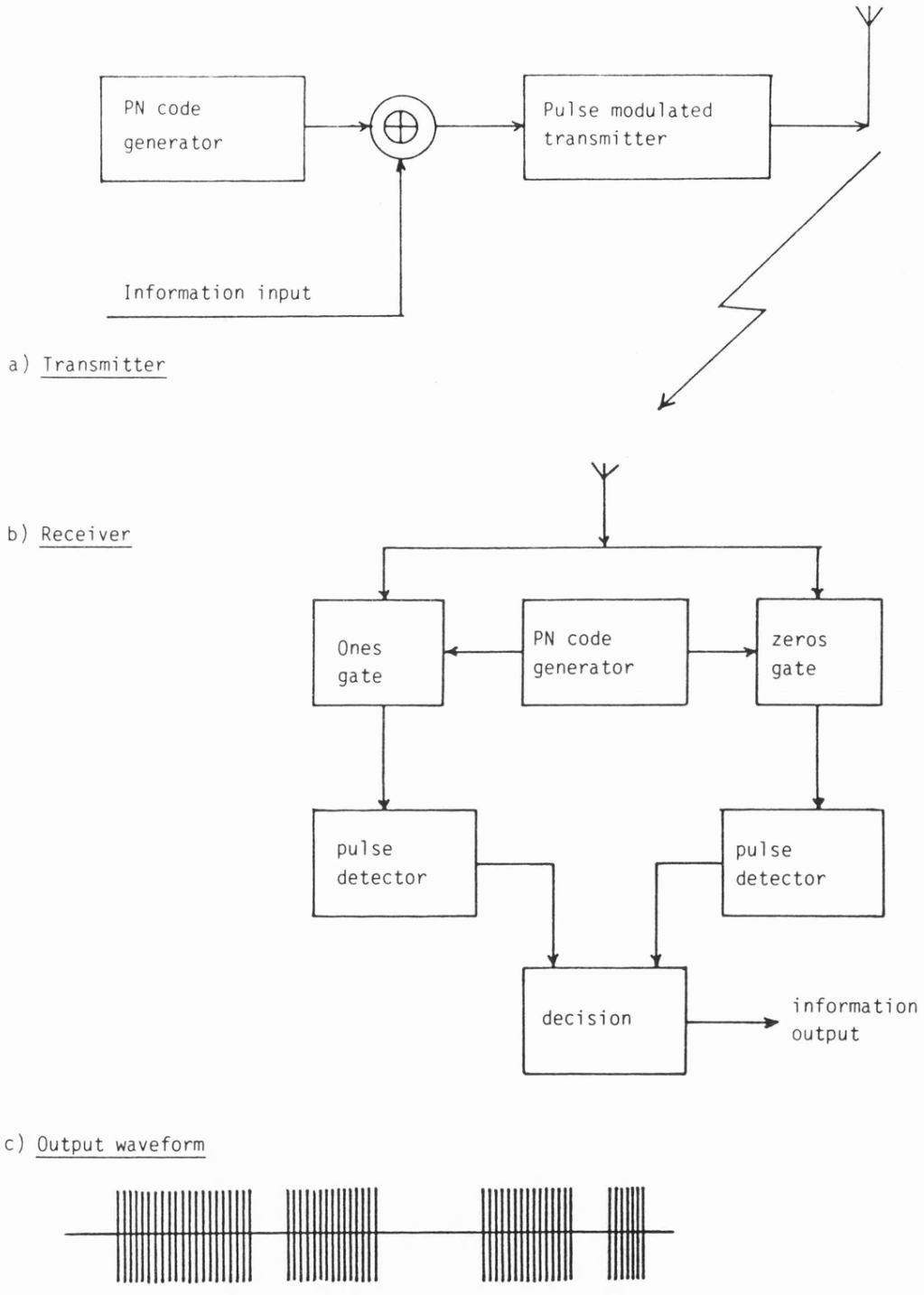


Figure 1.14. Simple time hopping (pseudonoise pulse) system.

The disadvantage of simple time hopping systems is that they have inefficient interference rejection. In particular, a continuous carrier which has a frequency identical to the centre frequency of the receiver cannot be eliminated and thus leads to the blockage of the system. In order that an interfering transmitter can have any real chance of causing disturbances to the transmitted signal in the time hopping system, it must be operated continuously as the code sequence is unknown to it. This counts as a point greatly in favour of the time hopping system since its duty cycle is much lower and in fact the power for this reduced duty cycle is less by a factor equal to the signal duty cycle when compared with that of the interfering transmitter.

The combination of time and frequency hopping techniques forms the basis for one form of time division multiple access (TDMA) system. In practice, this is frequently used to overcome the disadvantages in time hopping systems, where the presentation of a continually interfering transmitted signal could lead to the blockage of communication between users [16].

1.4.6 Chirp System

Pulse-Frequency modulation or chirp systems have been widely used in radar. In their fundamental form, the signals used are simple and do not use coding as in other forms of spread spectrum modulation to spread their transmitted signal bandwidth. Swept-frequency pulses, similar to those from a sweep generator are employed, by which the transmission bandwidth is extended to a greater extent than needed so that it achieves high process gain, without use of any code sequence. Pulsed radio frequencies vary in a

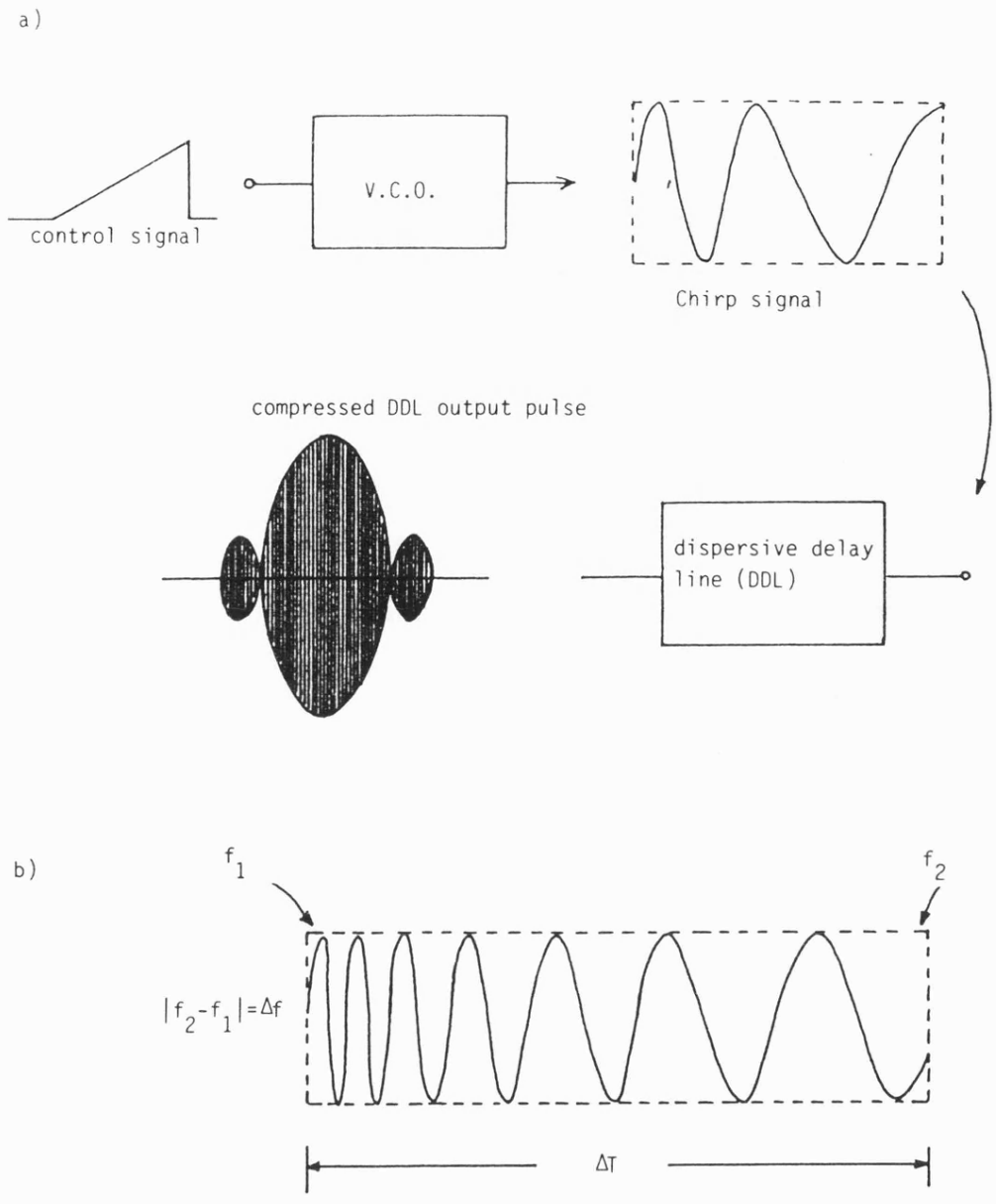


Figure 1.15 Chirp system waveform.

a) Typical chirp waveforms.

b) Transmitted chirp signal (one sweep).

known manner during each pulse. The greatest advantage in its use lies in the reduction of transmitted power.

The receiver employs a dispersive or matched filter, to match the angular rate of change of the transmitted frequency swept signal and to compress it into a much narrower time slot such that it behaves in the same way that a high power (but narrow) pulse does [16]. Therefore it is commmonly used in radar and also in communications, where reduction of power is an important factor [31]. Figure 1.15 shows a typical chirp system.

1.5 GENERATION AND PROPERTIES OF CODES

1.5.1 Feedback Shift Register Generators

With the exception of chirp spread-spectrum systems, which do not employ spreading sequences, all other spread-spectrum systems rely on the properties of the spreading function to achieve their interference rejection properties. For ease of generation the spreading sequences are generally binary codes. For optimum performance the sequences need to have properties which are close to a random binary sequence. However, for the case of generation and synchronisation the codes must also be deterministic and relatively easy to generate. Although it is possible to generate a perfectly random sequence, since a replica is required in the receiver phase locked to the transmitter it is unrealistic to expect that synchronisation could be maintained when the channel fades and either the transmitter or receiver is subject to Doppler Shift.

Linear feedback shift register sequence generators are capable of producing large numbers of different codes, some of which are very well suited as spreading functions. These codes are periodic, rather

than truly random, however the length of the sequence can be made extremely long, in excess of 10^{26} bits, with a corresponding long period of the sequence. With such long sequences the properties of the sequence closely approach that of a random sequence if the observation time is restricted. The great advantage of a shift register sequence generator is that it is relatively straightforward to programme and load the sequence generator with an initial starting state so that both transmitter and receiver sequences can be initially synchronised.

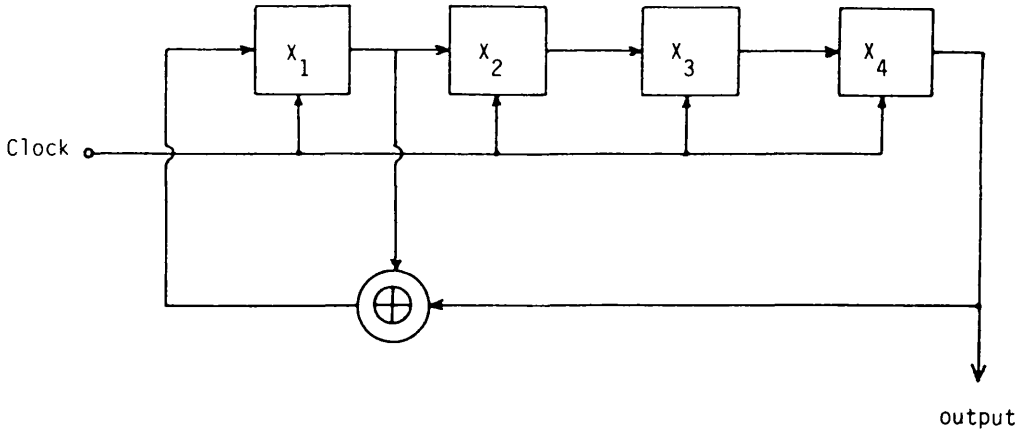
A shift register generator produces sequences which depend on the length of the shift register, the feedback tap connections and the initial starting state of the sequence. The codes produced in this type of generator may be grouped into two classes; maximal length sequences (m-sequences) and non-maximal length sequences.

1.5.2 Maximal Length Sequences

The maximal length sequence is the longest code sequence that can be produced by a given shift register generator. If the shift register has n stages the length of a maximal sequence is:

$$L = 2^n - 1 \text{ chips}$$

and then the sequence repeats. If the sequence length is less than $2^n - 1$ the sequence is non-maximal. The maximal sequence contains every 'n' tuple except the all zero's state. If the all zero's initial state is loaded into the register an auxiliary sequence of the length of one chip is produced. The number and position of the feedback taps dictate whether the sequence is maximal or non-maximal. Figure 1.16(a) shows a block diagram of a typical maximal length



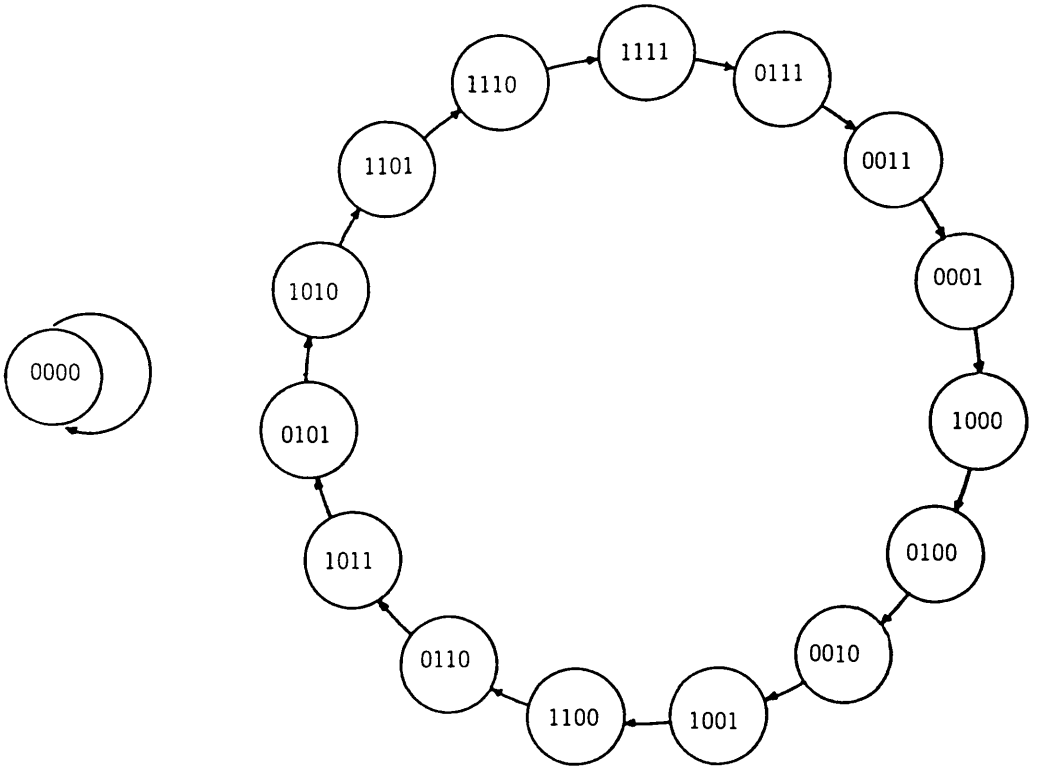
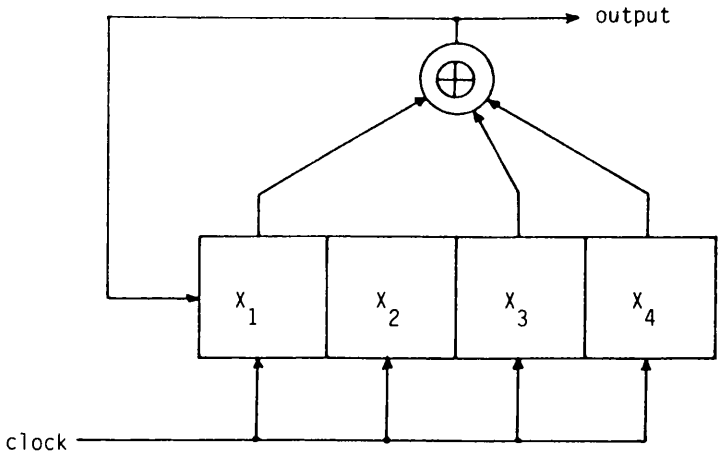


Figure 1.16(a). Block diagram of a 4-stages feedback shift register and its (2^n-1) stages, generating maximal length sequence.



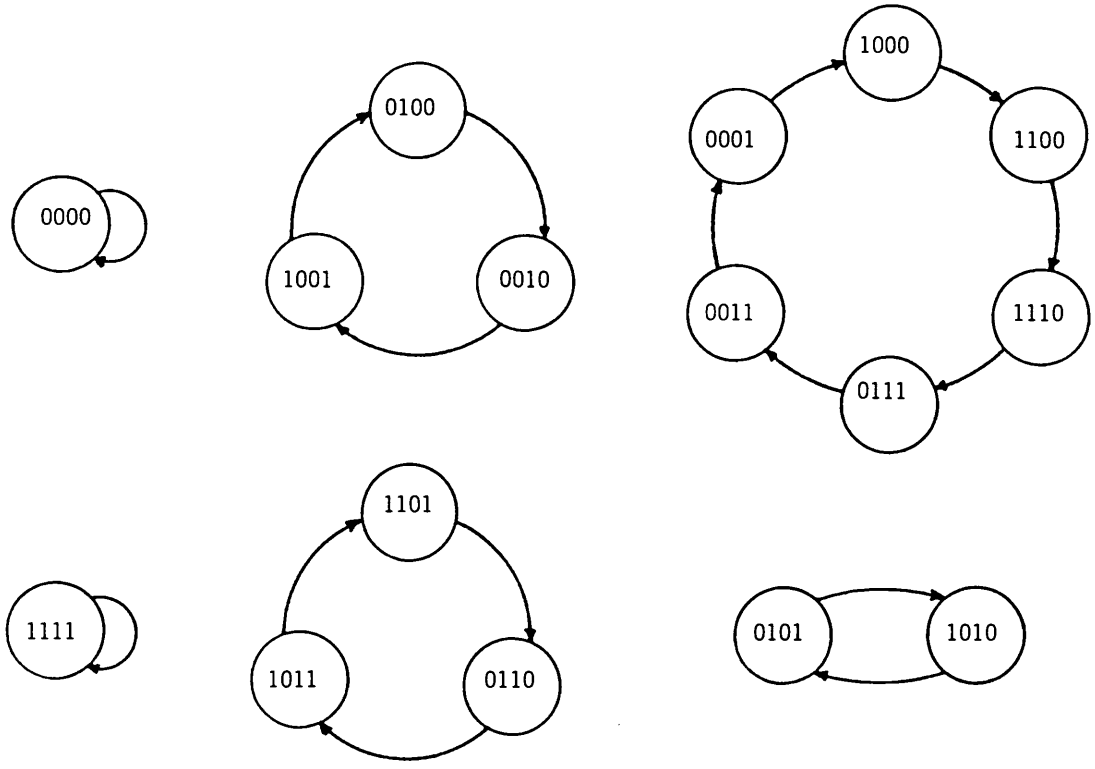


Figure 1.16(b). Non-maximal sequences generated from a 4-stages feedback shift register with data feedback 1 ⊕ 3 ⊕ 4.

shift register generator of length 15 chips (n=4). Here the taps are taken from the last and first stages and modulo added together before feeding the result to the input of the shift register. Also shown in this diagram are six other non-maximal sequences.

In general, the n stage register has a feedback function

$f(x_1, x_2 \ldots x_n)$

where $x_1, x_2 \ldots x_n$ represent the output states of the shift register. The taps are selected by the switching functions $C_1, C_2, \ldots C_n$ which is either 0 or 1 depending on whether a tap connection is made or not.

Thus:

$$f(x_1, x_2 \ldots x_n) = C_1.x_1 \oplus C_2.x_2 \oplus C_3.x_3 \oplus C_4.x_4 \ldots C_n.x_n \qquad 1.27$$

where $\oplus$ indicates a modulo 2 addition and $C_1.x_1$ is the AND function.

The output of the feedback function is fed back to the input of the register. Clearly it is the choice of the feedback function which determines whether the sequence will be maximal length or not. In general, the correlation properties of maximal sequences tend to be better than those of non-maximal sequences. Peterson [32] has produced a table of different feedback connections for maximal length sequences for between 2 to 89 stages, so that sequences of any length from 3 to 6.189×10^{26} chips are easily available.

A code sequence used for spread-spectrum systems must have the following qualities [17]:

1. Good autocorrelation properties which have two distinguishable levels and low cross-correlation properties.

2. Sufficient length to support maximum-distance ranging systems such as the Ranger project and the Venus space probe.

3. Sufficient length to support the expected jamming margin.

4. There must be a large family of sequences having all the same correlation properties.

5. Ready implementation.

Maximal length sequences are frequently employed to satisfy these requirements. Given below are the properties of these sequences.

1. The number of ones in a sequence exceed the number of zeros by 1 (because the all zero's state does not occur in the sequence. This is called the balance property.

2. The statistical distribution of ones and zeros is well defined and equal. Relative positions of the runs of ones and zeros vary from sequence to sequence, however, the number of each run length does not vary between sequences of a given length. For long sequences the run property of maximal sequences is similar to random sequences in that runs of 2 consecutive 1's occur half as frequently as runs of 1, etc. for longer runs.

Because of these randomn properties maximal length sequences are often called pseudo-noise sequences.

3. The autocorrelation function of a maximal length sequence is such that for all values of phase shift the normalised correlation value is -1/L, except for phase shifts in the range

of $-1<\tau<1$ bit where the correlation varies linearly from -1/L to +1 (where L is the sequence length). This correlation property will be discussed in Section 1.6.

4. A modulo-2 addition of a maximal length sequence with a phase shifted replica of itself results in another replica with a different phase shift from either of the originals. This is called the linear addition property.

5. Every possible state or 'n' tuple of a given n stage generator exists at some time in the sequence with the exception of the all zero's state. Each state lasts for one and only one clock bit. This is called the state exhaustion property.

Zieler [33], has shown that the number of different maximal length sequences produced by an n stage shift register generator is given by:

$$N_m = \frac{\phi(2^n-1)}{n}$$

The expression $\phi(x)$ is an Euler number and represents the number of positive integers, including 1 that are relatively prime to and less than (x).

1.5.3 Combination Code Sequences

These are non-maximal length sequences, nevertheless they have useful properties in spread-spectrum systems, as will be stated. The most important of the combination sequences are the Gold sequences [34, 35], the JPL ranging codes [36], and the composite sequences [37]. This last types is sometimes called a Kronecker sequence [38].

Although all these types of sequence are not maximal length sequences some of them do use maximal length sequences in their construction. Some of these sequences will be explained here.

Gold code sequences [34, 35]: A block diagram of a Gold code sequence generator is shown in Figure 1.17. The two codes 1 and 2 are maximal length sequences generated from two separate feedback shift registers, 1 and 2, respectively clocked by the same frequency and combined together by modulo-2 addition to form a Gold code sequence. The two equal length maximal length sequences may have different or identical feedback functions but with different initial starting states. The length of the resulting sequence is the same as the length of code 1 or code 2, i.e. $L=2^n-1$. Two main advantages are obtained from generating the Gold sequences. The first advantage is that a very large number of codes can be obtained, much larger than the number of maximal length sequences of length n. In fact there are (2^n-1) different gold sequences generated from only two maximal length sequences, each of length (2^n-1) plus the two generating sequences. This large number of sequences is, of course, ideal for large multi-user CDMA systems, particularly since the number of maximal length sequences of length less than 1023 bits is extremely limited, and insufficient to provide a sufficiently large number of address codes. However, this gain in the number of address codes would be lost if the auto-correlation and cross-correlation properties were significantly worsened. Fortunately, it is possible to select Gold code sequences in which the correlator properties of all the sequences in the set are uniform, bounded and well-defined,

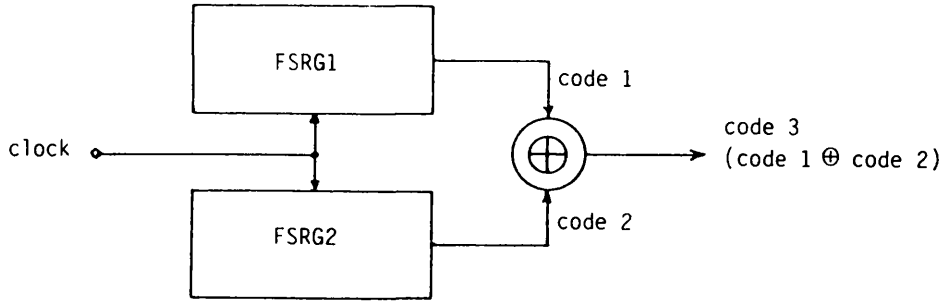


Figure 1.17 Gold code sequence generator configuration.

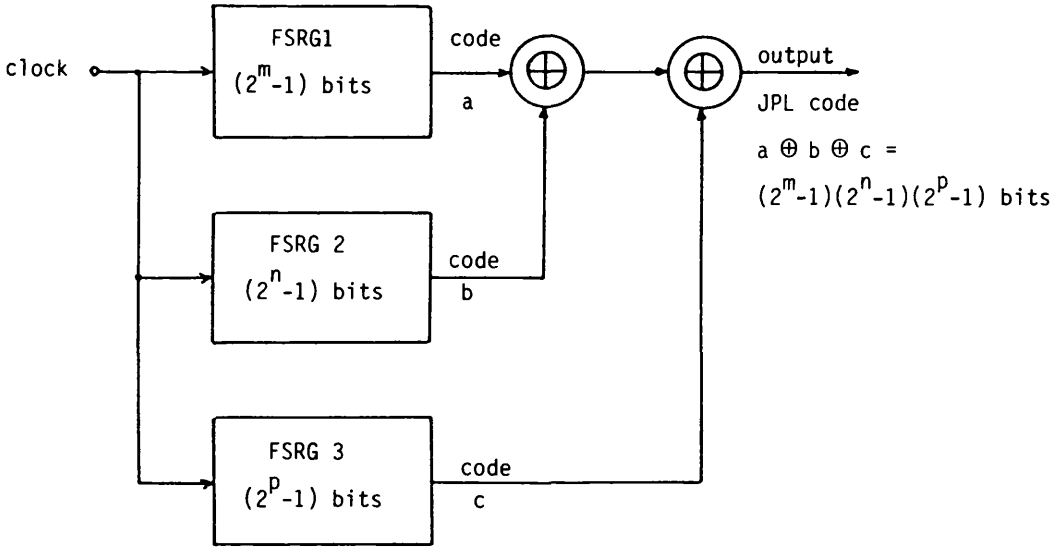


Figure 1.18. Typical JPL code sequence generator configuration.

in a way which would be impossible to obtain by maximal length sequences.

Gold [35] has given an algorithm for selecting the feedback taps to achieve preferred Gold sequences (i.e. those with the best cross-correlation performance) and has further shown that the cross-correlation function of these preferred sequences is three valued. For these sequences the peak cross-correlation value between the two generating maximal sequences a and b is:

$$\Psi_{ab}(\tau)_{cross} \leq 2^{(\frac{n+1}{2})} + 1 \quad \text{for n odd}$$

$$\Psi_{ab}(\tau)_{cross} \leq 2^{(\frac{n+2}{2})} + 1 \quad \text{for n even}$$

and the three cross correlation values for the resulting Gold code are for n odd:

$$-1 \ , \ -(2^{\frac{n+1}{2}} + 1) \text{ and } (2^{\frac{n+1}{2}} + 1)$$

In other words the peak cross-correlation is no worse than the cross correlation value of the two generating sequences.

Unfortunately, because the Gold sequences are non maximal, the auto-correlation function is not two valued, but four valued.

Three of these values are identical to the three cross correlation values, and the fourth is the normal autocorrelation peak of unnormalised value:

$2^n - 1$

Thus, although the cross correlation value is not worsened, the "index of discrimination" is lower for the case of the Gold code. The index of discrimination is defined here as the difference between the magnitude of the peak autocorrelation value and the magnitude of the worst case autocorrelation side lobe. Although not a serious drawback, when compared with the advantage of a large number of different sequences, reduction of the index of discrimination reduces the system processing gain, and the ability to synchronise in noisy conditions [39].

JPL ranging codes [36]: the configuration of JPL ranging code is identical to that of the Gold code except for the difference in the individual code lengths. The JPL codes are constructed from two or more maximal length sequences whose lengths are relatively prime to one another, the output of which are modulo-2 added to form the resulting sequence, as shown in Figure 1.18. The JPL code's length is equal to the product of the individual code lengths. The advantage of this technique is that the overall code length can be very long, which is useful for providing unambiguous information of range over very long distances. The other advantage of the JPL code is that because it is composed of two shorter sequences synchronisation of the receiver can be accomplished by separate operations on the component codes which are much shorter than the overall length of the JPL code. This type of sequence is used exclusively for ranging applications and thus the cross correlation performance is not important.

Composite or "Kronecker" sequences [37, 38]: These sequences are similar to the JPL sequences in that they use two sequences except

that for composite sequences the clock rate of one individual sequence is slower than the other individual sequence by the length of the latter. In other words, one entire bit of the slow, outer, sequence is modulo-2 multiplied by a much higher speed code to produce a long high speed code. These sequences will be explained in detail in Chapter Five as well as their properties and advantages.

The other type of sequence applications found in multiple access systems is the family of Barker codes [40]. These consist of a finite number of ± symbols and have unique properties in that their aperiodic correlation values are ±1/L, where L is the code length. However, there are only a few known Barker codes, and these can be found in [41].

1.6 AUTO- AND CROSS-CORRELATION OF CODES

In the design of spread-spectrum systems, both the auto-correlation and cross-correlation properties of the codes are of vital importance when determining the performance of a multi-user system. Furthermore, since the power spectrum of a signal is related to its auto-correlation function via the Wiener-Kintchine relationship [30] knowledge of the auto-correlation function of a sequence can be used to determine the frequency spectrum of the signal.

Factors such as the code type, length and bit rate all affect the correlation properties of the code. Consequently, the spectrum of data modulated by a maximal sequence will be considerably different from data modulated by a Gold code or JPL code. This may have important consequences in system design.

1.6.1 Auto-Correlation Function

The auto-correlation function of a waveform is defined as the time average of the waveform multiplied by a time shifted version of itself. Therefore, it is a function of the time shift, τ. Where the waveforms are of binary type, τ can be, for convenience replaced by the number of bits displaced. It can be said that the time average of the waveform is really a measure of the DC component, or for a binary waveform, the imbalance between the number of ones and zeros.

Auto-correlation in general is defined as the integral:

$$\Psi_{auto}(\tau) = \lim_{t \to \infty} \frac{1}{2T} \int_{-T}^{T} f(t) f(t+\tau) dt \qquad 1.28$$

which is a measure of how similar the signal is to its phase shifted replica. To get a representation of the correlation between two binary waveforms, or sequences, the product (or for simplicity's sake the modulo-2 addition) of the sequence is taken, bit-by-bit. It will be noted that an agreement leads to a zero and a disagreement to a one.

The correlation Ψ between the sequences is then given by:

Ψ = number of zeros - number of ones

The normalised form Ψ' is sometimes used to express the correlation, where Ψ is divided by the total number of bits in the sequence [30], i.e.

$$\Psi' = \frac{\text{number of zeros - number of ones}}{\text{number of zeros + number of ones}} \qquad 1.29$$

Therefore, for zero shift between two sequences

$\psi' = 1$

and for the case of maximal length sequences for a shift other than zero or multiple of periodic length

$\psi' = \frac{-1}{L}$ where L is the code length = $2^n - 1$

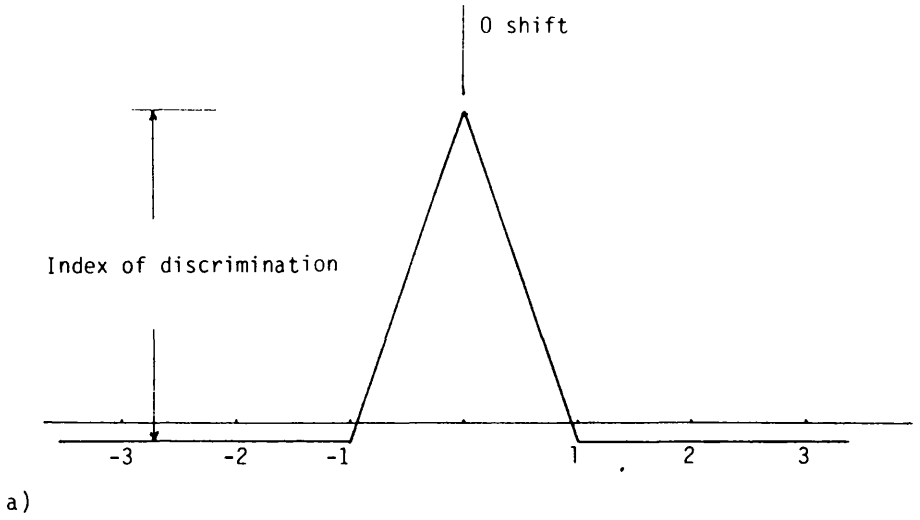
As an example, consider a three stage shift register generating a maximal length sequence of period T bits. The autocorrelation for all shifts of the sequence is given below:

$S = S_1\ S_2\ S_3,\ S_3 \oplus S_2 \rightarrow 1$

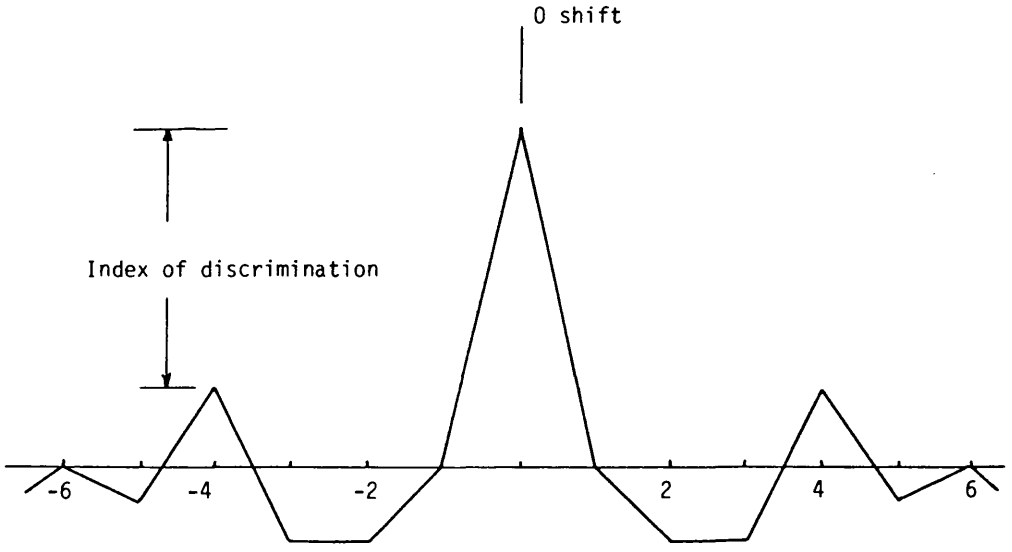
Reference sequence: 1 1 1 0 0 1 0

Shift	Sequence	Agreements	Disagreements	A-D
1	0 1 1 1 0 0 1	3	4	-1
2	1 0 1 1 1 0 0	3	4	-1
3	0 1 0 1 1 1 0	3	4	-1
4	0 0 1 0 1 1 1	3	4	-1
5	1 0 0 1 0 1 1	3	4	-1
6	1 1 0 0 1 0 1	3	4	-1
0	1 1 1 0 0 1 0	7	0	7

It is to be noted that A-D (net correlation) is -1 for all shifts except zero shift or synchronous condition, and $2^n - 1 = 7$ for zero shift condition. All maximal sequences have this characteristic. The correlation increases or decreases linearly in the region between zero and plus or minus one bit shift respectively so that the autocorrelation function for an m-sequence is triangular



a)



b)

Figure 1.19 Auto-correlation function.

a) Maximal sequence.

b) Gold sequence.

as shown in Figure 1.19(a). Similarly the auto-correlation function of other types of sequences can be calculated. A typical example of Gold sequences is shown in Figure 1.19 (b).

1.6.2 Cross-Correlation Function

Cross-correlation is the measure of similarity between two different code sequences, which is quite useful in designing a spread spectrum system where the receiver is not allowed to respond to any signal, other than the proper addressing sequence. The general integral for cross-correlation is:

$$\Psi_{cross}(\tau) = \lim_{t \longrightarrow \infty} \frac{1}{2T} \int_{-T}^{T} f(t)\, g(t+\tau)dt$$

In spread spectrum systems the effect of cross-correlation between the local code and the code of the undesired signal manifests itself as a part of the interference signal power appearing as an unspread component in the receiver. Figure 1.9(b) shows how the signal appears in the data bandwidth instead of being spread as a noise like signal. This results in two effects, first, "coherent" interference may be caused by the unspread signal to the wanted signal and thereby lower the performance, second, false correlations may occur when the local receiver is trying to synchronize with the wanted signal, and thus delay or even stop the desired signal from being detected [30].

From examination of the sequences produced by the modulo-2 sum of the two sequences under consideration, the degree to which code sequences suffer from unwanted cross-correlation can be calculated.

The following is an example of the normalised cross-correlation function that has been generated by a three states and two stages

shift register for two simple m-sequences:

First sequence

($n = 3$, $2^n - 1 = 7$) 1 1 1 0 1 0 0

Second sequence

($n = 2$, $2^n - 1 = 3$) 1 1 0

The two sequences are now compared with bit-by-bit until both sequences have repeated extra number of times. This will occur after $3 \times 7 = 21$ bits.

First sequence 1 1 1 0 1 0 0 1 1 1 0 1 0 0 1 1 1 0 1 0 0

Second sequence 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0

Mod-2 sum 0 0 1 1 0 0 1 0 1 0 1 1 1 1 1 0 0 0 0 1 0

number of zeros in mod-2 sum = 11

number of ones in mod-2 sum = 10

$$\therefore \psi' = \frac{11-10}{11+10} = \frac{1}{21}$$

The above calculation shows the value of the cross-correlation function for the two sequences to be very small and invariant for all cyclic shifts. In fact it can be shown that for any two such as those in the example, that have lengths that contain no common factors, their cross-correlation function is relatively small. Such sequences are termed "relatively prime". In practical spread spectrum systems it is often necessary to choose a common code length for all signals, so care must be taken in choosing a set of codes that have good mutual cross-correlation properties. Even if the

sequence length is a prime number there can be no guarantee that the cross-correlation function for a particular set of sequences will be small. No general method of predicting the exact cross-correlation behaviour appears to exist at the present time [30, 35].

The quotient of auto-correlation function ($\neq 0$) to autocorrelation function (0) for Gold sequences of length $2^n - 1$ is less than

$$\frac{2^{(n+1)/2}}{2^n-1} \qquad \text{for n odd}$$

$$\frac{2^{(n+2)/2}}{2^n-1} \qquad \text{for n even}$$

The same bounds are valid for the cross-correlation coefficient between different Gold sequences.

For maximal length sequences, the bounds are: the quotient of auto-correlation function ($\neq 0$) to auto-correlation function (0) for a sequence of length 2^n-1 is:

$$\frac{-1}{2^n-1}$$

1.7 MODULATION OF THE SPREAD DATA ONTO THE RF CARRIER

After spreading the baseband data by the high speed code it is necessary to modulate this signal with the RF carrier prior to transmission. Direct sequence modulated spread spectrum systems are quite similar in many ways to more conventional digital communication systems. They employ:

i). Amplitude Shift Keying (ASK): In this type of modulation the carrier amplitude is switched between the two or more values, usually ON or OFF for binary signal. The resultant modulated signal then

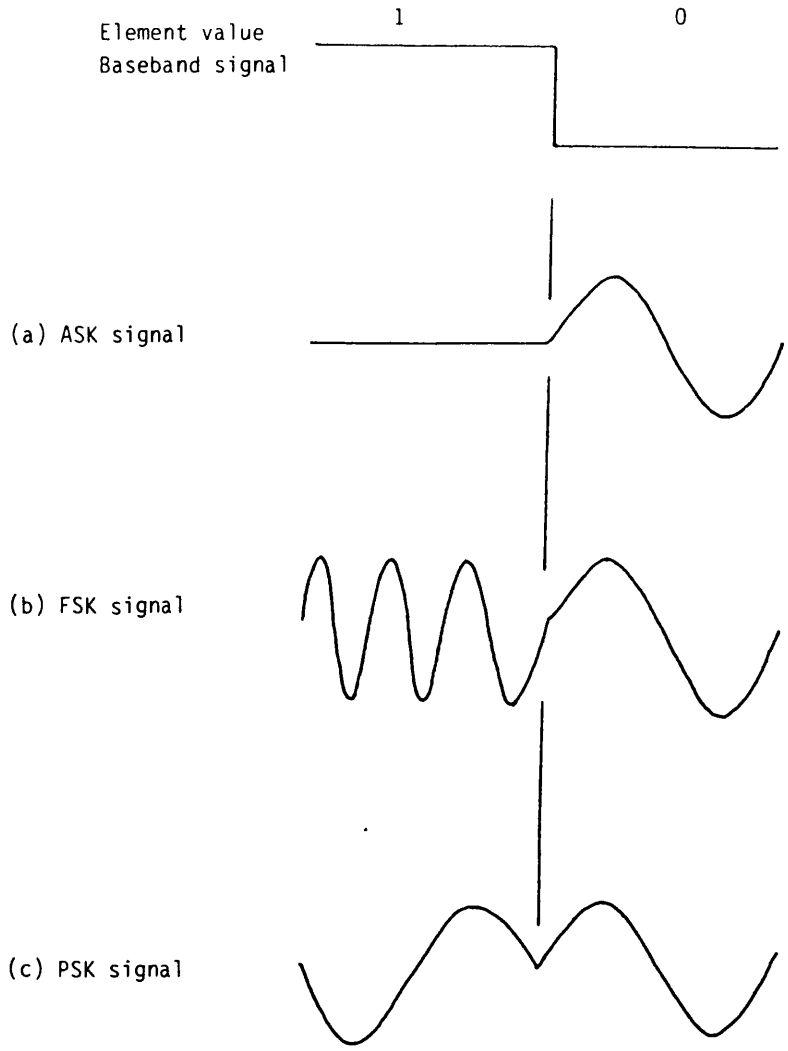


Figure 1.20 Basic types of modulation.

consists of radio frequency pulses or marks, representing binary 1 and spaces of zero amplitude representing binary 0.

ii) Frequency Shift Keying (FSK): In frequency shift keying, the instantaneous frequency of the carrier signal is switched between two (or more) values in response to the high speed code. The binary FSK signal is clearly the sum of two complementary ASK signals of different carrier frequencies. There is no phase change here in the signal carrier at the boundary between two signal-elements.

iii) Phase Shift Keying (PSK): Here, the phase modulated signal uses the same carrier frequency for the two binary elements, with a phase difference of π rad between the carriers of the two elements. This is also a suppressed carrier ASK signal, whose two binary elements are negatives to each other. Other types of PSK modulation include quadrature phase shift keying QPSK in which the carrier frequency is subject to shifts of 0, $\pi/2$, π and $3\pi/2$ rad. The QPSK modulation can be viewed as the sum of two BPSK signals in phase quadrature. The three modulation methods are illustrated in Figure 1.20.

In a spread spectrum system, the main concern in choosing a modulation signal is the distribution of power spectral density over the bandwidth.

1.7.1 The Spectrum of the Transmitted Sequence Modulated Data:

The unwanted sidelobe energy was found to be different from one type of modulation to another [42, 43]. Figure 1.21 shows the one sided spectrum of three types of modulated signals: QPSK, BPSK and MSK. Here, MSK (minimum shift keying) will refer to the generic family of signals for which:

1) The modulating pulse is symmetrical about t=T/2, 0 otherwise.

2) The modulated carrier has a constant envelope. Signals such as ASK and FSK are related to the MSK's family.

Of the signals available, the MSK-like signals appear to be the most promising. They offer two significant advantages. Firstly, their inherent reduced sidelobe energy levels, when compared to BPSK and QPSK modulated signal. Secondly the MSK family of signals has minimal incidental amplitude modulation, so that they can be filtered and then passed through non linear processing without significant regeneration of the original sidelobe structure. BPSK and QPSK signals have 100 percent incidental AM that cannot be reduced by filtering, and non-linear processing reconstructs the sidelobes as if they were never reduced [42].

Referring to Figure 1.21, it is seen that the first null is at a frequency of 1/2T hertz for QPSK, 0.75/T hertz for MSK, and 1/T hertz for BPSK. The null to null bandwidths for the bandpass spectra are twice these values. It will also be noted that the sidelobes for MSK fall off at a rate of 12 dB per octave, while the sidelobes for BPSK, QPSK fall off at half this rate.

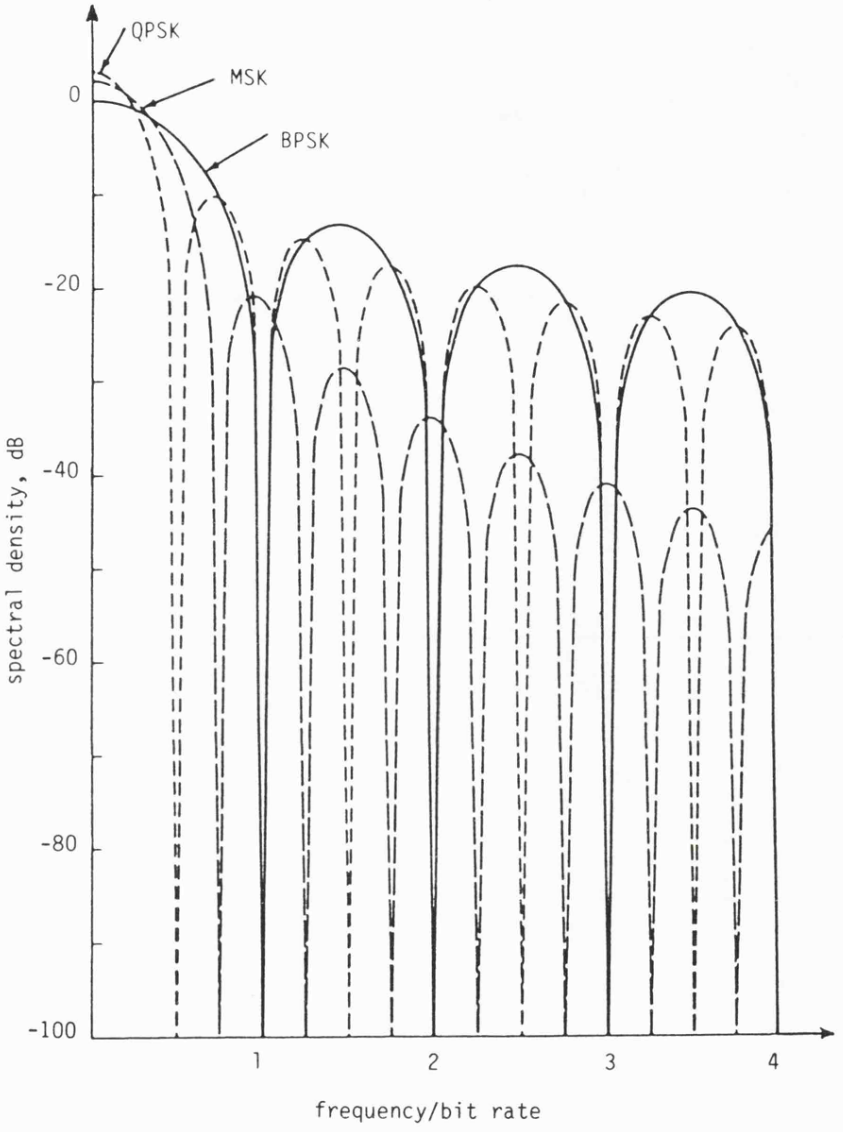


Figure 1.21. Power spectra for QPSK, MSK, and BSK.

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CHAPTER TWO

SYNCHRONISATION AND TRACKING OF SPREAD SPECTRUM SYSTEM

2.1 INTRODUCTION

In spread spectrum communications, initial code synchronisation and maintenance of code synchronisation plays a vital role in the separation of wanted and unwanted signals, since the phase of the locally generated code in the receiver is the key to the despreading process. Although the requirements of the frequency hopping and direct sequence systems, with respect to synchronisation, are broadly similar, there is more flexibility in the case of the former. In chirp systems, however, the synchronisation does not exist in the same manner, but on a pulse-by-pulse basis. This is because the chirp systems have a dispersive filter in the receiver and this provides rapid pulse correlation [1].

For those systems which employ code sequences, the receiver must recognise both the bit rate and the frame of the received wanted signal very rapidly and then generate a replica of it before any communication can take place over the link. Usually this process is accomplished with two main associated criteria : i) usually no **a priori** information about the received code phase is available to the spread spectrum receiver; ii) as a spread spectrum system is intended to be operated in a multiple access mode, the receiver has to perform under conditions of extremely poor signal to noise ratios, usually considerably less than 0 dB.

The problem of synchronisation in spread spectrum systems is undoubtedly the hardest and the most critical part of the system, especially if the transmitter and/or receiver are not fixed but

moving at a high spead, where the Doppler frequency offset has a significant influence on the timing of the system. The other major problem is the length of the pseudo noise spread code. As most spread spectrum users tend to use very long sequences, for reasons discussed earlier, acquisition of synchronisation can be a very lengthy process.

The problems can be divided into two parts:

- Initial synchronisation
- Tracking.

2.2 INITIAL SYNCHRONISATION (ACQUISITION)

This is the mechanism by which the bit rate and the frame of the received signal is detected initially by the receiver. This process may involve a preliminary coarse synchronisation procedure followed by a fine synchronisation system. Ultimate phase synchronisation to better than 10^{-2} bit should be possible in noise free environments.

Many techniques for achieving initial synchronisation have evolved, some with simple requirements, others with complex implementations for both direct sequence and frequency hopping systems. Most of these techniques use either an active correlator or passive correlator at the heart of the system.

The main differences between an active and a passive correlator lie in the form of the reference pseudo noise sequence generated in the receiver. In the former, a synchronous replica of the pseudo noise sequence is generated as a real time waveform for multiplication with the received signal and the resulting signal filtered to around the data bandwidth or integrated over the data bit

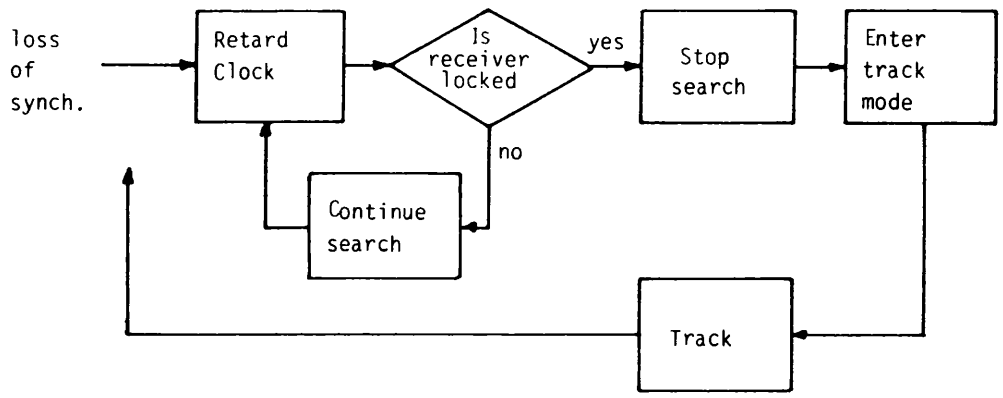
duration to approximate the correlation of the two signals. In the passive correlator however, the received signal is multiplied by a **fixed** reference copy of the pseudo noise sequence embedded in the transfer function of a matched filter and the result integrated over the data bit duration.

Some of the methods used in these techniques are listed below:

- Serial synchronisation
- Synchronisation preambles
- Transmitted reference method
- Universal timing
- Burst synchronisation
- Sequential estimation
- Special coding for acquisition of synchronisation
- Synchronisation by a microprocessor control system
- Techniques employing tapped delay line.

2.2.1 Serial Synchronisation

By far the most commonly used synchronisation techniques are the serial search techniques. Any sychronisation scheme that operates its code sequence at a rate different from the transmitter's code generator is classified as a serial synchronisation system, or is said to use serial search [2]. In this technique the two code sequences slip in phase at a constant rate with respect to each other, stopping only when the synchronisation point is reached, as shown in the flow diagram of Figure 2.1(a). Because of the nature of the pseudo noise code involved, which gives rise to the two level auto-correlation functions (shown in Figure 2.1b) the receiver examines all possible code phase positions until the peak of the



a) Flow diagram of sliding-correlator synchroniser.

b) Block diagram.

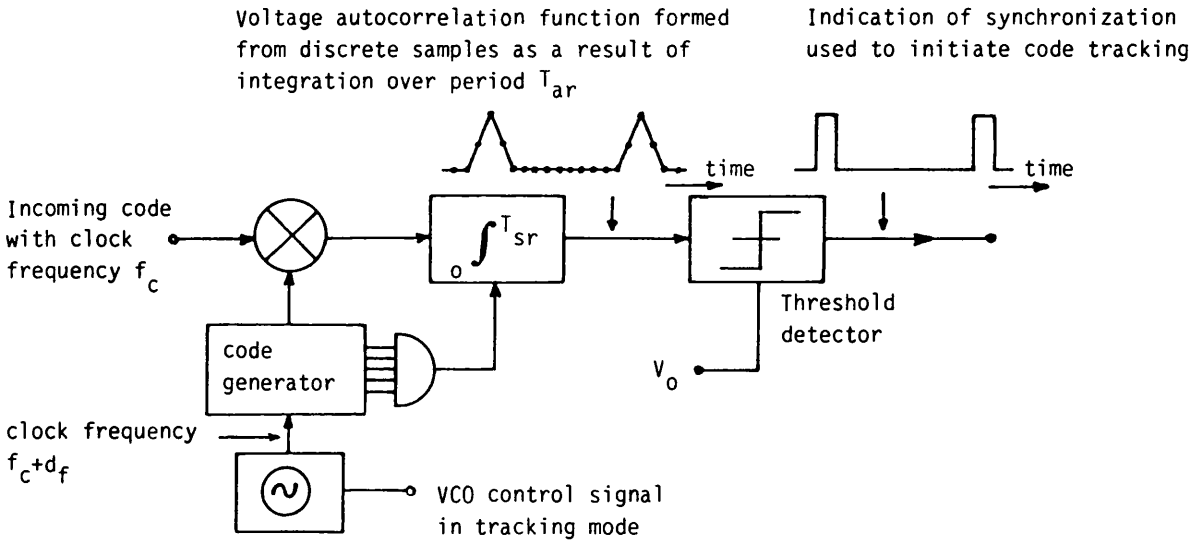


Figure 2.1. Sliding correlator synchronizer.

auto-corrlation triangle is detected, at which the search is stopped and the tracking circuit initiated to maintain the received and the locally generated code sequences in synchronisation. If the tracking attempt is considered unsuccessful (on the basis that the correlation value cannot be maintained) the coarse synchronisation process is restarted. This type of search process is sometimes called a "sliding" correlator. An analysis of this method has been developed by Sage [3]. The advantage of the sliding correlator is its simplicity, since it requires few extra circuits such as a correlator, threshold detector, and code frequency controller as well as the tracking circuit. However, the problem of using a simple sliding correlator, is that, when a long sequence is used the examination of all possible phase positions is very long and it is limited in response time by the bandwidth of the system's post-correlation receiver. For example, a system with a post-correlation (baseband) receiver bandwidth of say 1 kHz could recognise synchronisation in approximately 0.35 ms (by applying the general rise time-to-bandwidth relation T_r=0.35/BW) [1], and the time used to slide through the point of correlation (taking into account the correlation function is two bits in width) should be minimum of this amount. The maximum search rate then would be approximately $2/T_r$ or 5.7 K bit S^{-1} [1].

2.2.2 Synchronisation Preambles

The search time is an important parameter in spread spectrum communication, and this time depends mainly on the length of the sequence used. Consider, for example, a system with a code sequence

length of $(2^{10}-1)$, or 1023 bits, having the same bandwidth and hence the same maximum search rate, as the example considered in Section 2.2.1. The search time is:

$$T_s = \frac{1023}{5700} = 0.179 \text{ sec.}$$

However, if the length of the sequence is increased to $(2^{15}-1)$ or 32767 bits, the search time also increases to:

$$T_s = \frac{32767}{5700} = 5.748 \text{ sec.}$$

note that those two search times are calculated under the assumption that the synchronisation peak is detected in the first pass.

In the synchronisation preamble technique, a special short code sequence, which has special rapid acquisition parameters, is used at the beginning of each transmission. However, the code properties which allow the preamble synchronisation method to work rapidly compromise the correlation properties and the noise rejection property is worsened, and this increases the likelihood of possible false correlations due to interference. Typical synchronisation preambles range in length from several hundred bits to several thousand, depending on the specific systems requirements. The following four criteria generally set the limits on the preamble's length: 1) minimum preamble code sequence length is bounded by the cross-correlation function, 2) interference rejection requirements, 3) maximum code sequence length is set by maximum available acquisition time, and, 4) the code repetition rate may tend to be bounded by the preamble code length in either direction so that the preamble repetition rate does not fall within the information

bandwidth of the system, so that it could appear as an interference signal [1].

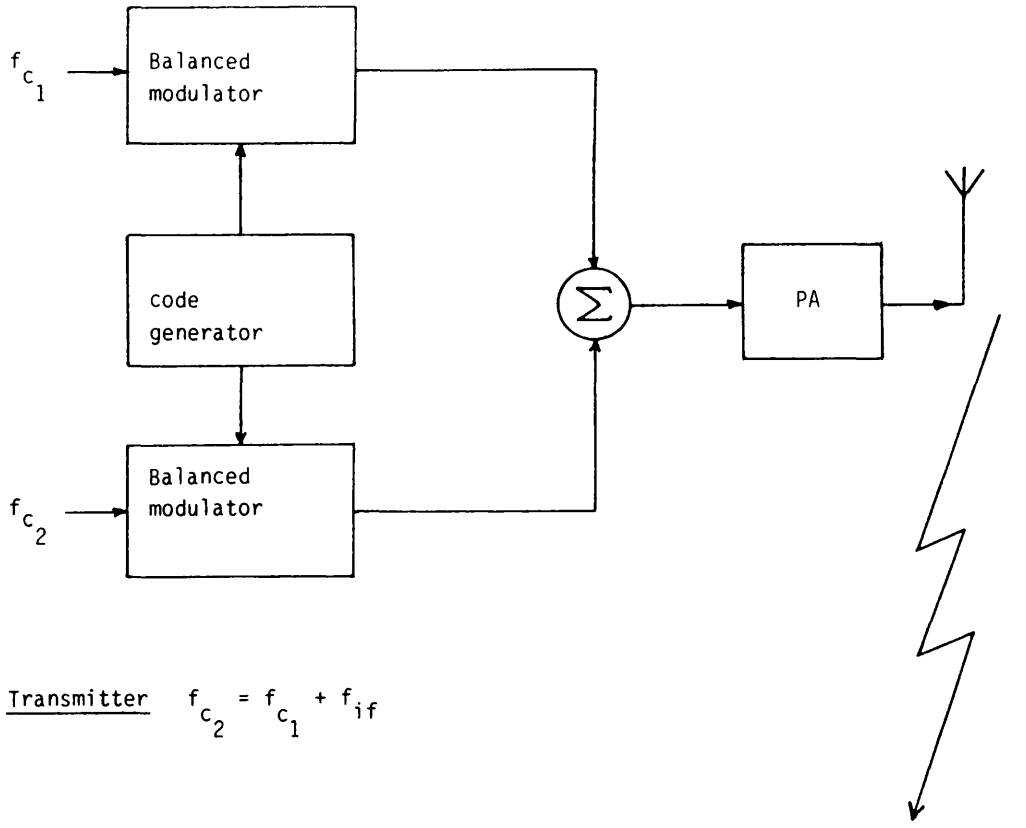
2.2.3 Transmitted Reference Method

This method may be used for initial synchronisation, tracking, or both when the receiver must be as simple as possible [4, 5]. The transmitter generates the code sequence and transmits it on a separate frequency to the receiver along with the signal to be demodulated. Their carrier frequencies are offset by an amount equal to the first IF in the receiver as shown in Figure 2.2.

This technique has the advantage of reducing the complexity of the receiver because there is no need for a code sequence generator and search or tracking circuit. However, there is also a disadvantage in the technique because of the noise or interference which might be introduced in both the reference and the desired signal channel during the transmission through the channel. This noise and interference causes errors at the correlator output of the receiver [1]. Of course, if the reference code is transmitted only to achieve rapid synchronisation acquisition with a subsequent switch to normal direct sequence demodulation, sub-systems, such as local sequence generator and tracking circuit must also still be included.

2.2.4 Universal Timing

Synchronisation between a fixed transmitter and receiver can be achieved when the time of the day is known to the transmitter and the receiver within a fraction of a second provided that the distance between them remains constant (to ensure that the delay due to propagation remains unchanged).



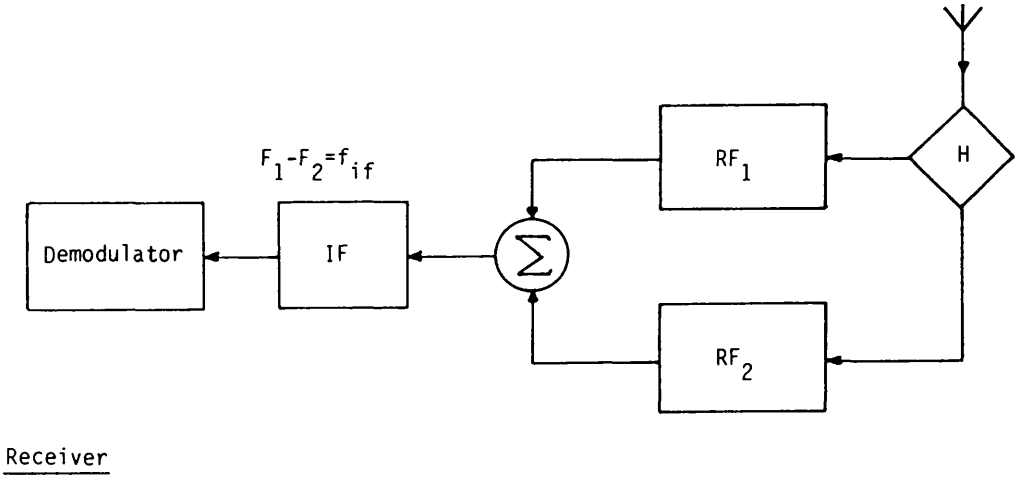


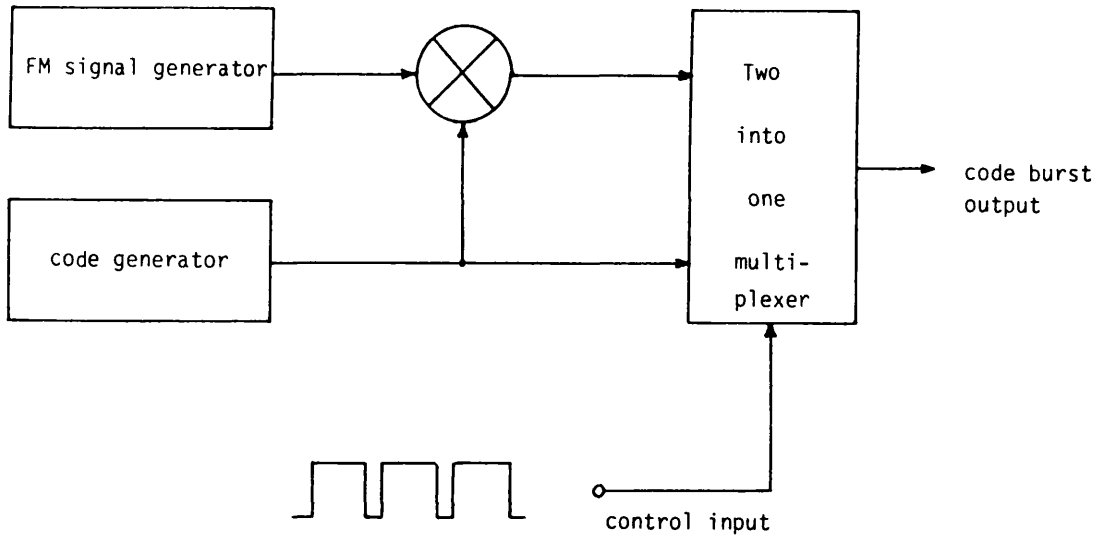
Figure 2.2. Transmitted reference synchronization method (direct sequence application)

So all codes used in the network could be set to a certain state (for example, all ones) derived from a certain time and that state renewed at regular time intervals or for every new transmission. However, some form of search and track circuit is still necessary due to the variation in time and propagation and Doppler shift.

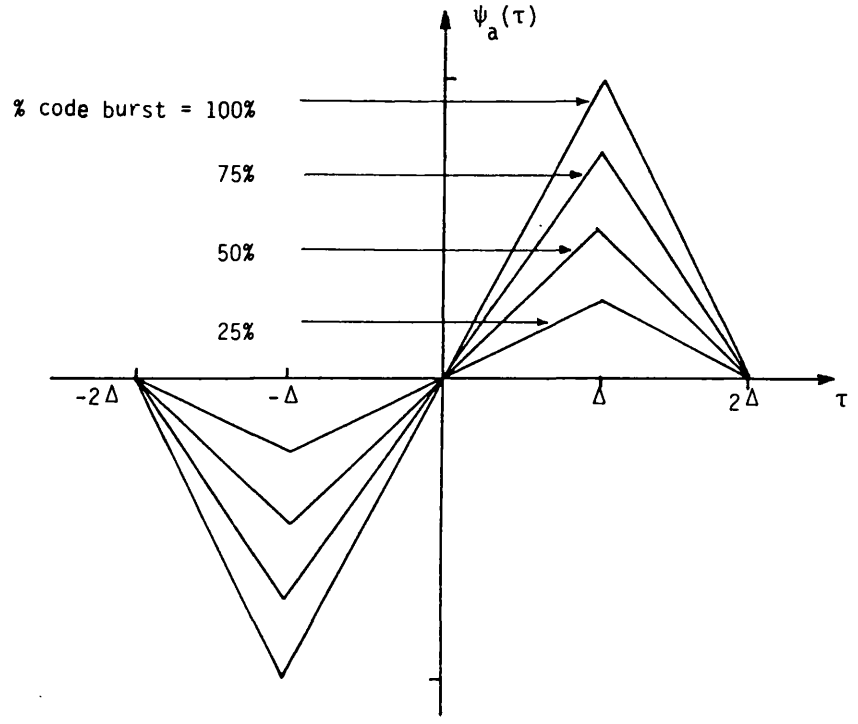
The universal timing method has been used principally in satellite communications in which ephemeris data provides accurate distance information and ambiguity can be reduced to the point at which search processes may be minimised. If the frequency sources and position estimation methods are very accurate, the mobile user can also use universal timing methods for synchronisation and tracking. Today's technology can provide this accuracy without too much difficulty using Caesiam clocks.

2.2.5 Burst Synchronisation

Instead of the method mentioned in the previous section, it is possible to transmit a short high speed message to inform the spread spectrum receiver of the code sequence and carrier synchronisation. Once synchronisation has been achieved, the code burst is switched off and tracking code phase takes place as normal [6]. Figure 2.3 illustrates this technique. Depending upon the logical state of the control input the multiplexer either passes sequence modulated data or pure sequence to the RF modulation section for transmission. The period of the code-burst, or in other words the duty cycle, is dependent upon the mark-to-space ratio of the control signal input. An important feature is that the sequence runs continuously and therefore no loss of phase is encountered during the bursts [7].



a) Block diagram



b) Effect of percentage code Burst on discriminator characteristic

Figure 2.3 Code Burst Generator.

The only interference signal which might break the communication is a very large amount of continuous radio frequency power to overcome the high peak power available to low duty cycle of the burst transmitter [1].

2.2.6 Sequential Estimation

It is possible to achieve synchronisation between the spread spectrum transmitter and receiver simply by inserting a certain number of bits of the code sequence (taken from the received signal) into the receiver's local code generator, and to start the code sequence of the receiver from that point. The frequency of the local clock generator must be very near to the frequency of the received signal, and a tracking circuit has to be added immediately to maintain synchronisation.

The RASE (Rapid Acquisition by Sequential Estimation) synchronisation technique developed by Ward [8], which is shown in Figure 2.4, has the advantage of rapid synchronisation in noiseless conditions or high input signal to noise ratio. This is because under these conditions the first n bits of the received sequence can be correctly identified at the first attempt. RASE, however, has the drawback that it is more vulnerable to interference signals than some other techniques. This is because the demodulator demodulates the received code without benefit of processing gain. Any noise increases the probability that **any one** of the n bits may be in error and this would load the wrong starting sequence into the generator. Thus, as the noise increases the probability of an error increases rapidly and the number of attempts at synchronisation also must increase. The longer the sequence, and hence n, the greater the

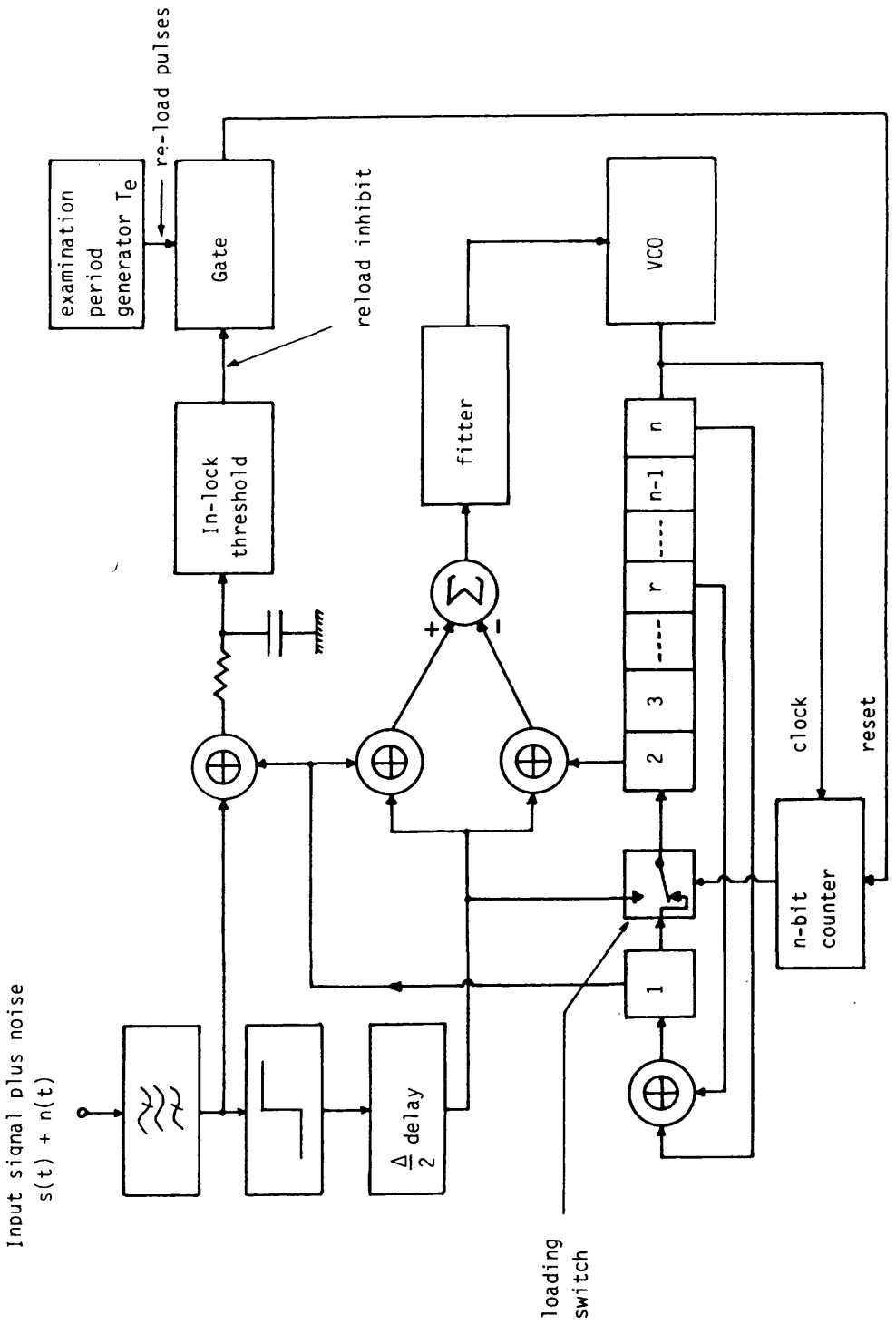


Figure 2.4. RASE system.

probability of an error in estimating the sequence (cf. sliding correlator techniques, in which the converse is true). Hence the acquisition time increases as the input signal to noise ratio decreases. An average acquisition time, recorded by Ward [8] shows 90 ms at -6dB input SNR, 300 msec. at -10 dB input SNR, and 1 sec. at -12.5 dB SNR for a sequence of length $(2^{15}-1)$ clocked at a rate of 1.5MHz.

The RARASE (Rapid Acquisition by Recursion - Aided Sequential Estimation) technique proposed by Ward and Yiu [9] is an extension of RASE. The block diagram of a typical RARASE system for a five stages maximal sequence generator is shown in Figure 2.5. In this technique the known recursion relation of the pseudo noise signal is used to determine if a short estimate of the state of the received pseudo noise signal is probably correct or not. This is done by checking if the estimate loaded into the pseudo noise generator would produce the correct feedback bit, so as to continue to emulate the incoming sequence. Consequently, the system can decide whether an attempt should be made to track with its then present estimate or not. A change over switch at the input of the first shift register, which is controlled by the synchronisation-worthiness indicator, select either the estimate of the incoming sequence or the output from the pseudo noise feedback logic. So a high proportion of the incorrect initial state estimates can be discarded and the acquisition time can therefore be speeded up. The improvement obtained with the RARASE over that of RASE system has been calculated by Ward and Yiu [9] and is given by:

$$\frac{T_a \text{ RARASE}}{T_a \text{ RASE}} = [p^2 + 3\,(1-p)^2]^n \qquad 2.1$$

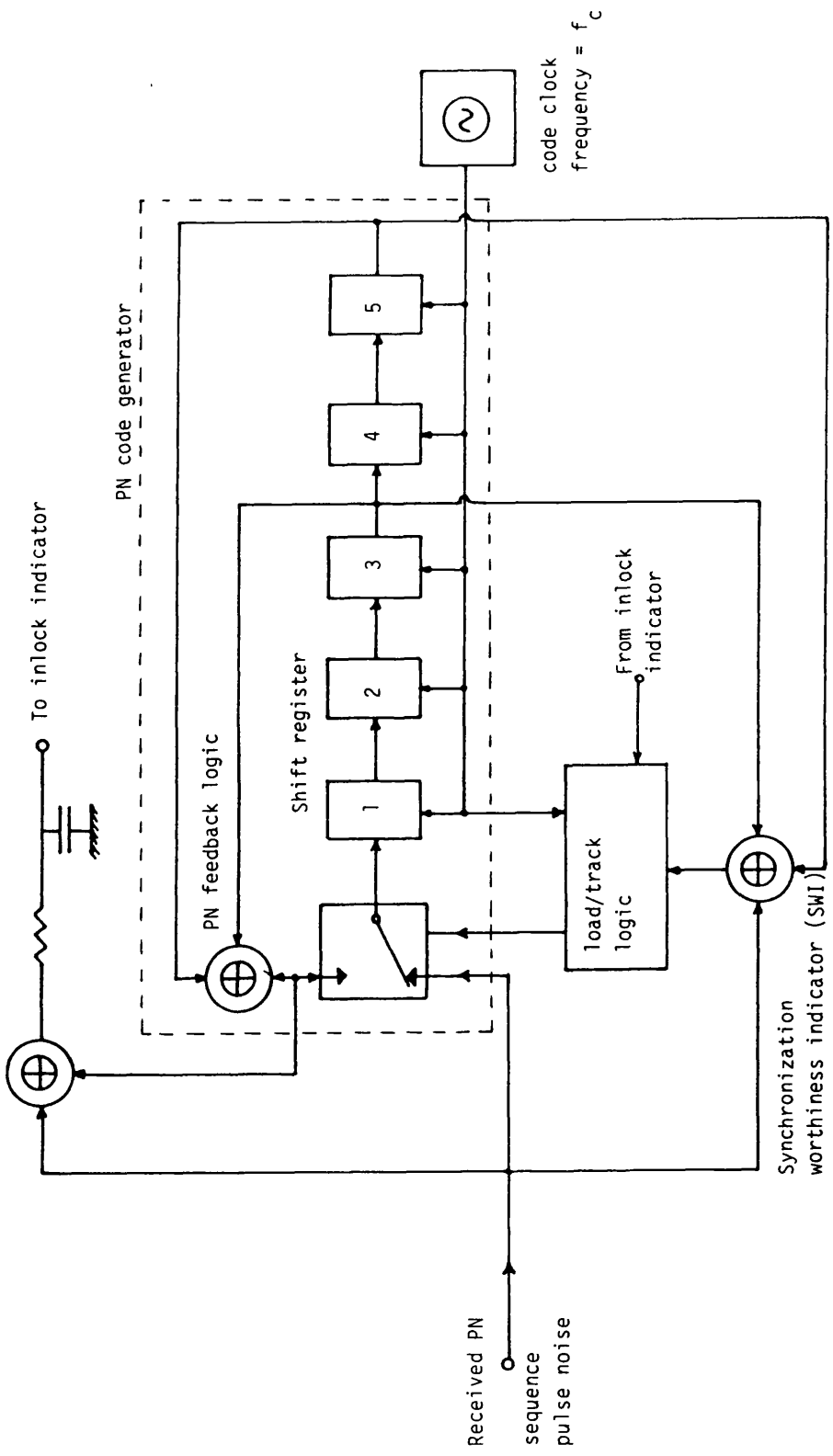


Figure 2.5. RARASE system

where p = the probability of a single bit of the estimate being correct.

n = the number of bits tested by recursion.

The search/lock strategy described above could be useful in designing a minimum acquisition time pseudo noise system which operates only in a moderate signal to noise ratio environment.

2.2.7 Special Coding for Synchronisation Acquisition

More rapid spread spectrum system lock-up could be achieved by using special codes, specifically designed for synchronisation.

The JPL component code [10, 11] discussed in Chapter 1 is made up of shorter codes, each of length (2^P-1) bits, combined together (by modulo-2 sum) to give a long code of length $(2^m-1).(2^n-1)$ ... (2^r-1), where $m \neq n \neq r$. This code has a special correlation property, which is different from the maximal linear sequences in that the latter has only one point of autocorrelation. The component codes, on the other hand, have one more correlation possibility than there are components in the code (i.e. if a code is made up of three component subcodes, there are four autocorrelation points associated with the overall code). Moreover, all but one of these autocorrelation levels are associated only (and separately) with the individual codes making up the composite code. The highest correlation level corresponds to total composite code synchronisation. The receiver first cross-correlates one of the component codes with the received code sequences, a partial correlation occurs at the point of synchronisation when the two component sequences are synchronised. Then the second component

sequence is initiated which increases the partial correlation level. This process continues until the two overall codes are synchronised. The advantage of this technique is that it provides for rapid synchronisation without the use of a preamble or anything other than the code itself. A maximal sequence of say $(2^{24}-1)$ bits needs much longer to synchronise than a JPL component code of the same length whose component codes are $2^7-1=127$, $2^8-1=225$, and $2^9-1=511$, since the search process over these individual lengths needs only to search over only 127 + 225 + 511 = 893 bits. As with all other synchronisation techniques described so far, with the exception of the serial search, the penalty paid for rapid acquisition is the reduction of interference rejection and the reduced ranging capability when all code components are not synchronised.

Anderson (12) also defined a set of codes with well defined correlation properties that may be employed for synchronisation. Short preamble codes might also be considered special codes, but in general, the only difference between them and the code sequences used after acquisition is length.

Another special code for synchronisation is the composite sequence proposed by Beale and Tozer [13] which is also known as the Kronecker sequence by Sarwate and Stark [14]. The construction of this composite sequence was given in the previous chapter and it achieves rapid sychronisation in a manner similar to the JPL codes. A full detail of this technique will be given in Chapter Five.

2.2.8 Synchronisation by Microprocessor Control System

The recent advancements in microprocessor and minicomputer design technology has enabled them to be used in many fields including communication systems. The objective of using a microprocessor device is to carry out as much of the synchronisation and tracking process as possible in software. This can also be extended to generate the local code sequence keeping the hardware as little as possible. Of course this mainly depends on the speed of the microprocessor used and the clock frequency of the system under consideration.

Davies, Al-Najar, and Al-Rawas [15] have implemented a system using an F8 microprocessor, which has the advantage of low cost, easy interfacing, reasonable speed, and the availability of a software-compatible single-chip microcomputer. Figure 2.6 shows a block diagram of a low-data-rate spread spectrum system controlled by microprocessor. The microprocessor controls a voltage controlled oscillator and sequence generator and carries out the correlation processes needed for the acquisition and tracking modes. Switching between modes is achieved by changing an interrupt vector. The receiver operates in two alternative modes. While searching, the processor sends a constant voltage to the voltage controlled oscillator which causes a frequency offset between the local code frequency and the nominal frequency of the received signal, then it carries out the cross-correlation between the two sequences. When the threshold is exceeded, it is assumed that the two sequences are aligned, and the processor immediately alters the voltage sent to the voltage controlled oscillator and this changes the interrupt vector

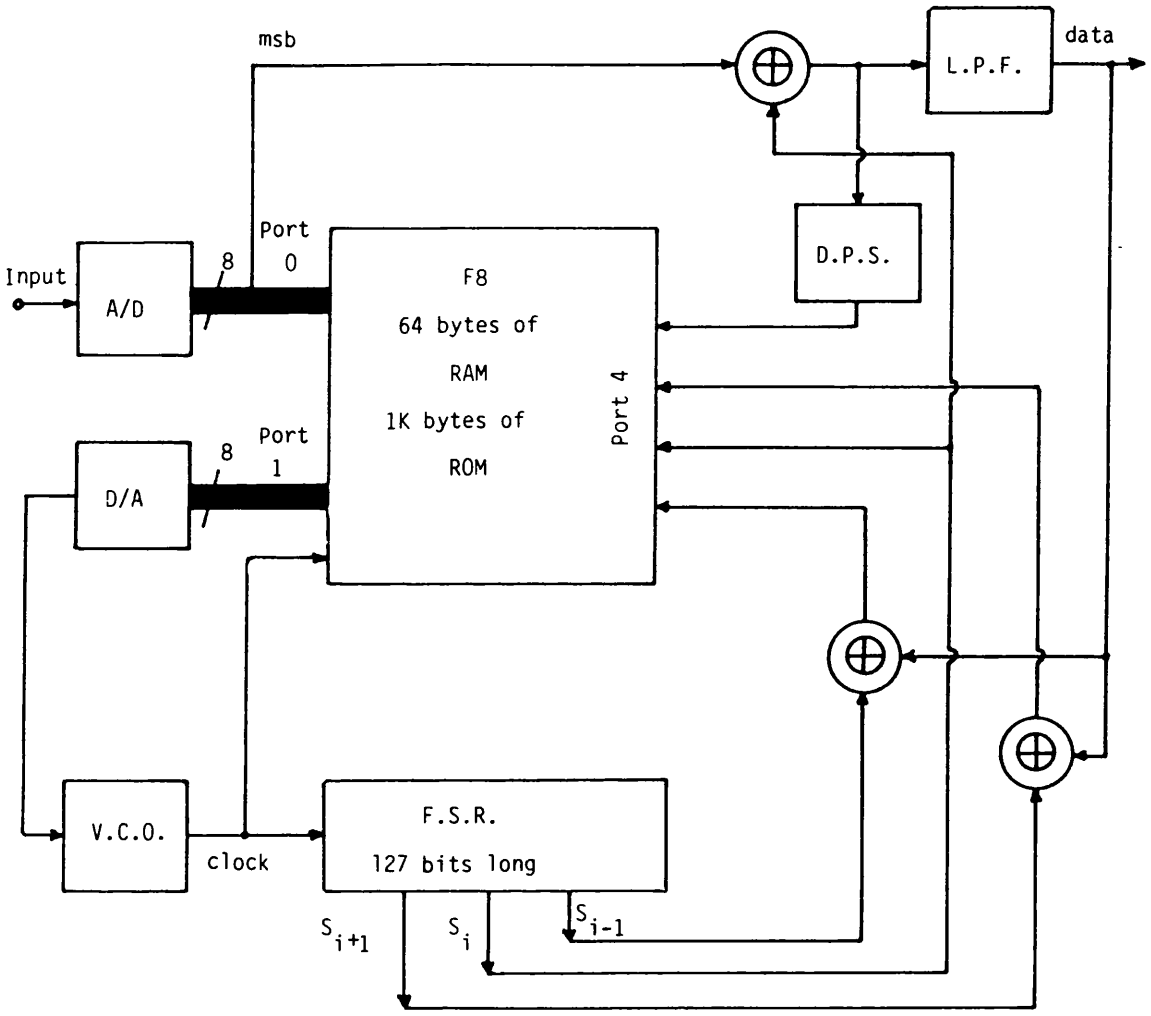


Figure 2.6. Microprocessor Synchronizer Technique.

to that for tracking. The error signal produced by the tracking process is then added to the voltage sent to the voltage controlled oscillator, so maintaining the alignment.

A system such as this has the advantage of being able to define the search procedure and relevant parameters by software and as a result to be adapted in a relevant manner, such as the prevailing signal to noise ratio at the input to the detector changes or if the local code sequence generator is generated by software for example a different transmitted signal can be easily received just by changing the software. The disadvantage of this technique is that only low-data-rate spread spectrum systems can be implemented due to the speed limitation of the existing microprocessors.

2.2.9 Techniques Employing Tapped Delay Lines

In all synchronisation techniques discussed above, the received spread spectrum signal was correlated with a receiver-generated replica of the spreading code. The output of this correlator was then processed to indicate whether or not synchronisation had occurred so that tracking could take place. This type of correlator was called an active correlator. Several other techniques use the so called passive correlator rather than the active correlator. The choice between an active or passive correlator implementation is largely dictated by the frequency at which it is intended to operate, the spread bandwidth, or equivalently the code chip rate, the data bit duration and the interference rejection requirement. However, in many cases the implementation of suitable matched filter is technologically difficult, costly and limited to certain applications. The fundamental difference between an active

correlator and a passive correlator lies in the form of the reference code signal generated in the receiver.

A matched filter generates a time reversed replica of its desired input signal when its input is an impulse. The transfer function of a matched filter is the complex conjugate of the signal to which it is matched [16]. The output of y(t) of any filter is the convolution of its input x(t) and its impulse response h(t), that is

$$y(t) = \int_{o}^{t} x(\tau)h(t-\tau)d\tau \qquad 2.2$$

where the filter is assumed to be causal and the input is assumed to begin at t=0.

In the case of spread spectrum system where the input to the matched filter is a baseband signal and the filter impulse response is a time reversed element of the receiver despreading code, the matched filter continuously correlates the received signal with this element of the spreading signal and generates a maximum output when it receives the corresponding element of the received spreading signal. This output can be sensed and used to start the receiver code generator at the appropriate phase, and synchronisation will be accomplished. This acquisition strategy is called matched filter synchronisation [2]. A convenient method of generating a matched filter for spread spectrum applications is to use a tapped delay line in a non-recursive (finite impulse response) configuration to achieve the required impulse response.

Figure 2.7 illustrates a delay line matched filter made up of 7 delay elements that could recognise a particular code sequence provided that the delay time of each delay element is equal to the expected period of the bit rate of the input sequence. When the

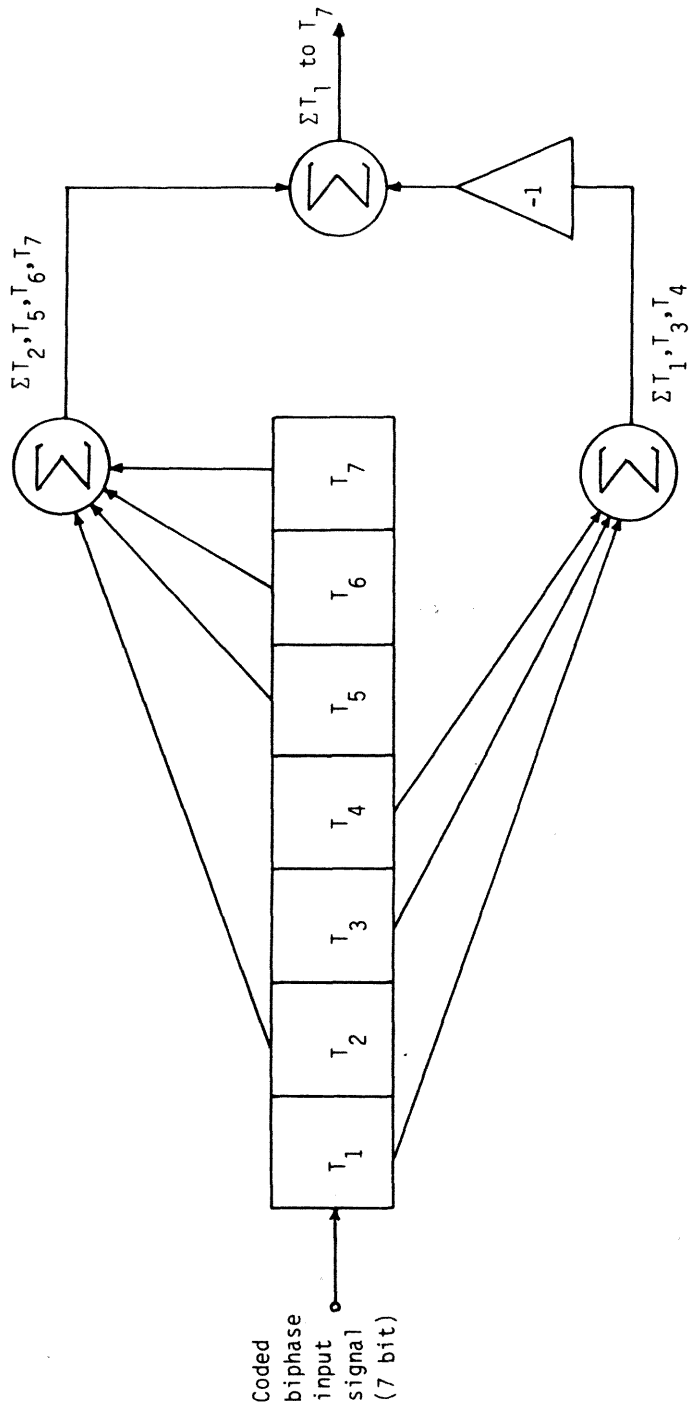


Figure 2.7. Delay line matched filter.

delay line element exactly matches an input signal, the signal summation is perfect. If, however, the code bit rate does not match the delay line, only partial correlatiton between delay line outputs occurs. Therefore a compromise is needed between a low threshold which results in increasing the probability of false detection, and too high a threshold which in turn reduces the probability of successful detection of synchronisation [1].

In practice, the tapped delay line may be a surface acoustic wave (SAW) device based on an analog device utilising Rayleigh wave propagation on lithium niobate ($LiNbO_3$) or quartz crystals. Convolvers having a bandwidth of 50 MHz with time bandwidth product (TB) product of $\Delta\tau\Delta f \approx 1000$, where $\Delta\tau$ is the differential time delay and Δf is the filter bandwidth, have been built [17-20]. The required process gain or the time-bandwidth product determines the complexity of the matched filters. Charge-coupled devices (CCD) previously discussed are more complicated than the surface acoustic wave devices and they are less used in synchronisation of spread spectrum systems.

In noise free conditions, initial code acquisition of a direct sequence spread spectrum receiver using a passive correlator may occur much more rapidly than when using an active correlator [31], because the time delay and signal storage capability allows integration over a code sequence length immediately the complete sequence has been loaded into the CCD or SAW devices. This advantage of a matched filter becomes less pronounced when noise and interference is taken into account. Pandit [22] has demonstrated that the mean synchronisation delay for an active correlator increases more slowly than for a matched filter, as the received

signal to noise ratio is decreased. Experimental results described by Pandit [22] for SAW matched filters, matched to 255-bits sequence, show that the mean synchronisation delay can increase by a factor of 10 for 3dB reduction in received signal to noise ratio (from -14 to -17 dB in this case). Nevertheless, extrapolating Pandit's results, it appears that a matched filter can achieve faster synchronisation than a correlator for received signals to noise ratios above about -20dB when the sequence length is, L=1023, bits.

2.3 TRACKING

Once synchronisation has been achieved, it is immediately necessary to control the clock of the code sequence so that the received signal and the local code sequence maintain synchronisation during operation of the communication link. This is usually done by means of a closed loop circuit called a tracking loop which employs feedback to reduce any errors to a value that is as small as possible, so that the codes remain matched to within a small fraction of a clock period. Three forms of the tracking loop are available for doing this:

a) Delay lock tracking loop.

b) Tau-Dither tracking loop.

c) Coherent carrier tracking loop.

Convolvers discussed in Chapter One can also be used as a tracking technique in spread spectrum systems.

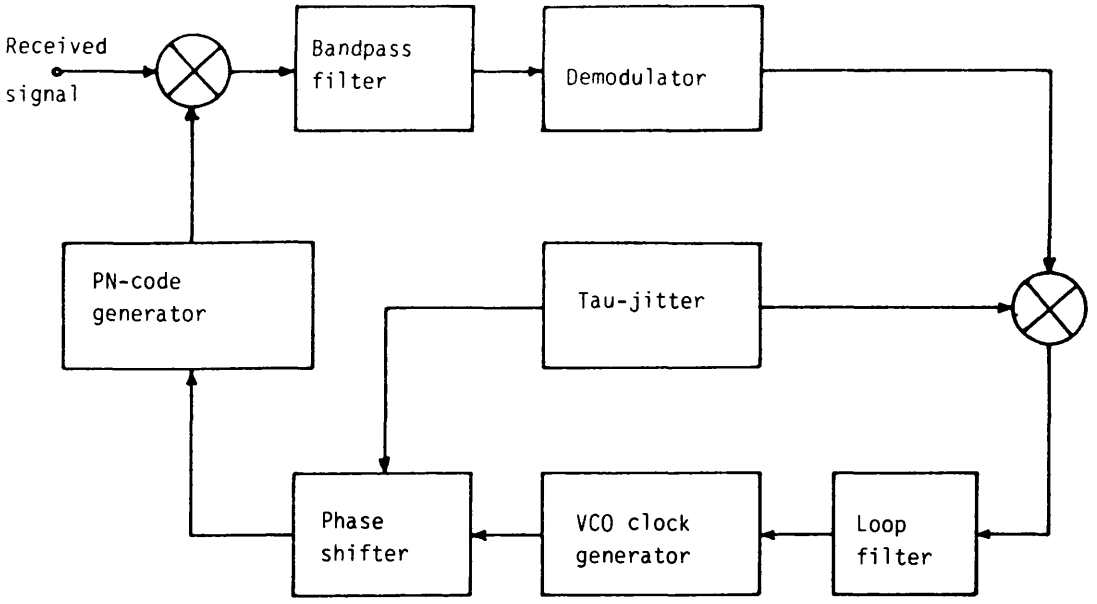
The delay lock tracking loop is considered to be the most important technique and most commonly used in spread spectrum receiver. This technique will not be discussed in this chapter, but

in detail in the following chapters, as it provides the basis for the synchronisation of the communication system under investigation.

2.3.1 Tau-Dither Tracking Loop

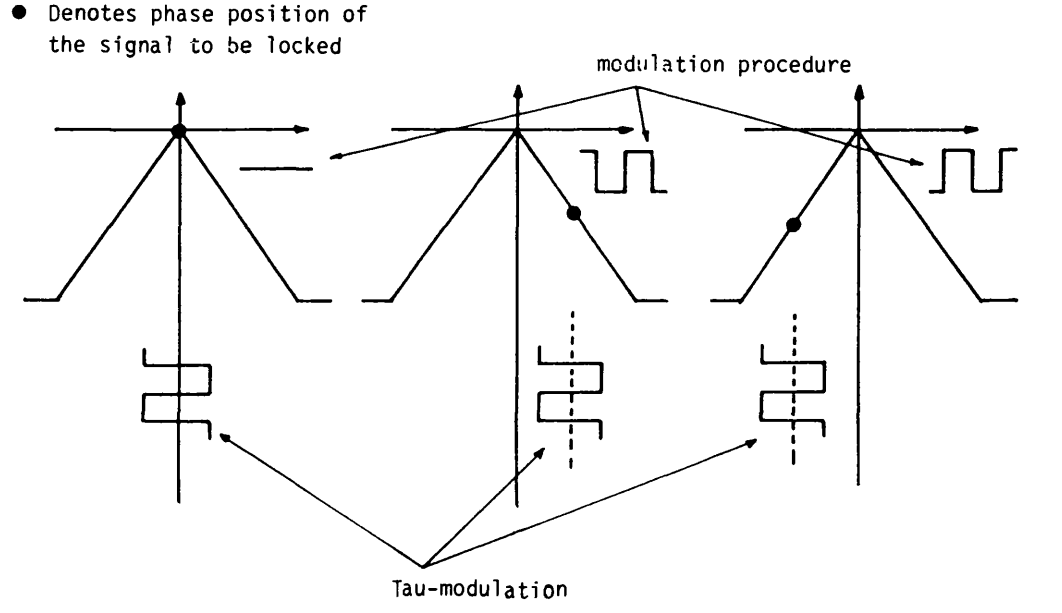
Tau-Dither tracking is an error signal generating method similar to those used in some servo systems for position sensing and correction.

Tau-Dither clock tracking in spread spectrum systems makes use of the triangular code correlation function possessed by random and maximal length binary codes. The idea is to cause the code phase of a locally generated replica sequence to remain as close as possible to a received code phase so that the timing of the two codes will remain essentially at the peak of correlation. The way this is done is to degrade the correlation deliberately by a known amount, observe the effect, and employ the information gained to improve the degree of correlation. A Tau-Dither tracking loop is sometimes called a Tau-jitter, and in fact, is very similar to the delay lock tracking loop [1]. The received signal is correlated with an early and late version of the locally generated pseudo noise code. Unlike the delay lock loop where two correlators are used, the correlation in Tau-Dither loop is done by a single correlator on an alternating basis. Figure 2.8 shows a typical Tau-Dither clock-tracking loop. The pseudo noise code generator is driven by a clock signal whose phase is "dithered" back and forth in accordance with the binary signal. This eliminates the necessity of ensuring identical transfer function in the two arms of a normal double correlator. The degree of correlation between the received and local codes changes according to the phase dither, and this causes a shift in the amplitude of the



a) Block diagram

b) Typical tracking signals



i) in phase ii) phase retarded iii) phase advanced

Figure 2.8. Tau-Dither system.

signal input to the demodulator. As the clock phase is shifted back and forth, the signal is amplitude modulated at the phase shifting rate. This signal determines the necessary error signal, so as to reduce the tracking error that exists between the two sequences. The information demodulator, usually for phase shift keying or some other form of angle modulation, is not affected by a small amount of amplitude changes, because of the orthogonality of angle-modulated and amplitude-modulated signals.

The main advantage of this technique is that there are some economies of implementation which compare with the delay tracking system. Because of its relative implementation simplicity, the Tau-Dither loop has been recommended for pseudo noise code tracking in TDRSS (Tracking and Data Relay Satellite System) to shuttle Ku-band communication link [23].

The disadvantage of this system is that when synchronisation occurs, the correlator is never working at the peak of its correlation characteristic. The two operating positions, advanced and retarded from the peak is defined by the tau-modulation, always hold the sequences at the position slightly offset from the correlation peak and therefore the output signal to noise ratio is never at its maximum. Hartmann [24], has shown that the signal to noise performance of the Tau dither loop is about 3 dB worse than the delay lock loop. However, the Double-Dither tracking loop proposed by Hopkins [25], has the same noise performance as the delay lock loop. It also solves the gain-imbalance problem of the delay lock loop. The price paid for simultaneously achieving those two points is increased hardware complexity, as shown in Figure 2.9.

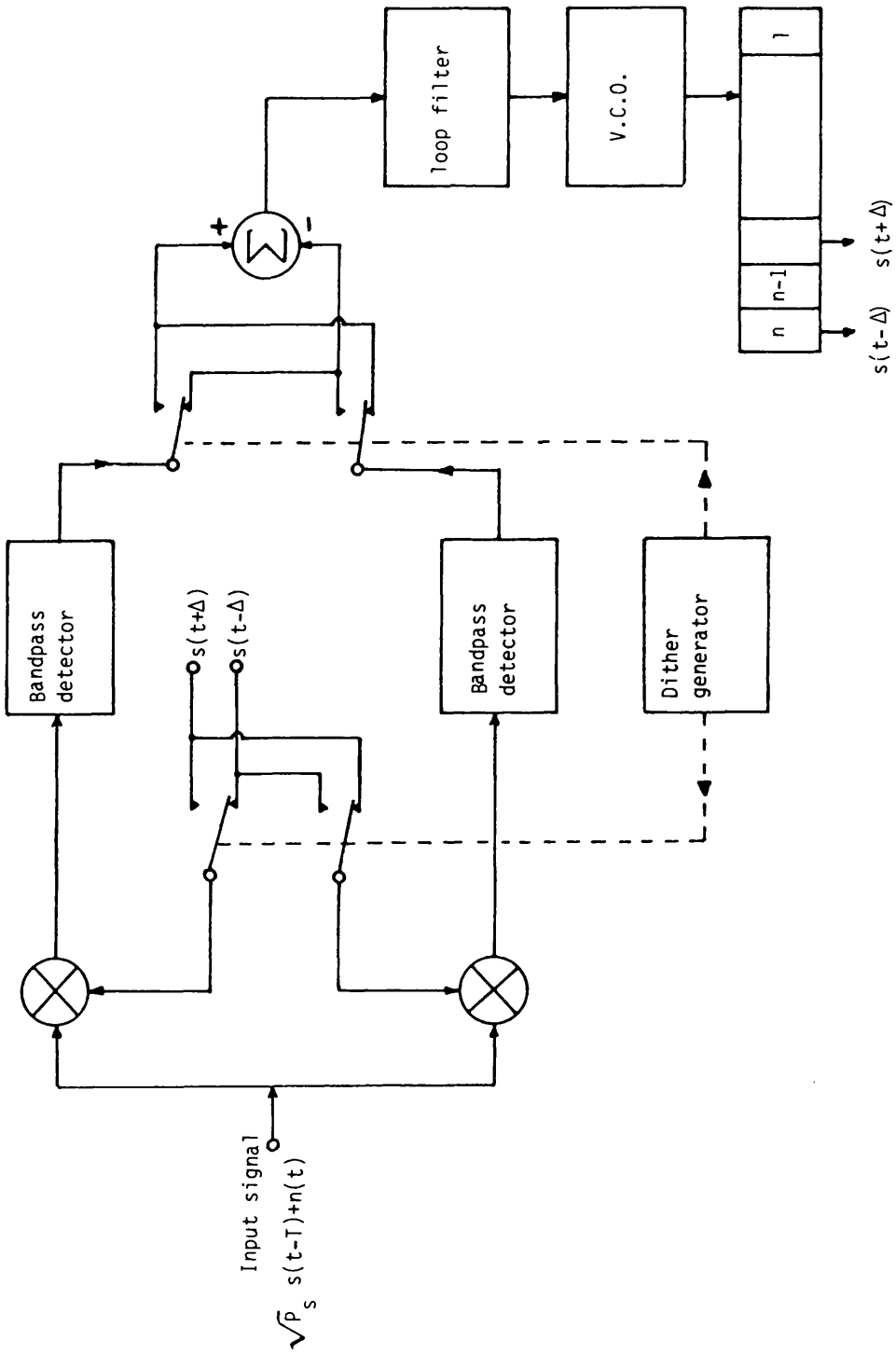


Figure 2.9. Double Dither Loop.

Nevertheless, it has an improved performance compared to the Tau-Dither loop.

2.3.2 Coherent Carrier Tracking Loop

In carrier coherent systems the mechanism used is just what the name implies. In other words, the code sequence clock rate is designed to be a submultiple of the carrier frequency or both carrier and clock are derived from the same source. Common sources must be used in the transmitter and receiver (i.e. each must have common code rate and carrier sources - not implying that both transmitter and receiver have the same source). When the modulation rate and carrier frequencies are coherently related, tracking one will also provide for the other; for instance, consider a transmitter in which a 50 Mbps code sequence direct sequence modulates a 500 MHz RF carrier. The carrier is derived as a 10 times multiple of the code clock. At the receiver, the local oscillators are also derived from the code clock, and the post correlation signal is translated down to a convenient demodulation frequency by mixing with these code-rate-related oscillators. Thus, the transmitter's 50 Mbps code clock rate is precisely related to the carrier signal seen at the receiver's demodulator, and a single phase lock loop demodulator can be used to track both code clock and carrier frequency shifts. A simple ± 1 bit correlation search is sufficient to satisfy this difficulty and once the proper phase is chosen only the frequency needs to be tracked [1]. A carrier coherent tracking system is illustrated in Figure 2.10. The use of this type of system is limited however, in that the transmitter from which it receives signals must have a code clock rate and carrier phase coherence for the receiver to operate.

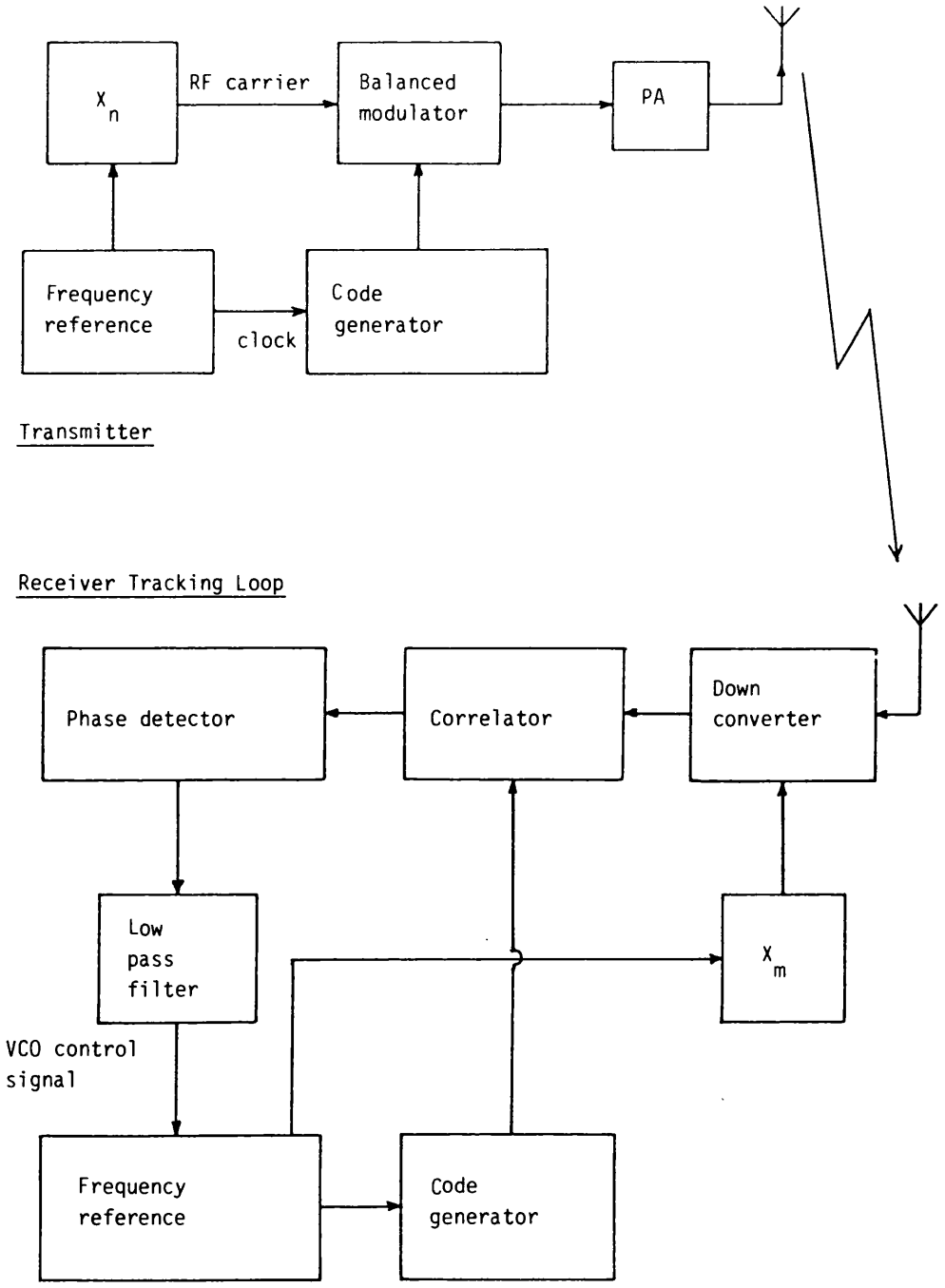


Figure 2.10. Carrier-lock tracking system.

Otherwise unrelated frequency drifts between clock rate and RF carrier would cause the receiver to lose lock.

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CHAPTER THREE

DEVELOPMENT OF AN IMPROVED DELAY LOCK LOOP FOR USE IN SPREAD-SPECTRUM SYSTEMS

3.1 INTRODUCTION

The most important techniques for initial synchronisation and tracking of pseudo-noise sequences in spread-spectrum systems have been discussed briefly in Chapter 2, together with their advantages, disadvantages and current performance limitations. In some systems initial acquisition of phase lock between the transmitted and locally generated PN sequences is a two stage process using either an active (or sliding) correlator [1], a matched filter [2,3] or a convolver [4] to provide coarse synchronisation to within ± 1 bit. Fine synchronisation and subsequent phase tracking may then be accomplished using either a delay lock loop (DLL) [5] or the tau dither loop [6]. However, both types of loop may be used to acquire initial synchronisation as well as track the delay error between sequences by performing a simple serial search of all the sequence epochs. In spread-spectrum systems used for timing and ranging this latter approach is most certainly the one which would be used. However, in multiple access CDMA communications systems rapid synchronisation is of vital importance, and where system complexity is not a prime consideration use of a matched filter, or correlator with an appropriate search/lock strategy [7,8] such as RASE or RARASE, would be used to achieve a rapid coarse synchronisation, even when the transmitted PN sequence is embedded in noise. Synchronisation by a microprocessor [9] is also used for low data rate systems.

However, the use of a tracking loop to maintain phase synchronisation between the received and locally generated sequences when the phase of the transmitted sequence changes (due to Doppler shift, for example) is vital. Another example where a tracking loop would be needed is when a spread-spectrum system is used in a mobile application. These types of signal are subject to rapid shadow fading and multipath fading, and during a fade some loss of synchronisation may be expected. In order to minimise data errors in the transmitted message rapid resynchronisation is necessary. This requires a phase tracking loop which is fast, yet has a narrow noise bandwidth to minimise in-lock phase jitter when synchronisation has been achieved. Immunity from spurious multi-path signals should also be a desirable feature of the loop.

The delay lock loop has found widespread use in both CDMA spread-spectrum systems and ranging and timing systems based on PN techniques. As outlined in Chapter 2, the delay lock loop has several advantages over its chief rival the tau dither loop, a principal reason being that in-lock jitter can be made smaller in the case of the DLL. In this chapter novel methods for improving the acquisition and tracking performance of the DLL, without compromising the in-lock jitter performance, are considered in detail. The modifications are considered for both the case of a simple ranging application, where the PN sequence is not modulated by digital data, and the case of a CDMA spread-spectrum system where the PN sequence is modulated by digital data. This latter system requires special techniques within the loop. As shown in Chapter 1, the synchronisation circuit is generally at an I.F. frequency (which may be modelled by a base band model) or directly at baseband. For this

reason most of the work in this chapter considers a baseband model of the loop and all experiments are carried out on a baseband loop.

The discriminator characteristics formed by the DLL phase detector are particularly important in determining the acquisition and in-lock performance of the loop. In this chapter the effect of the width and polarity of the discriminator characteristics on the acquisition of lock are considered. The effect of damping ratio is also considered.

3.2 THE DELAY LOCK LOOP

The delay lock loop was first proposed by Spilker and Magill [5] in 1961 as "The delay lock discriminator - an optimum tracking device" specifically for tracking maximal length PN sequences in ranging systems. It is now arguable whether the structure they proposed can be considered in any way "optimum", nevertheless it is a very useful circuit. Many, slightly different, variants of the loop now exist. Most of these variants concern the methods by which data modulation is removed from the received PN sequence in a spread-spectrum communication system. The following types of DLL have been used in ranging and communication systems.

i) DLL for synchronising unmodulated binary PN sequences.

ii) DLL for time gated PN sequences.

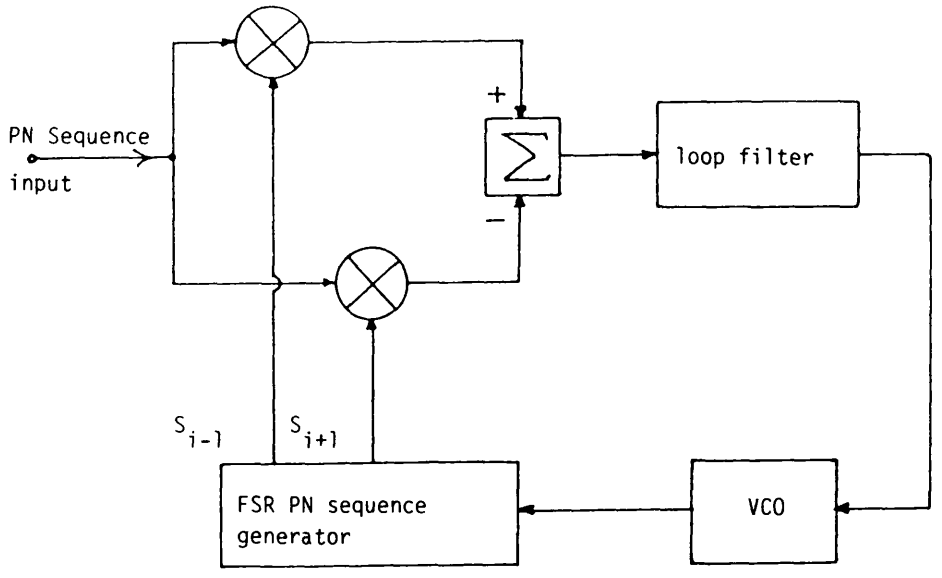
iii) DLL for synchronising data modulated binary PN sequences using: duplicated loops, envelope detectors and square law devices.

iv) Coherent carrier DLLs.

Detailed descriptions of these loops can be found in references [10-17]. In principle all these loop configurations use the basic loop proposed by Spilker and Magill, and it is this loop which will be considered in greater detail, together with a description of how the loop may be modified to accommodate data modulated PN sequences.

The choice of PN sequence is particularly important in both multi-access and ranging systems, as detailed in Chapter 1. Both systems require sequences with "good" two level auto correlation performance and low values of cross-correlation when the wanted sequence is correlated with the other, similar length, PN sequences. Maximal length PN sequences have relatively good cross-correlation properties and a two level auto-correlation function, and have found widespread use.

Figure 3.1a shows a schematic diagram of a baseband model of the basic DLL used in a ranging system. The structure is similar to that of a phase locked loop, but the DLL has a more complex phase detector. Figure 3.1b shows a schematic diagram of the loop when used at an I.F. frequency. It is obvious that both baseband and I.F. loops are identical in operation. Considering the baseband model, the received maximal length PN sequence is separately correlated with "early" and "late" replica sequences generated locally within the loop by a feedback shift register sequence generator clocked by the voltage controlled oscillator (V.C.O.). The separate correlations between the maximal length PN sequences produce a triangular correlation function of width 2 bits and normalised peak amplitude 1. For the remaining L-2 bits the correlation has an amplitude only -1/L, where $L=2^n-1$ is the length of the maximal sequence and n



a) Baseband 2-Δ delay lock loop

b) Phase-coherent correlation delay lock loop

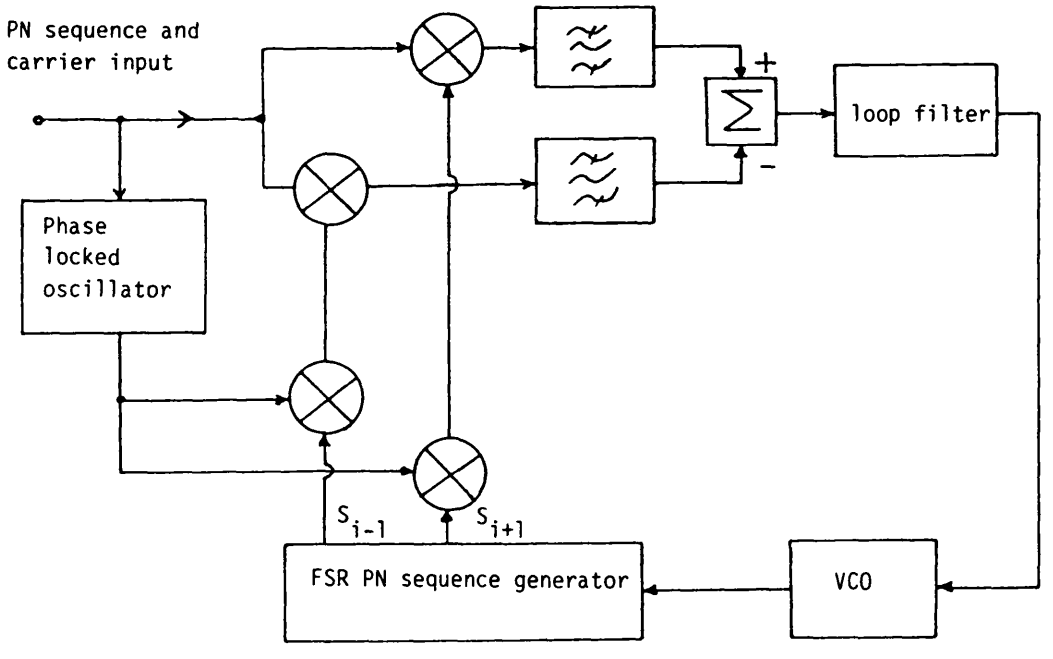


Figure 3.1 Delay lock loop structure

is the number of shift register stages used. This is shown in Figure 3.2. If the early and late sequences differ by 2 bits, the separate correlations differ by 2 bits. If these correlations are differenced the composite correlation function shown in Figure 3.3 (a) is formed. This forms the discriminator characteristic, or error curve, of the loop. These characteristics form the phase detector of the loop and the error signal fed to the VCO is proportional to the discriminator characteristic, which is dependent upon the relative delay between the two sequences. (Note that this error signal will be offset in voltage before being applied to the VCO and so the sense of the feedback is always negative).

For maximal length PN sequences the discriminator characteristics are 'N' shaped over a range of relative delay between the two sequences of only $\pm$ 2 bits. For all other values of delay the discriminator characteristic has a value of zero and no information regarding the relative phase between the codes is passed to the VCO. To overcome this problem it is necessary to ensure that in this condition the VCO idles at a slightly higher frequency than the clock frequency of the received PN sequence so that the loop can perform a serial search of all code epochs, until the codes next come into coarse synchronisation where-upon pull-in may be attempted by the loop.

If instead of using early and late sequences which are separated by 2Δ bits (forming what is termed the 2Δ DLL), they are separated by only 1 bit a different discriminator characteristic is formed, as shown in Figure 3.3b. A DLL with such a characteristic is termed a 1ΔDLL.

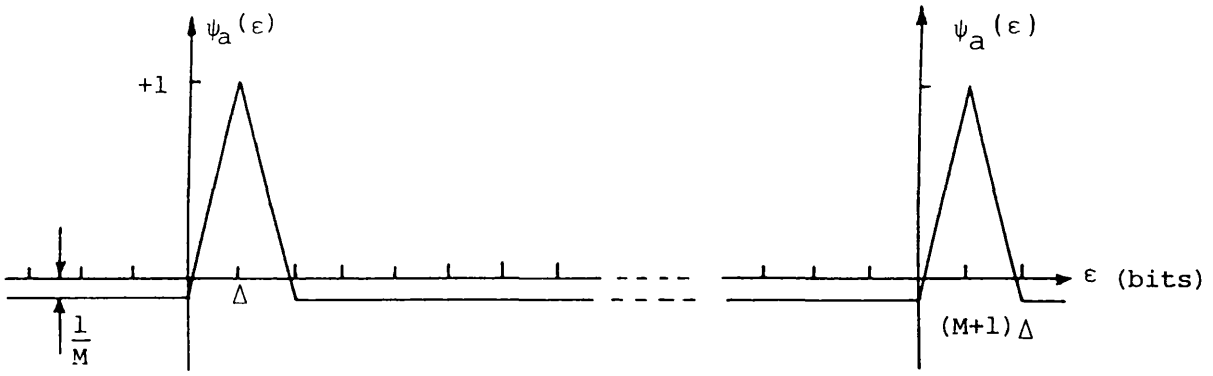
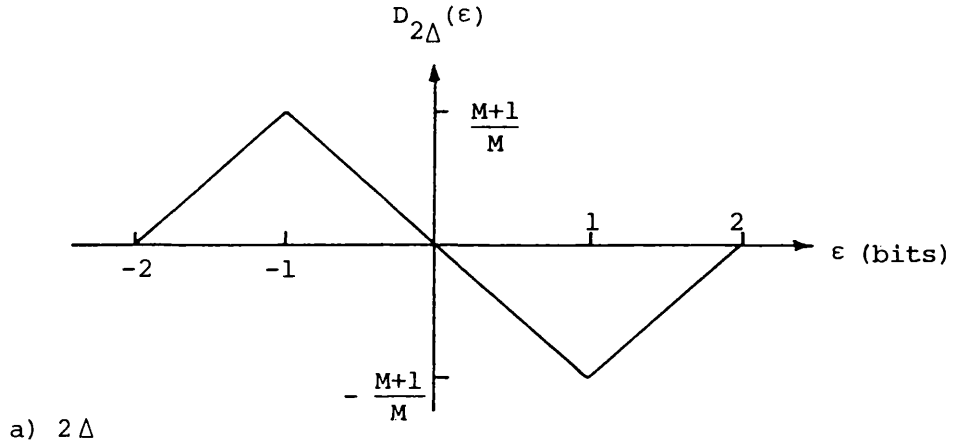


Figure 3.2. Auto-correlation function.



a) 2Δ

b) 1Δ

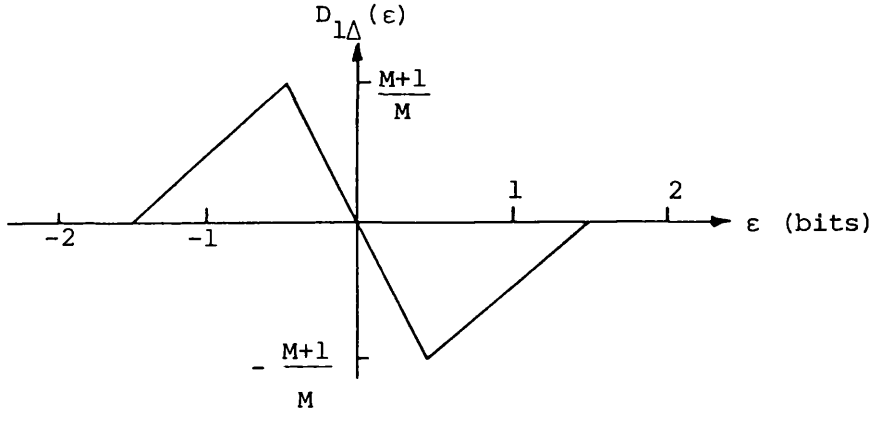
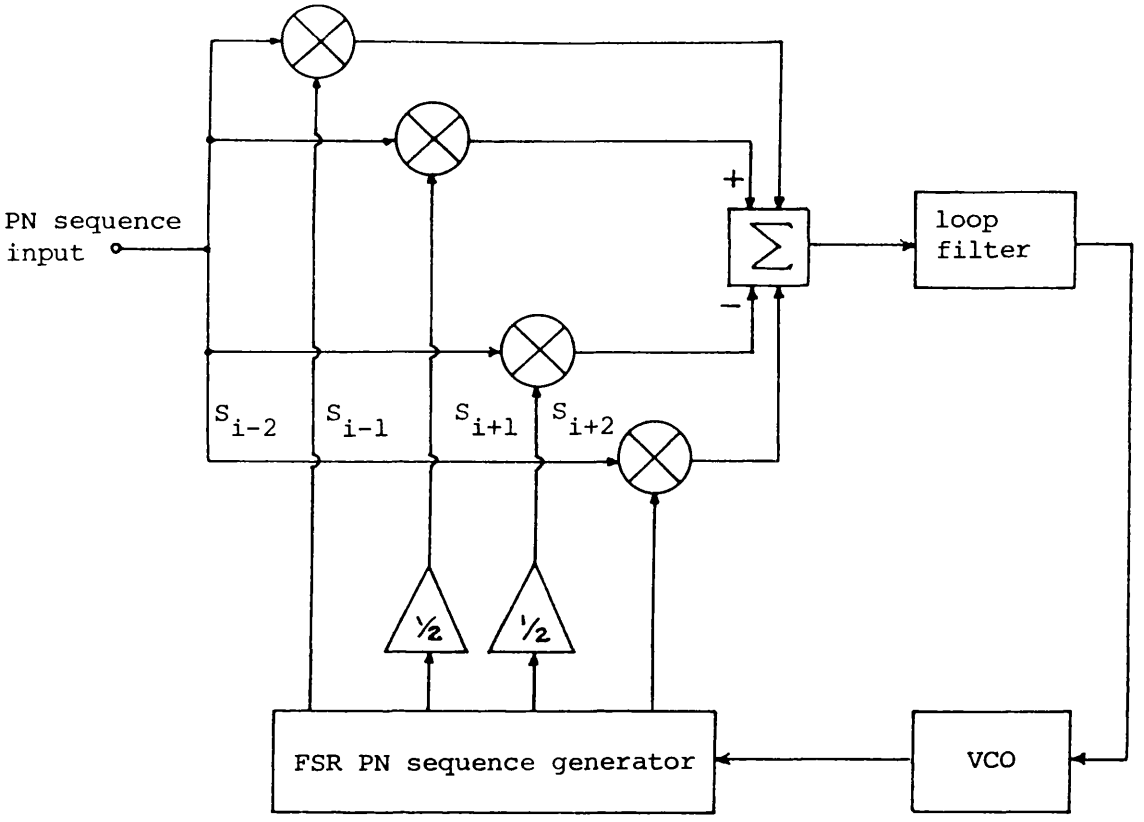


Figure 3.3. Discriminator characteristic or N-shaped error curve of 2Δ and 1Δ delay lock loop.

The correlations in the DLL are formed by the mixers in each arm and the single low pass filter constituting the loop filter. This is possible because the mixers and the difference amplifier are linear, and as the cut-off frequency of the loop filter is much lower than the clock frequency of the PN sequence it acts like an integrator. It is not necessary to perform true correlations in each arm of the loop prior to differencing, however, it should be realised that this places severe bandwidth requirements on the difference amplifier because it must not distort the mixed digital pulses prior to the differencing and filtering.

An advantage of the 2Δ DLL is that phase information is supplied over a greater range of delay error and it thus has the advantage of being able to maintain frequency lock over greater phase deviations which occur when the received PN sequence is corrupted by noise which frequency modulates the VCO. The 1Δ DLL effectively has a 3dB higher loop gain and this gives a slightly improved in-lock noise performance. However, far more serious, is the fact that the maximum rate at which the sequence epochs can be searched serially by the loop is half that of the 2Δ DLL.

Davis and Al-Rawas [18,19] have considered the advantages in broadening the discriminator characteristics beyond the 2Δ DLL characteristics. Although it might appear that this is at the expense of increased hardware complexity, since many early and late replica sequences are generated simultaneously by the feedback shift register sequence generator, the increased hardware is confined to an increase in the number of mixers, one per DLL arm, and several inverting scaling amplifiers. Figure 3.4 shows a block diagram of a standard



a)

b)

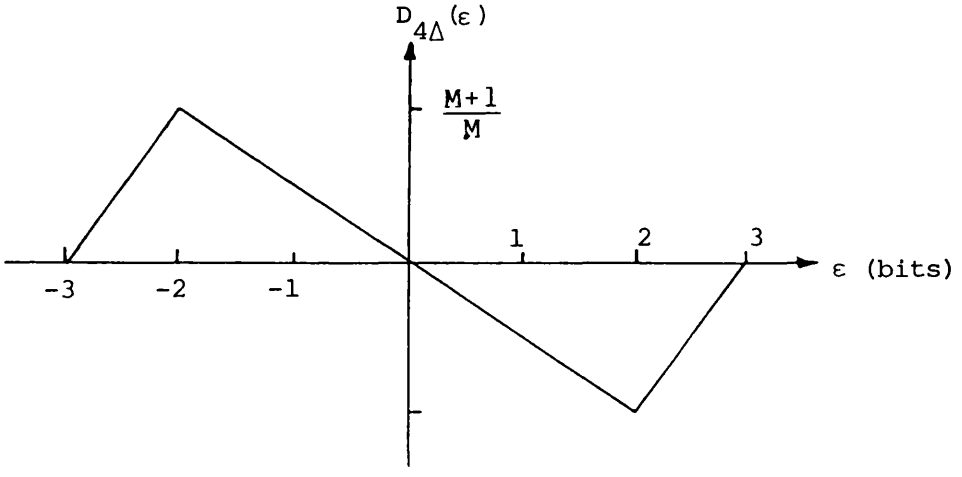


Figure 3.4. 4-Δ Delay lock loop

a) Schematic diagram

b) Discriminator characteristic

4Δ delay lock loop and its corresponding discriminator characteristic.

The widened 4Δ discriminator characteristic is obtained by correlating the received PN sequence with scalar weighted early and late sequences which are then arithmetically summed and filtered. The algorithm for determining the scalar weightings of each sequence is given in references [18, 19]. The effect of the width of the discriminator characteristics on the maximum search rate will be given in section 3.2.4 of this chapter.

3.2.1 The Delay Lock Loop Used in Data Modulated Systems

Sequence inversion keying is often used for data modulation [20]. In such a technique the phase of the transmitted PN sequence depends on the logic state of the data bit, such that the PN sequence is inverted when the data bit changes state. When the local replica sequence is correlated against the data modulated PN sequence the discriminator characteristic is inverted at the data rate. Even though the data rate is much lower than the chip rate of the PN sequence, it is still likely to be higher than the cut off frequency of the loop filter (because the DLL loop must be less prone to the effects of input noise than the data if the system is to operate reliably). Consequently the loop filter averages out the alternating value of the error signal, and the resulting signal fed to the VCO is zero.

R.B. Ward [20] has modified the delay lock loop to permit it to be used with sequence inversion keyed data modulation. This is shown in Figure 3.5. The loop correlator is duplicated, with each half of

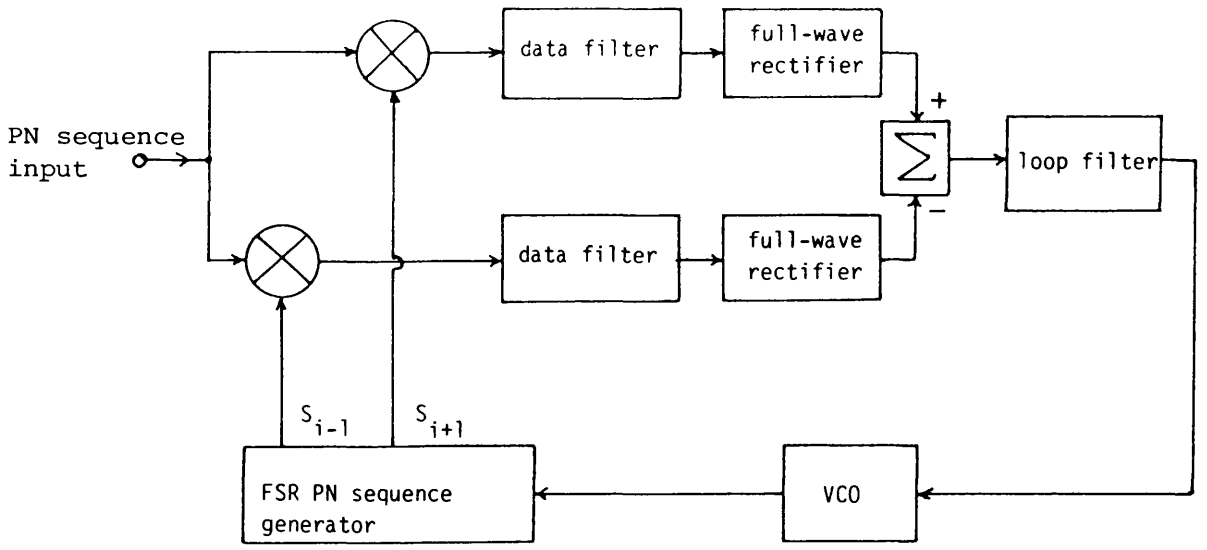


Figure 3.5. Delay lock loop for use with sequence inversion keying modulation.

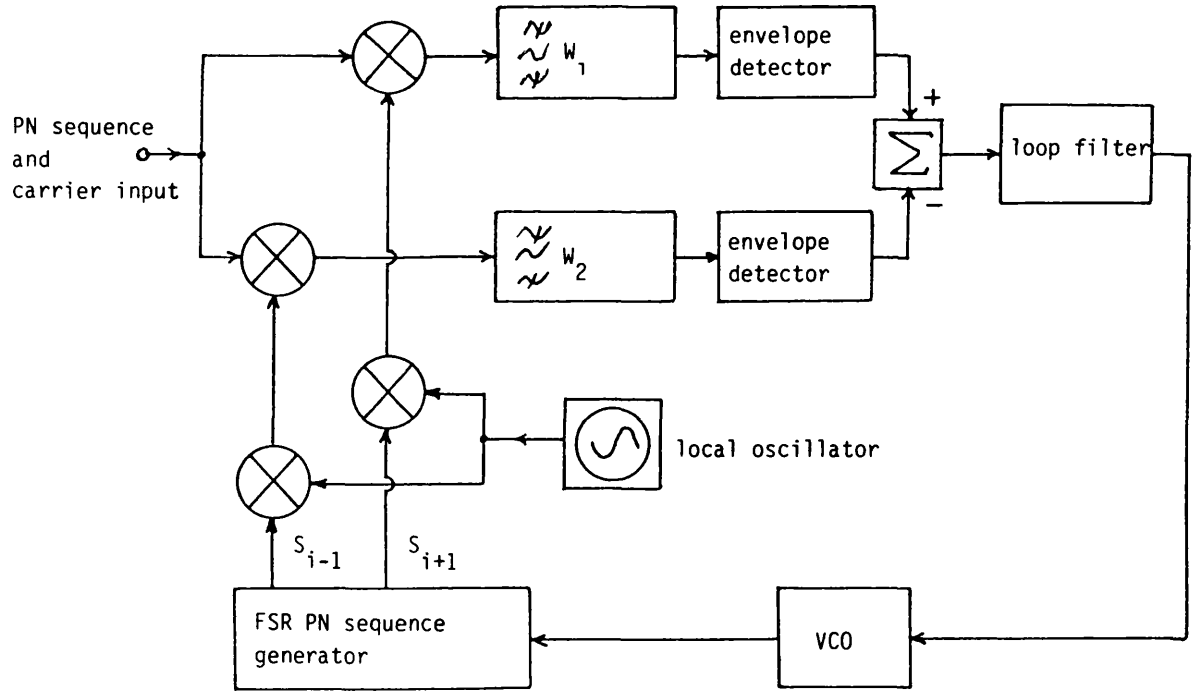


Figure 3.6. Envelope correlation delay lock loop.

the loop rectified, and the individual correlator outputs combined with an appropriate d.c. offset to the VCO to provide full wave rectification of the error signal. This ensures that the feedback is always negative, regardless of the data polarity. This technique requires two extra mixers, and may be considered somewhat extravagant.

A simpler technique for maintaining the polarity of the error signal to the VCO is shown in Figure 3.6. Here, it is simply necessary to put linear amplitude demodulators into each arm of the DLL. This also full wave rectifies the discriminator characteristic. Simple diode circuits and square law devices have been proposed to perform the a.m. demodulation, however, these non-linear methods distort the discriminator characteristics, as shown in figure 3.7 [14] and it will be seen that the DLL has a very low effective gain at the position of zero delay error. This, of course, seriously affects the ability of the loop to maintain very accurate phase synchronisation when in lock. A solution to this problem is to use the "synchronous" type of a.m detector shown in Figure 3.8. In this type of circuit the a.m. or double sideband modulated signal is fed to one input of a mixer, whilst the other input to the mixer is fed from a hard limited version of the signal. This type of detector is linear with a wide dynamic range of 30-50dB (depending upon the mixer used). It will be seen however, that although the structure of the loop is similar to a standard DLL the number of mixers required is similar to that required by Ward's circuit. Ormondroyd and Shipton [14] have proposed a somewhat different approach using the technique of data feedback. The technique is illustrated in Figure 3.9. A data estimate from the data correlator is fed back to, and mixed with

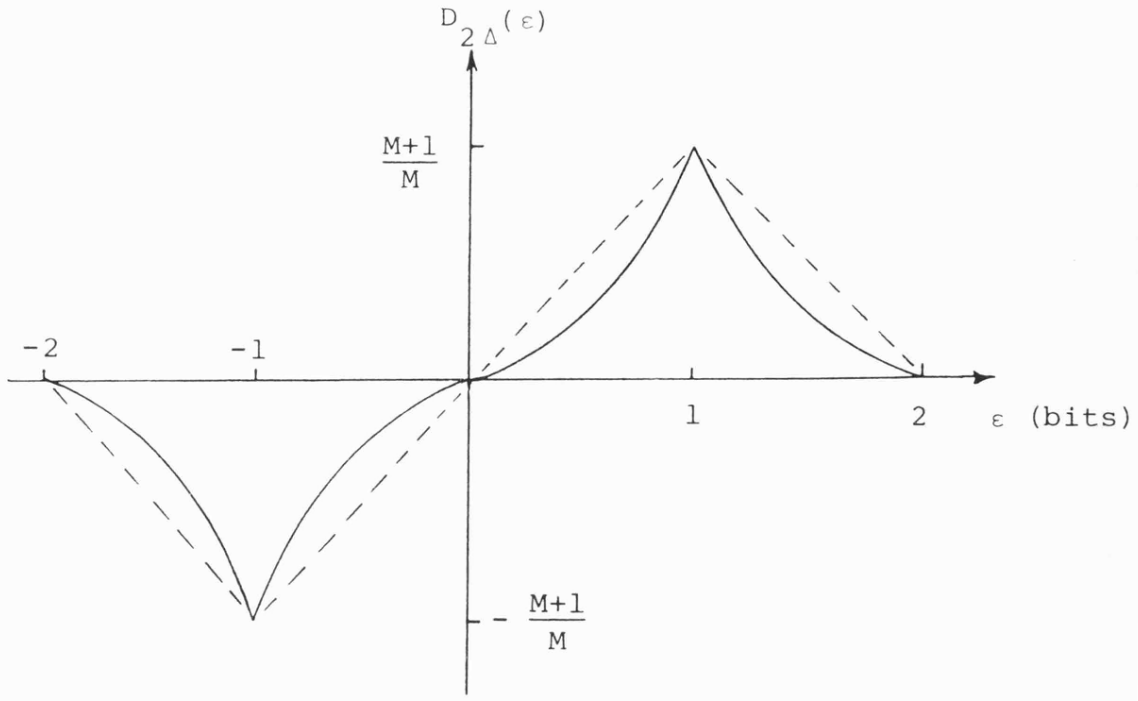


Figure 3.7. Discriminator characteristic with a square low detector as the envelope detector.

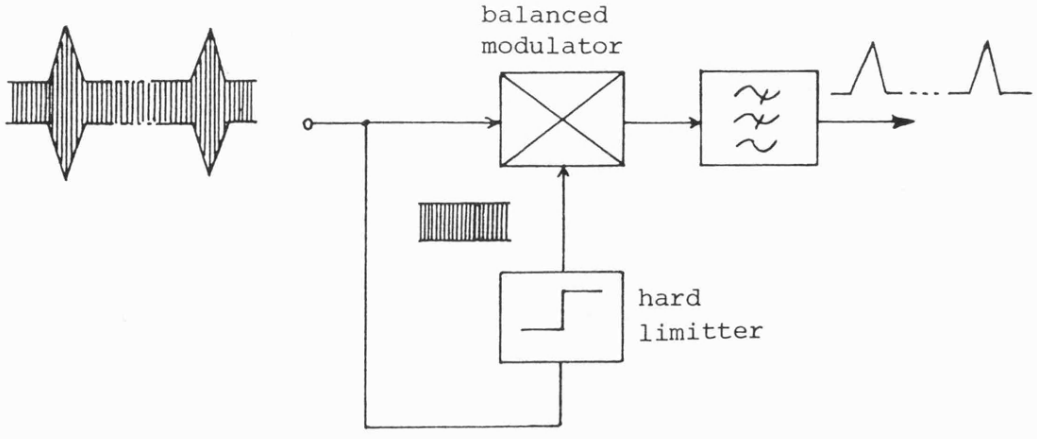


Figure 3.8. Coherent envelope detector.

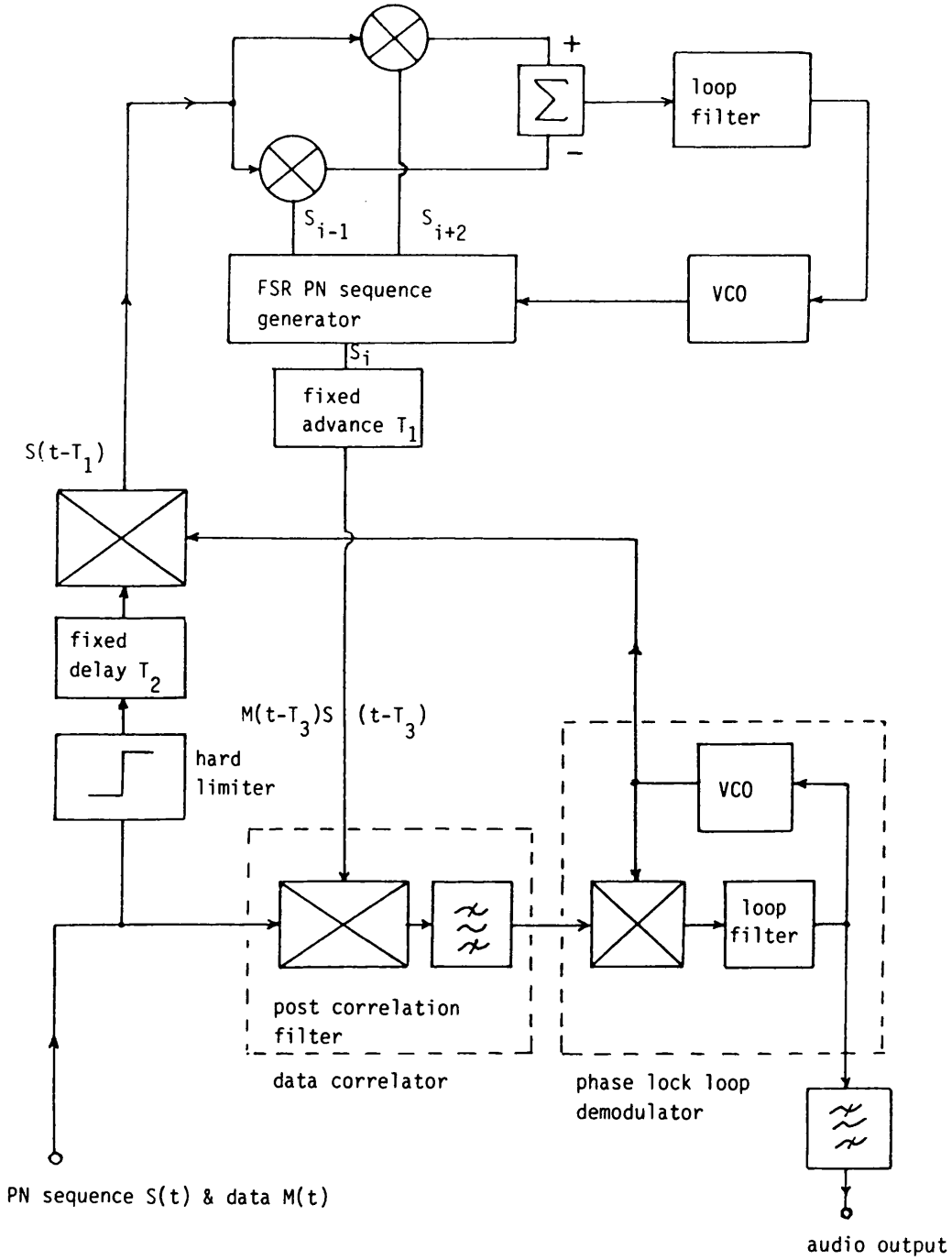


Figure 3.9 Delay lock loop with data feedback.

the data modulated PN sequence in the DLL. If the data estimate is a good one data is removed from the PN sequence. The data estimate is obtained by performing a slow serial epoch search between the received and locally generated sequence. As the two sequences slide past the point of phase synchronisation the data estimate is made via the normal data correlator. This estimate is used to remove the data on the PN sequence and the loop "snaps" into lock. If the serial search is too fast a reliable data estimate cannot be made and the phase lock may not be possible.

3.2.2 Acquisition using a Delay Lock Loop

In general, an obvious requirement of the synchronisation system is that the initial acquisition of lock should be as rapid as possible and tracking of phase changes due to doppler shift, etc. should be accurate and fast.

As has been said earlier the delay lock loop can be used for acquiring synchronisation as well as maintaining phase synchronisation. The error curve obtained for maximal length sequences gives information regarding the relative phases of the codes only when the sequences are within -n and +m bits of synchronisation where n=1/2, 1, 2, 3 and m=1/2, 1, 2, 3 [18]. Beyond this range of delay error no phase information is available to the voltage controlled oscillator until the sequences next come into synchronisation, which is achieved by offsetting the loop voltage controlled oscillator clock frequency relative to the clock frequency of the received sequence. The acquisition time of the delay lock loop is the mean time taken to search all the epochs of the sequence, plus the pull-in time required to achieve a given delay error

accuracy. Pull-in occurs from the moment when delay error information is supplied to the correlator. However, even in noiseless conditions final acquisition can only be guaranteed if the maximum initial search rate is less than a certain critical value, which, for the second order 2-Δ delay lock loop has been found to be [21]

$$V_{max_2} = 2\ \omega_n \text{ bit/sec} \tag{3.1}$$

where ω_n is the natural frequency of the loop (rad/sec).

For search rates above this value it is not possible for the standard 2-Δ delay lock loop to acquire lock. In noisy conditions it is only possible to specify a probability that lock will be achieved [22], even when the search rate is less than the maximum given by equation (3.1).

The search rate can, of course, be increased arbitrarily by increasing the natural frequency of the loop ω_n. However, this is at the expense of increased equivalent noise bandwidth of the loop. For a second order loop with active lag-lead filter this is given by:

$$B_n = \omega_n\ (\xi + 1/4\xi) \tag{3.2}$$

defined for the frequency range $-\infty < \omega < \infty$, where ξ is the damping factor of the loop.

This would worsen the in-lock phase jitter of the loop, and the delay lock loop design must be a compromise between good acquisition performance and in-lock jitter performance (and hence mean-time to loss of lock).

3.2.3 Transient Performance of the Delay Lock Loop

The dynamics of acquisition and pull-in are determined by the loop gain, loop filter characteristics and the shape of the discriminator characteristics. In particular, these parameters, set the maximum rate of change of phase error which the loop is able to track. More importantly, they also set the maximum rate of change of phase allowed in the initial epoch search from which the loop can still acquire lock.

It is convenient to present the delay lock loop as a linear equivalent circuit [5, 12, 13] in which the separate delay lock loop correlator arms and sequence generators are replaced by the discriminator characteristics. This represents the mean value of the delay error signal fed to the loop filter for a given delay error between the two sequences.

The loop filter has a transfer function F(s) and the lumped gain of the voltage controlled oscillator and mixer is given as G. Let us consider that the received sequence is $s(t + \tau)$, where τ is some arbitrary delay. The sequence has two values, ± 1, and the locally generated sequence is $s(t + \hat{\tau})$ also with values of ± 1. The tracking error is $\varepsilon = \tau - \hat{\tau}$, where $\hat{\tau}$ is the estimate of τ. The output of the correlator network is:

$$\{s(t+\tau)[s(t+\Delta+\hat{\tau}) - s(t-\Delta+\hat{\tau})]\}$$

Because of the averaging effect of the loop filter this is equivalent to the following correlation estimate:

$$= R(\tau-\hat{\tau}-\Delta) - R(\tau-\hat{\tau}+\Delta) = D_{2\Delta}(\tau-\hat{\tau}) = D_{2\Delta}(\varepsilon)$$

For a more general loop $D_{2\Delta}(\varepsilon)$ may be replaced by $D(\varepsilon)$. The linear model of the loop is shown in Figure 3.10. From this it is apparent that the time estimate, τ is expressed as:

$$\hat{\tau} = \frac{GF(s)}{s}[D(\varepsilon)] \text{ sec} \tag{3.3}$$

So $D(\varepsilon)$ is the normalised discriminator characteristic which relates the delay error, ε, between the sequences to the control signal operated on by $GF(s)/s$.

Normalising the timing estimate and delay error into bits rather than real time we may define new variables x and y such that:

$\varepsilon/T = x$, $\tau/T = y$ and $D(\varepsilon/T) = D(x)$

where $T = \Delta$ = the period of one chip of the maximal sequence.

Equation 3.3 becomes:

$$s(x-y) = GF(s)\,[D(x)] \tag{3.4}$$

F(s) is generally either a passive lag-lead low pass filter:

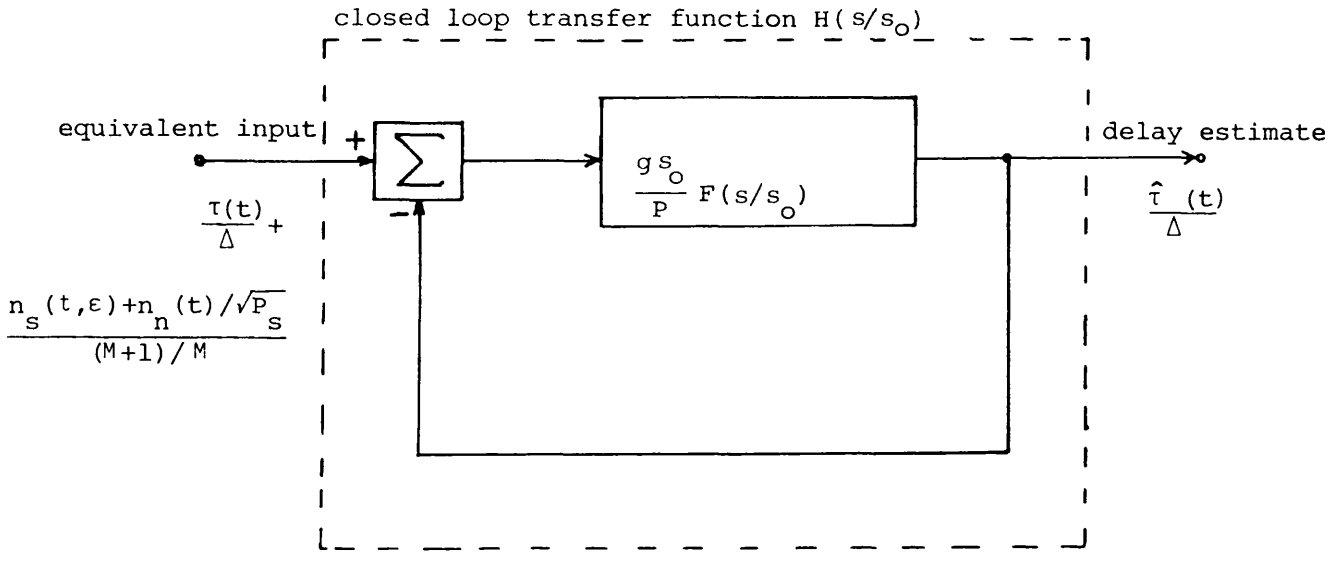
$$F_1(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s} \tag{3.5}$$

or an active lag-lead low pass filter.

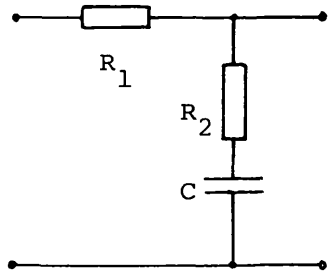
$$F_2(s) = \frac{1 + \tau_2 s}{\tau_1 s} \tag{3.6}$$

Using the passive filter for the sake of generality, it is possible to define $\tau_1 = G/\omega_n^2$, $\tau_2(2\xi/\omega_n - 1/G)$ and $g=G/\omega_n$, where ξ is the damping factor of the loop. If the gain G is high, such that $1/g << 2\xi$ then:

$$gF_1(s) \approx \frac{1 + 2\, s/\omega_n}{1/g + s/\omega_n} \tag{3.7}$$



(a)



(b)

loop filter

$$F(s/s_o) = \frac{1+\sqrt{2}\ s/s_o}{1+g\ s/s_o}$$

R_2 = arbitrary

$R_1 = (g/\sqrt{2}-1)R_2$

$C = \sqrt{2}/R_2 s_o$

Figure 3.10. Linearised equivalent circuit for the delay lock loop, valid for:

a) Block diagram

b) Loop filter

and thus

$$\frac{s}{\omega_n}(y-x)\,\frac{1 + 2\xi s/\omega_n}{1/g + s/\omega_n}\,[D(x)] \tag{3.8}$$

Defining [23]

$$\dot{y} = \frac{1}{\omega_n}\frac{dy}{dt}\ , \text{ and } \dot{x} = \frac{1}{\omega_n}\frac{dx}{dt}$$

as normalised rates of change of y and x (bit/sec) gives the results:

$$\frac{1}{g}(\dot{y}-\dot{x}) + \ddot{y}-\ddot{x} = D(x) + 2\xi\ \frac{d\,D(x)}{dx}\,\dot{x} \tag{3.9}$$

which may be rewritten as:

$$\frac{d\dot{x}}{dx} = -\frac{D(x) + 2\xi\,\dot{D}(x)\,\dot{x} - \ddot{y} + \frac{1}{g}(\dot{x}-\dot{y})}{\dot{x}} \tag{3.10}$$

This is the defining equation of the normalised phase plane of the acquisition trajectory. This non-linear equation cannot be solved analytically. For spread spectrum applications where the transmitter and receiver are stable and stationary $\dot{y}$ and $\ddot{y}$ will be zero. For mobile applications where there is a constant Doppler shift $\dot{y}$ is finite but $\ddot{y}$ is still zero. $\dot{y}$ represents the steady state tracking error due to transmitter code offset and this may be in a direction which reinforces the initial epoch search rate, or counteracts it. However, it is the net rate of change of the normalised error signal, $\dot{x}$, which is important for acquisition. If $\dot{y}$ is 0 then the normalised initial epoch search rate may be set at the value $\dot{x}_{s\ max}$, where $\dot{x}_{s\ max}$ is the highest value of x which will still allow phase lock. If $\dot{y}$ is finite and positive the maximum initial epoch search rate ($\dot{x}_{s\ max} - \dot{y}$) will be reduced. If the Doppler shift is such that $\dot{y}$ is negative the transmitted sequence is forced to slide past the local sequence and the net search rate is

enhanced. $\ddot{y}$ is only non zero when the vehicle is accelerating or the receiver VCO is not stable. As $\dot{y}$ and $\ddot{y}$ may be assumed to be zero in normal conditions, and g is high, the phase plane equation can now be written as:

$$\dot{x} \frac{d\dot{x}}{dx} = \ddot{x} = -D(x) - 2\xi \dot{D}(x) \tag{3.11}$$

which can be split into two simultaneous first order differential equations:

$$\phi = \dot{x}$$
$$\phi = -D(x) - 2\xi \dot{D}(x) \tag{3.12}$$

These can be solved using the Range-Kutta-Merson numerical technique. The method requires initial conditions for x and $\dot{x}$ and then subsequent values of $\dot{x}$ can be found for steps of x which satisfy equation 3.12. In this way the trajectory can be built up. The trajectory indicates whether lock has been achieved or not. The initial condition, $\dot{x}_s$, is then adjusted and a new trajectory computed until the maximum search rate is found. This occurs when the trajectory does not converge to the point $x = \dot{x} = 0$.

By examining equations (3.12), it is clear that the lock-on transient of the delay lock loop depends quite critically on the N-shape delay error characteristic D(x), and the maximum initial rate of change $\dot{x}$ or $\dot{\varepsilon}$. The characteristic of D(x) also determines how much the received signal and the locally generated sequence can be displaced without losing lock when phase synchronisation has been achieved.

3.2.4 Effect of the Width of the Discriminator Characteristic on the Maximum Search Rate

The maximum initial search or slipping rate has been computed by several authors [12, 13, 18] for different types of delay lock loops.

Neilsen [21] corrected the results of Spilker [13] and Zegers [24] by specifying the requirement that the discriminator characteristic should have a slope of -1 at x = 0, and showed that the maximum initial slipping rate of 1-Δ second order delay lock loop, $V_{1\ max}$, is

$V_{1\ max} = \omega_n$ for $\xi = 0.707$ where ω_n = natural frequency of the loop and $V = \dot{x}\,\omega_n$, as defined earlier.

For 2-Δ delay lock loop $V_{2\ max}$ is:

$$V_{2\ max} = 2\,\omega_n$$

Their phase plane plot or the acquisition trajectories are shown in Figures 3.11 and 3.12 for different values normalised initial search rate, $\dot{x}_s$ (i.e. $\dot{y}$ is assume to be zero and $\omega_n = 1$ rad s^{-1}).

Davis and Al-Rawas [18, 19] have shown that the initial search rate may be increased without increasing ω_n by broadening the discriminator characteristics beyond the normal width of 1-Δ or 2-Δ loops by the use of additional "early" and "late" correlations which are scalar weighted and summed, or differenced, as appropriate. They showed that the maximum search rate, $V_{4\ max}$, for the second order 4-Δ delay lock loop when $\xi = 0.707$ is:

$$V_{4\ max} = 4\omega_n$$

which is equal to twice the search rate of the 2-Δ loop having the same ξ and ω_n. The acquisition trajectories are shown in figure 3.13.

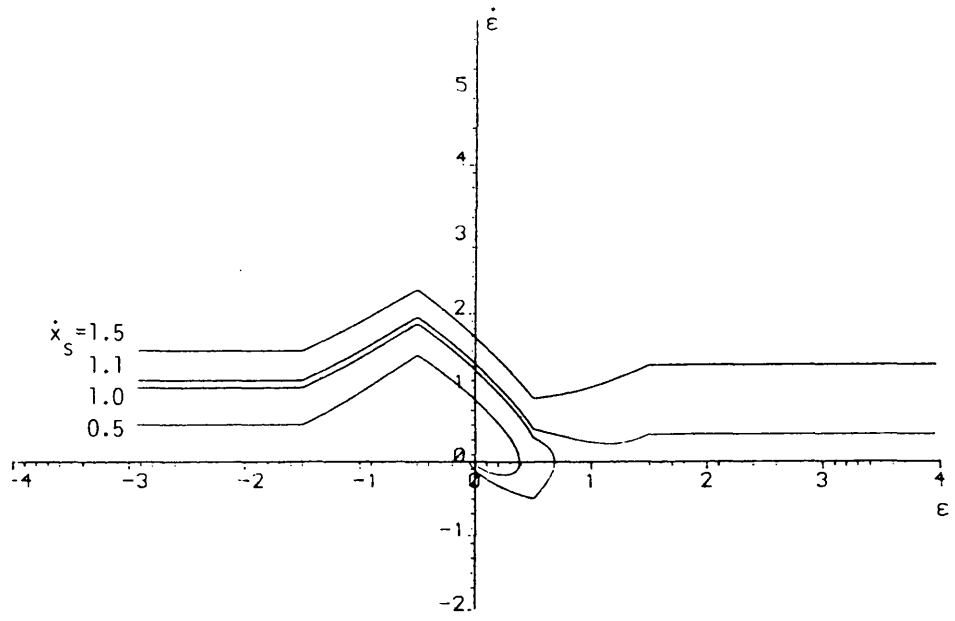


Figure 3.11 Acquisition trajectories of 1-Δ DLL

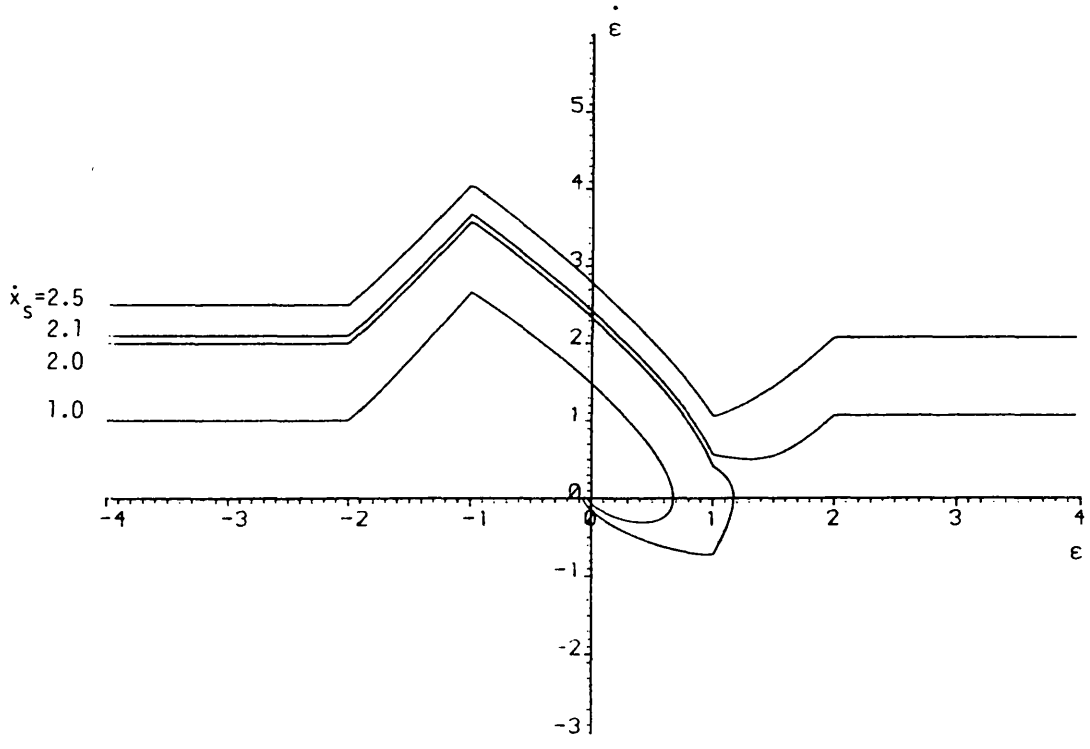


Figure 3.12. Acquisition trajectories of 2-Δ DLL

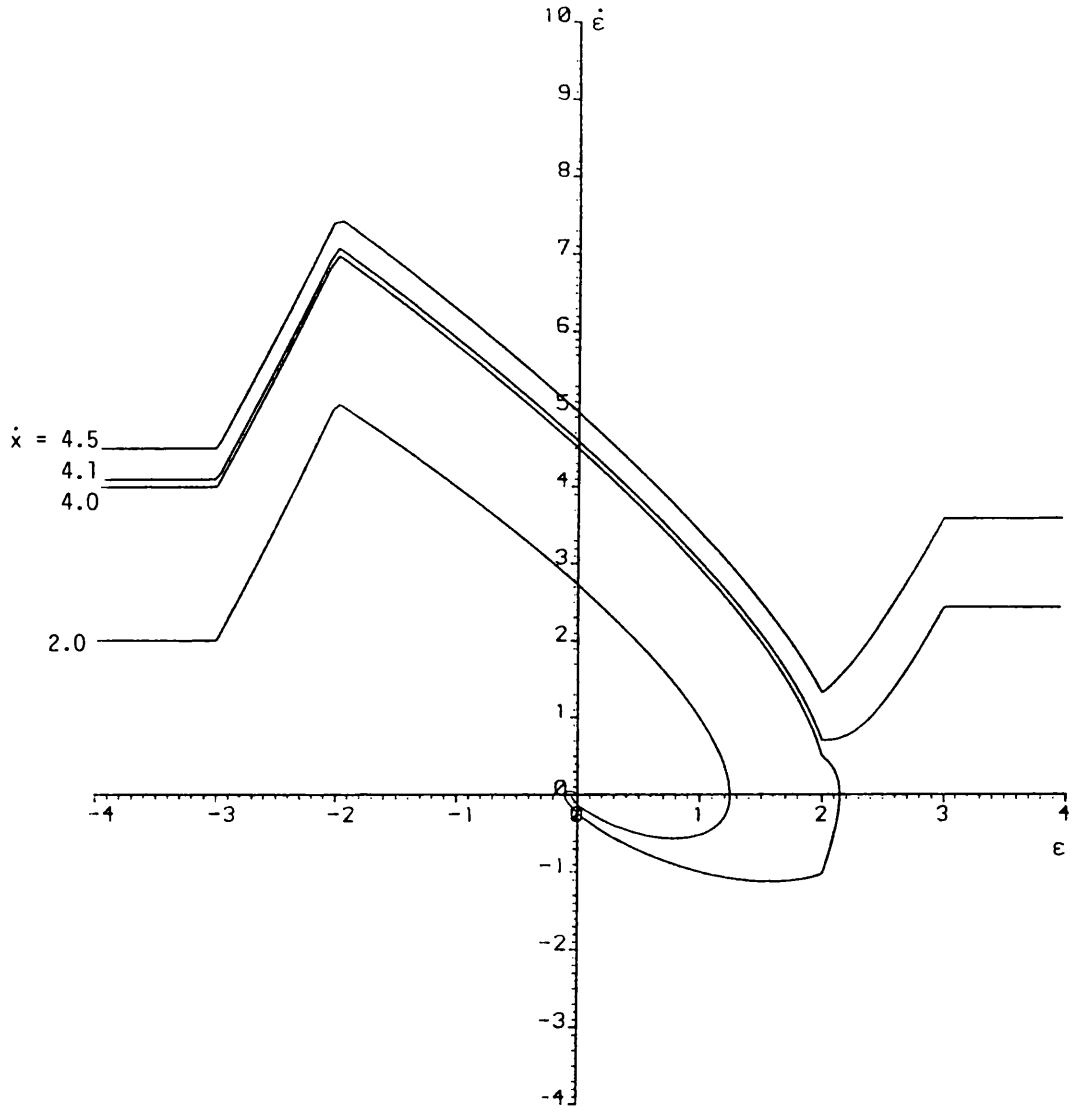


Figure 3.13. Acquisition trajectories of 4-Δ DLL

Therefore in general for symmetrical second order delay lock loops i.e. m=n,

$$V_{k\,max} = K\,\omega_n$$

where K is the separation between the "early" and "late" local reference sequences in the delay lock loop.

However, the case of the asymmetric loop has not been covered previously. As part of this program of research it has been found that for the general (n, m)Δ asymmetric loop the maximum search rate of the second order loop, for $\xi = 0.707$ is [25].

$$V_{max} \approx (2.3m - 0.3n)\,\omega_n \qquad (3.13)$$

for $G \longrightarrow \infty$, $\xi = 0.707$.

It can be seen that V_{max} may be increased almost arbitrarily by increasing the width of the discriminator characteristics. The limit is set by the length of the feedback sequence generator, and the penalty is increased hardware complexity. In effect, the extra correlations provide parallel processing of the code epochs. By examining equation 3.13, it can be seen that by increasing m only, i.e. broadening the "late" correlation function "triangle", the maximum initial search rate can be increased. But by increasing n or the "early" triangle of the discriminator characteristic the maximum search rate will be decreased. This is an important design criterion. A simple explanation of this behaviour is that as the loop performs a serial search at the rate $\dot{x}_s$ no information is provided to the VCO to alter this rate. As the sequences came into phase synchronisation the positive slope of the discriminator

characteristic causes the VCO to **increase** its search rate (note feedback is still negative because of the voltage offset on the VCO). The period of acceleration lasts for only 1 bit of delay error, however, the slope of the discriminator over this region is directly proportional to n, and this determines the maximum value of $\dot{x}$ actually achieved during pull in. When the sequences are synchronised by a further bit the slope of the characteristic changes to -1 (because characteristics in this region are always normalised to -1) and the VCO decreases in frequency and the search process slows down. For acquisition of lock the critical parameter is the value of $\dot{x}$ when x = 0 in the upper quadrant of the phase plane. Thus, if the loop search process slows down at a constant rate for all types of loop the period of deceleration before x=0 must be as long as possible. This implies a large value of m. This behaviour is shown in the following loops. Figure 3.14 shows the acquisition trajectories of two kinds of delay lock loop having the same width of discriminator characteristic, but different early and late autocorrelation functions (n, m). The 2-3Δ delay lock loop has a maximum normalised initial search rate of $\dot{x}_s$=6.2, which is much more than that of the 3-2Δ delay lock loop which is only 3.7.

In all these acquisition trajectories, the loop parameters chosen were: ω_n=1 rad/sec, ξ = 0.707, g$\longrightarrow\infty$. Also the slope of the discriminator characteristic D(0) was normalised to -1, as pointed out by Nielsen [21], to ensure identical in-lock performance for each loop. Each trajectory shows that there is a maximum search rate $\dot{x}_{s\ max}$ Above which, it is not possible to achieve lock.

Finally, the 1-3Δ delay lock loop, which has a 4Δ discriminator characteristic width is compared with a) 4-Δ delay lock

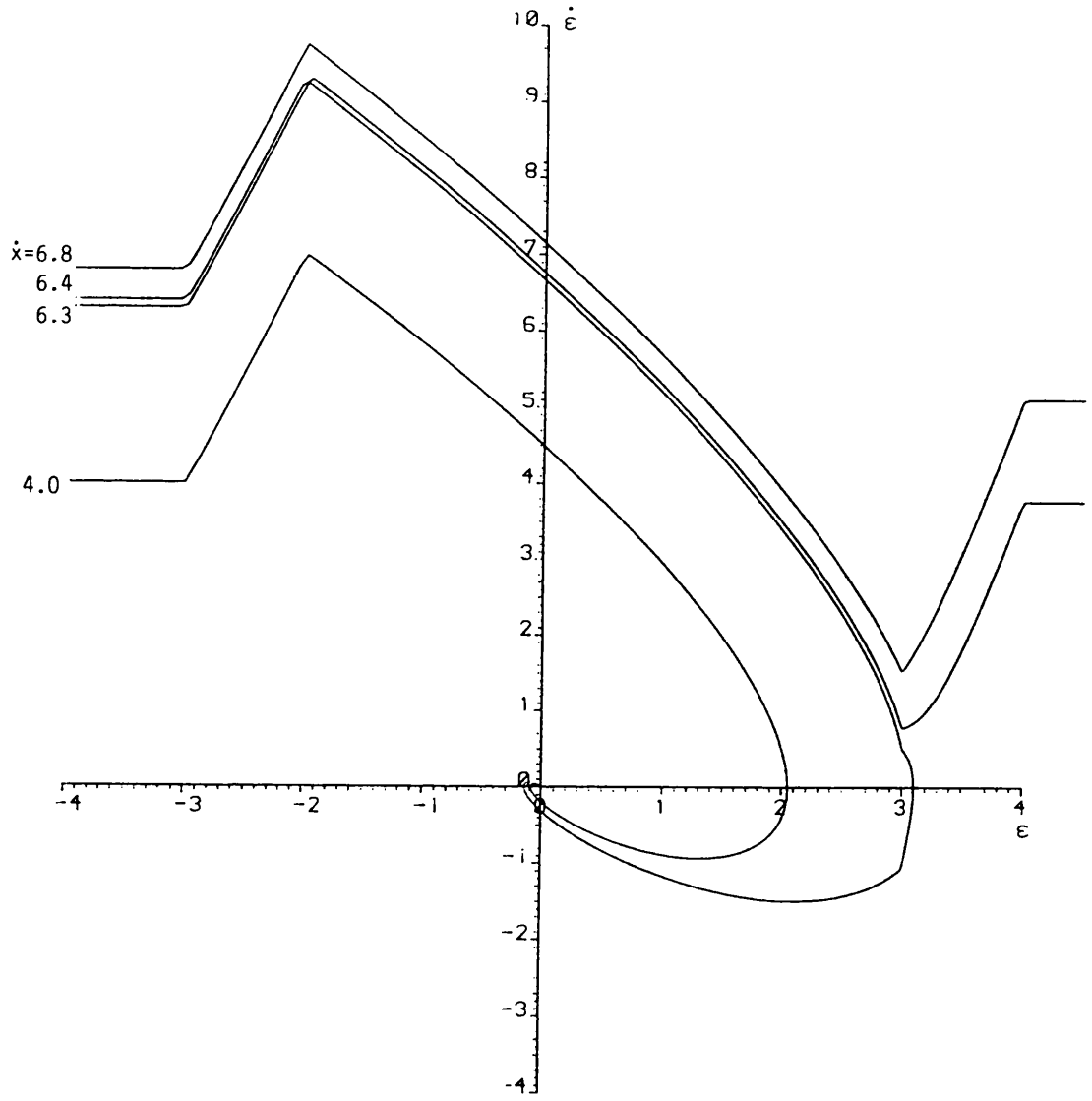


Figure 3.14 (a). Acquisition trajectories of 2-3Δ DLL.

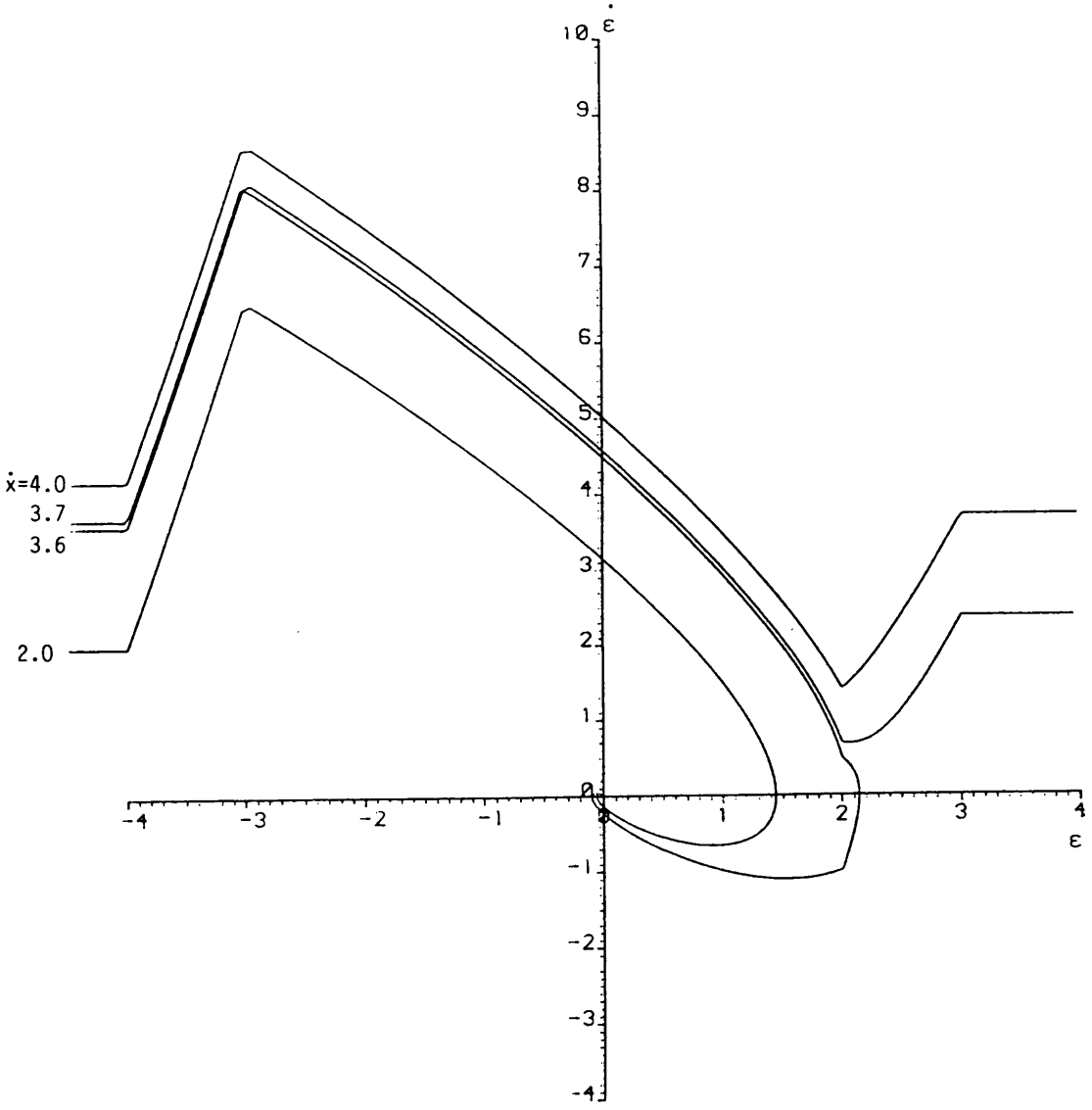


Figure 3.14(b). Acquisition trajectories of 3-2Δ DLL

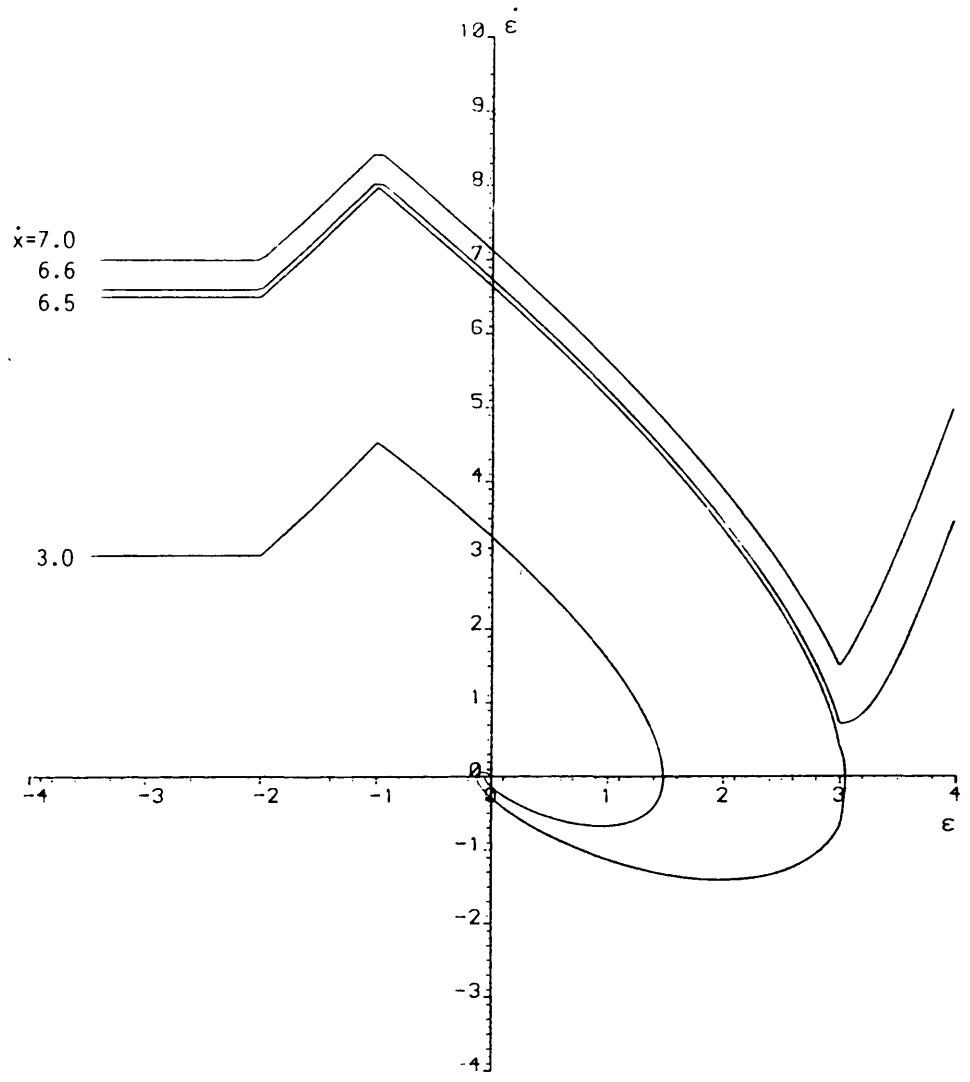


Figure 3.15. Acquisition trajectories of 1-3Δ DLL

loop and b) an even wider discriminator characteristic width such as 2-3Δ delay lock loop. The acquisition trajectories of the 1-3Δ delay lock loop is shown in Figure 3.15, which shows a maximum search rate of 6.5 ω_n. Clearly this is much higher than for the 4-Δ delay lock loop because the 1-3Δ loop has smaller n (i.e. lower acceleration) and larger m. In the second case although the 2-3Δ loop is wider than the 1-3Δ loop, the latter gives higher search rate, because it has smaller n and same m. The disadvantage of having small n is that the system may lose lock under high interference signal or poor signal to noise ratio. So one can note that the search rate can be made higher if the period for which the loop decelerates (in bits) can be increased relative to the period of acceleration. It is clear that the 4-Δ, 1-3Δ, and 2-3Δ loops have longer periods of deceleration relative to the period of acceleration than for the 1-Δ, 2-Δ, and 3-2Δ loops. Although the periods of deceleration are the same for 3-2Δ loop and 2-3Δ loop (or 4-Δ loop and 1-3Δ loop), the acceleration is twice as fast.

An important consequence of increasing the width of the discriminator characteristics is that the loop can tolerate wider phase deviations without losing lock due to either Doppler Shift or phase jitter on the VCO due to the presence of noise on the VCO control signal.

3.2.5 Effect of Gain on the Acquisition Trajectories

Figure 3.16 shows the acquisition trajectory of a standard 2Δ DLL plotted for an ideal loop gain, g=∞ and a loop gain g=10. Neilsen and Spilker [21, 10] have previously reported that if g>10 gain has very little effect on the trajectory, and the maximum

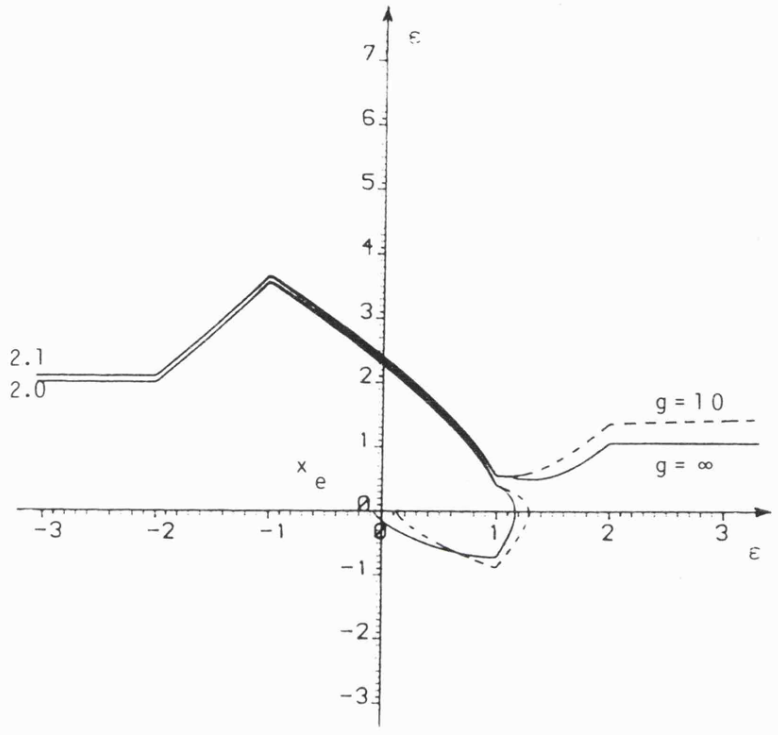


Figure 3.16. Effect of gain on the acquisition trajectories (2Δ DLL ξ=0.707).

initial search rate is little affected. However, Figure 3.16 illustrates two other interesting effects. The first is that when the loop gain is low the final steady state phase error (x_e bits) is considerably larger than for $g=\infty$ where steady state error is 0. This is due to loop stress, as pointed out by Gardner. Because the loop VCO idles at frequency greater than the nominal code clock frequency when frequency synchronisation has been achieved, a steady state error voltage is required to force the VCO to oscillate at the code clock frequency. This error voltage can only be generated via the discriminator and the two codes are phased offset to provide the error signal.

The second point is that if $\dot{x}_s > \dot{x}_{s\ max}$ the loop cannot acquire phase synchronisation and the codes continue to slide past each other. Note, however that when $g = \infty$ there is a new steady state search rate $\dot{x}_{s\ new}$ which is lower than the initial search rate. This is possible because of "memory" of the loop which stores the last value of delay error voltage when the discriminator characteristics change to 0 at +2 bit.

When $g < \infty$ this memory effect is imperfect - as shown in figure 3.16 and the search rate after the abortive synchronisation attempt slowly changes back to the initial value of $\dot{x}_s$.

3.3 A MODIFIED DELAY LOCK LOOP FOR IMPROVED SEARCH RATE

It is of great interest to modify the existing standard delay lock loops discussed earlier so that they can give a higher search rate to minimise the acquisition time, a wider search and tracking range, and allow higher Doppler shift to be tolerated. The

acquisition time is dominated by the serial search of the code epochs, rather than the pull-in time. This can be very long, especially when the code sequence used is very long. In spread spectrum systems the length of the sequence is very important because it determines the code repetition rate R_c.

$$R_c = \frac{\text{clock rate in bit per sec}}{\text{code length in bits}}$$

This repetition rate determines the line spacing in the radio frequency output spectrum and it is an important consideration in system design. One criterion for selecting code repetition rate is that the period of the code must exceed the length of any mission in which it is to be used. In most aircraft, for instance, an eight-hour code period may be used to exceed the flight capability [15]. Therefore, the acquisition time could be very long as well, and hence a significant amount of information could be lost.

From the foregoing it is apparent that the initial search rate can be increased, without altering the in-lock performance of the loop if the initial acceleration of the search process can be either removed, reduced, or changed into deceleration it is possible to increase the initial search rate of the delay lock loop yet still ensure that the maximum rate of phase change allows acquisition. Controlling the discriminator characteristics from within the loop enables this improvement to be effected.

3.3.1 Switched Delay Lock Loop

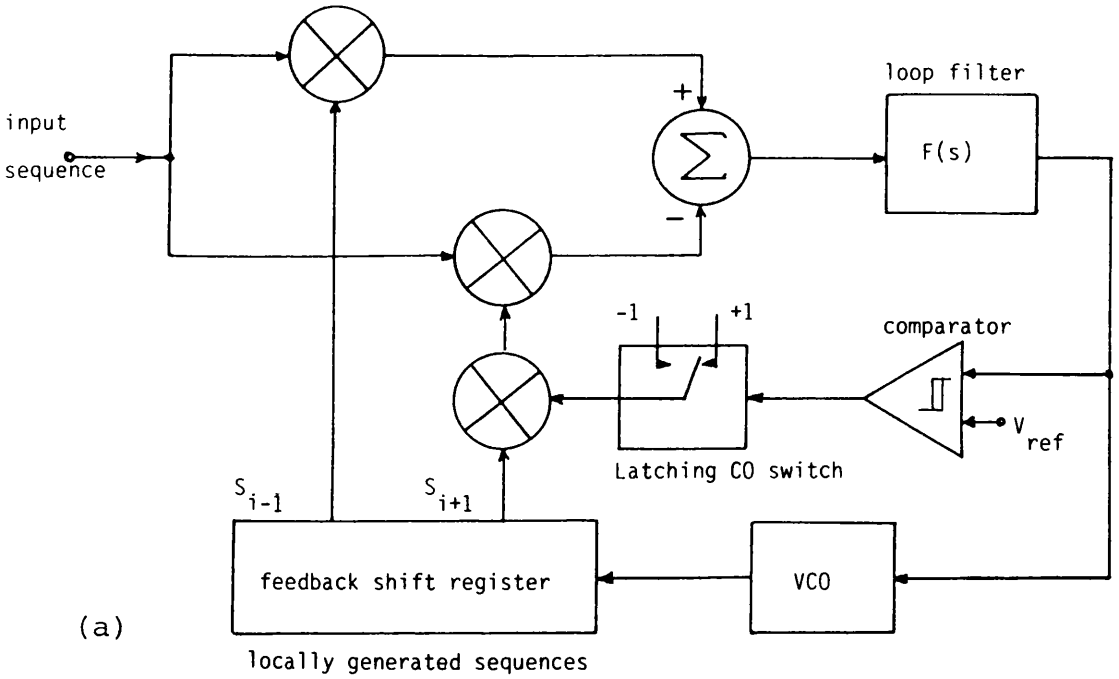
This section shows that a significant increase in search rate may be obtained by controlling the shape of the discriminator

characteristic from within the loop so that there is a minimal acceleration of the search rate during pull in.

Figure 3.17 shows a schematic diagram of a switched 2-Δ and 4-Δ delay lock loop applied to ranging receivers. These are purely for illustration and the technique may be applied to any delay lock loop configuration. Control of the discriminator characteristic is achieved by the addition of a linear multiplier, a latching changeover switch, and a peak hold/comparator. For a binary sequence an exclusive-OR gate controlled by an R-S latch may be used instead of the multiplier and switch.

The basis of the modification is to control the shape of the discriminator characteristic from that of the standard discriminator characteristic of Figure 3.18 (a) to that of Figure 3.18 (b), shown drawn for 1-Δ, 2-Δ, and 4-Δ loops. The exact position at which the discriminator characteristics are changed is determined from the output of the loop filter and the value of the reference voltage V_{ref}. In general the loop is first switched to produce the discriminator characteristic of Figure 3.18 (b) during the initial acquisition or searching phase. As the loop comes in to synchronisation, the slope of the discriminator characteristic is negative and the search rate decelerates rather than accelerates. When the delay error is at its peak negative value the loop is switched and the discriminator characteristic reverts to that of Figure 3.18 (a). The slope of the discriminator characteristic remains negative.

The control of the discriminator characteristics may be described more easily for the 2-Δ loop than the 4-Δ loop, although



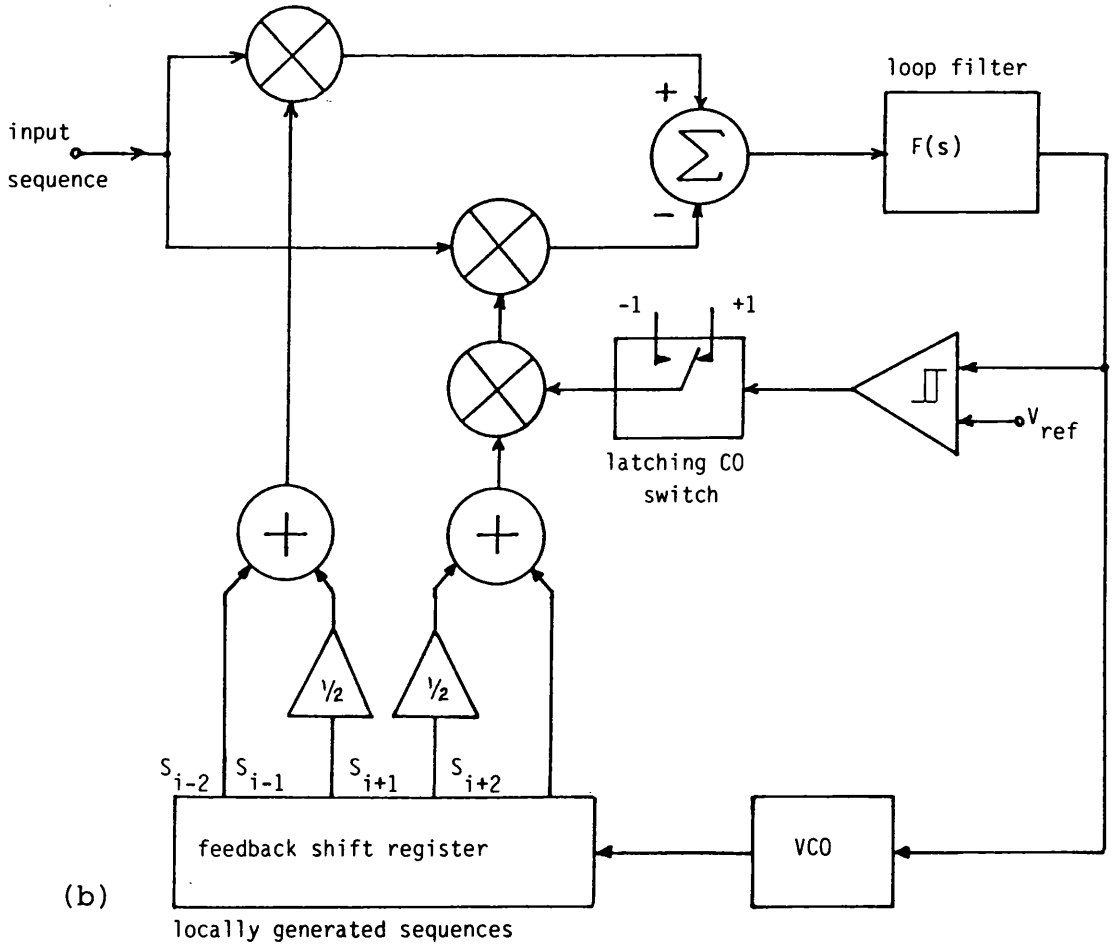


Figure 3.17. Switched delay lock loop schematics

a) 2-Δ loop

b) 4-Δ loop

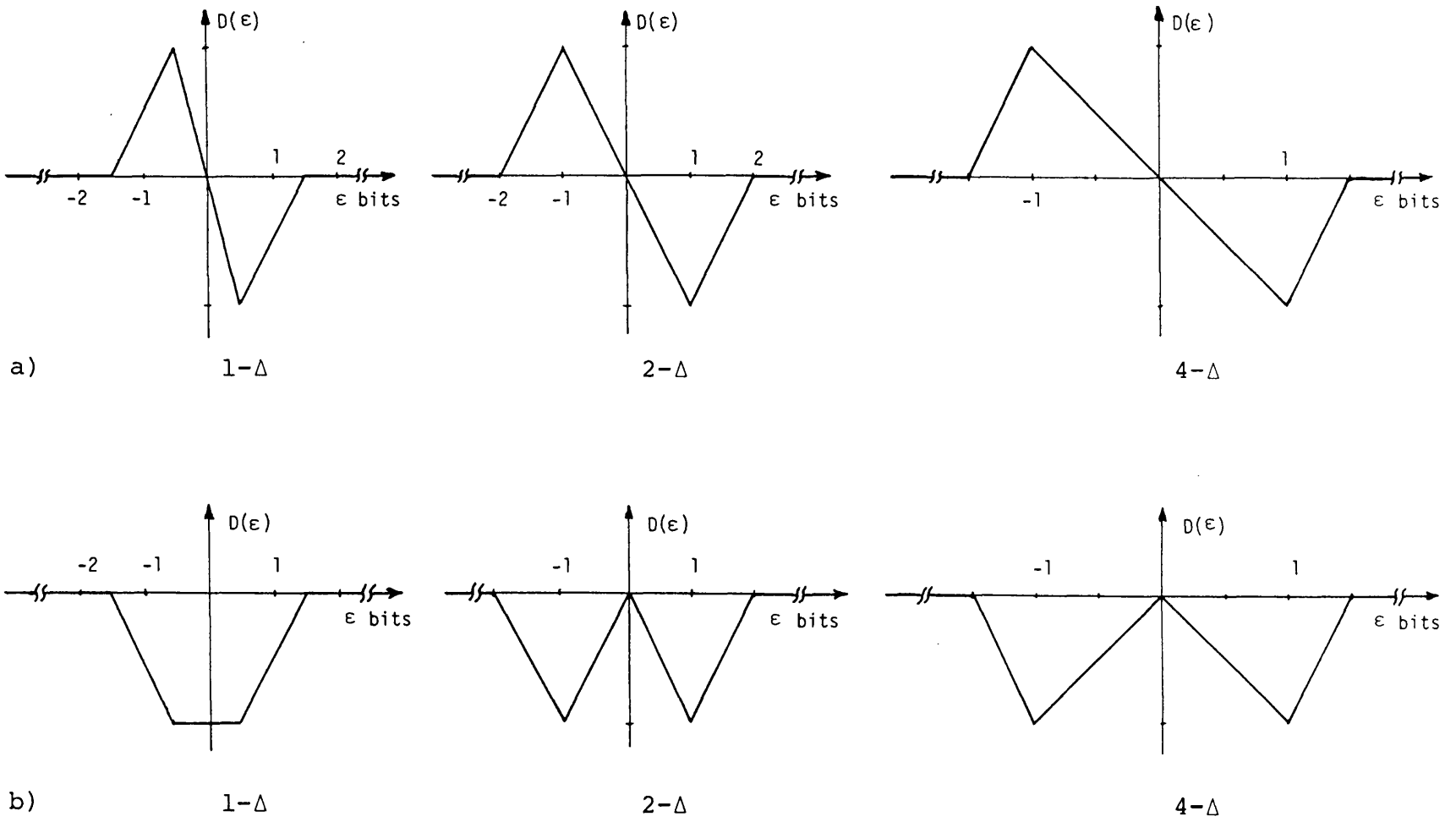


Figure 3.18. Normalised discriminator characteristics of 1,2 and 4-Δ DLL

a) Standard loops

b) Switched loops

the basic principle is identical. In the circuit of Figure 3.17 (a) either S_{i+1} or $\overline{S_{i+1}}$ may be fed to the appropriate arm of the delay lock loop under the control of the comparator when $\overline{S_{i+1}}$ is fed to the appropriate arm of the DLL that part of the correlation triangle is inverted. The sequences are initially switched so that S_{i-1} and $\overline{S_{i+1}}$ are fed to the arms of the delay lock loop to give the discriminator characteristic shown in Figure 3.18 (b). The search rate thus decreases as the sequences come into synchronisation (compared with an increase in search rate in a conventional delay lock loop). When the delay error is such that the discriminator characteristic has reached its peak negative value the state of the changeover switch changes and $\overline{S_{i+1}}$ is inverted back to the original sequence, S_{i+1}. This causes the correlation between the codes to change sign and the discriminator characteristic changes, as shown in Figure 3.18 (a). Although it is permissible to switch sequence $\overline{S_{i+1}}$ at other values of delay error during pull-in, switching over at the peak negative value gives the maximum improvement in search rate as shown subsequently. The switchover is controlled automatically. It may be controlled by comparing the delay error voltage with a fixed reference voltage, V_{ref}, in a Schmitt comparator, or using the peak hold/comparator circuit shown in Figure 3.17, and detailed later. Further, an "out of lock" detector, not shown, automatically resets the comparator to ensure that $\overline{S_{i+1}}$ is fed to the delay lock loop during the subsequent search if the loop should lose lock. The implementation shown in Figure 3.17 represents only one method of achieving a switched loop, other methods will be mentioned later.

It is clear that to maximise the initial search rate the acquisition trajectory of the loop must always show a decelerating

search rate in the upper quadrants of the phase of the trajectory.

By inverting the sequence during pull-in the mean value of the code correlation has a step increase, but after this step change the correlation function continues to decrease. The 'step' change would cause a large acceleration of the search process if allowed to pass directly to the voltage controlled oscillator, removing any benefit gained. However, this does not occur because of the low pass loop filter F(S), nevertheless, some acceleration of loop is inevitable and this limits the maximum initial search velocity from which acquisition can occur. This modification was applied experimentally and theoretically to 2-Δ, 4-Δ, 2-3Δ, 3-2Δ, 1-3Δ delay lock loops. In these experiments, the loop parameters are identical for each loop. A 1023 bit maximal length sequence was clocked at a nominal 1 MHz. The loop filter parameters were adjusted to give natural frequency ω_n=1 rad/sec and damping factor $\xi \approx 0.707$ and a loop gain G>40. It should be noted that because the loop filter and loop gain remains unchanged the in-lock noise performance of the modified loop is similar to that of the conventional loop. So the objective of the experimental work is to determine the phase-plane plot i.e. the acquisition trajectories of different types of the switched loop which indicates the maximum search rate for each loop in order to find out the benefit obtained. Details of the experimental set up are given in the Appendix.

A special circuit was built to detect the value of the delay error ε, for a range of delay errors from -5 bits to +4 bits, and also its derivative $\dot{\varepsilon}$ simultaneously, as shown in Figure 3.19. A Nicolet digital storage oscilloscope was used to store the values of ε and $\dot{\varepsilon}$ in order to plot the acquisition trajectories of the loops.

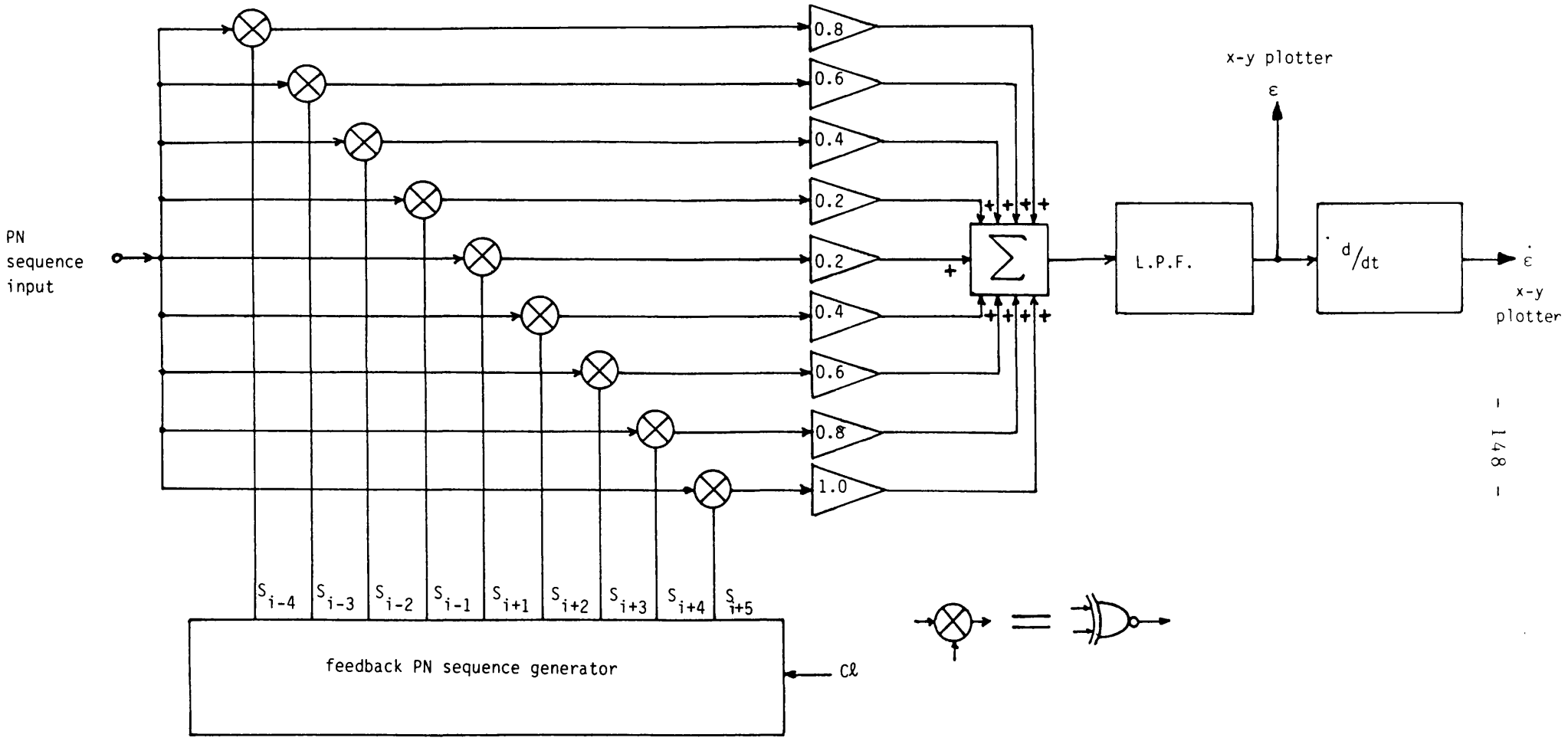


Figure 3.19. Schematic circuit diagram for the technique used to measure the acquisition trajectories of the DLLs.

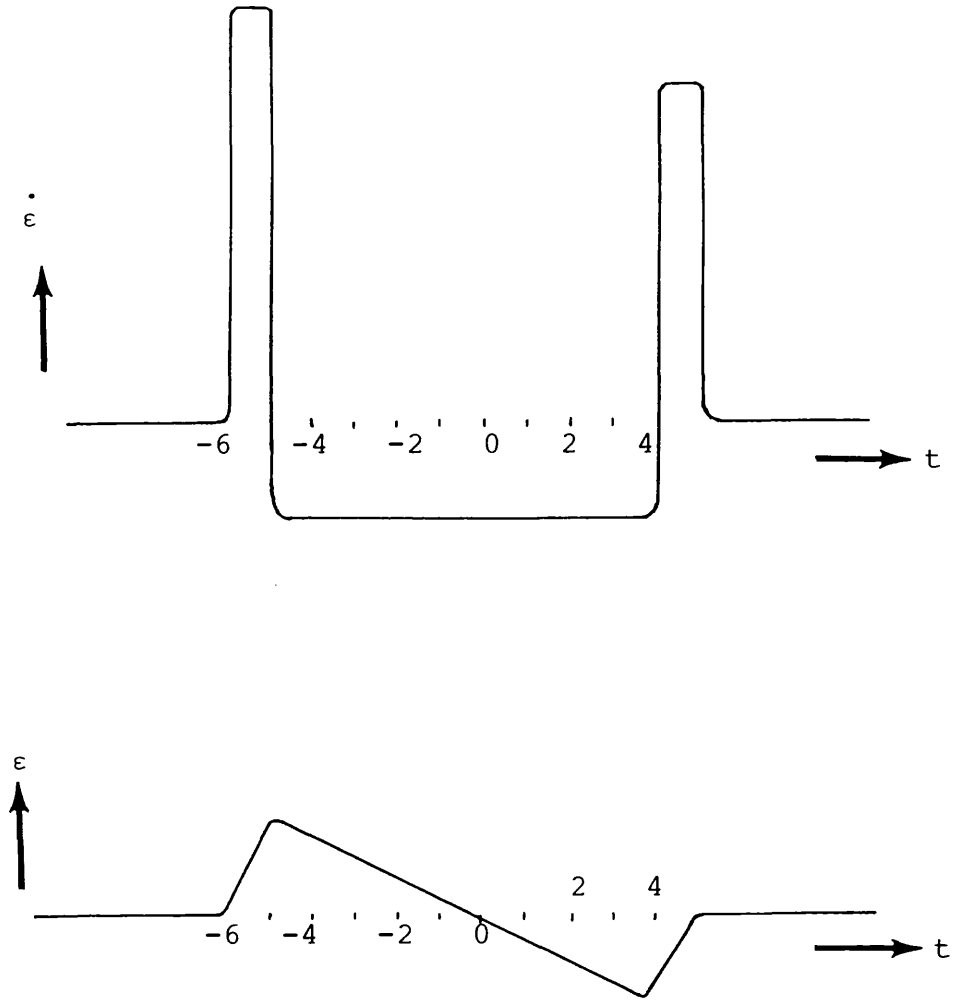


Figure 3.19 Continued.

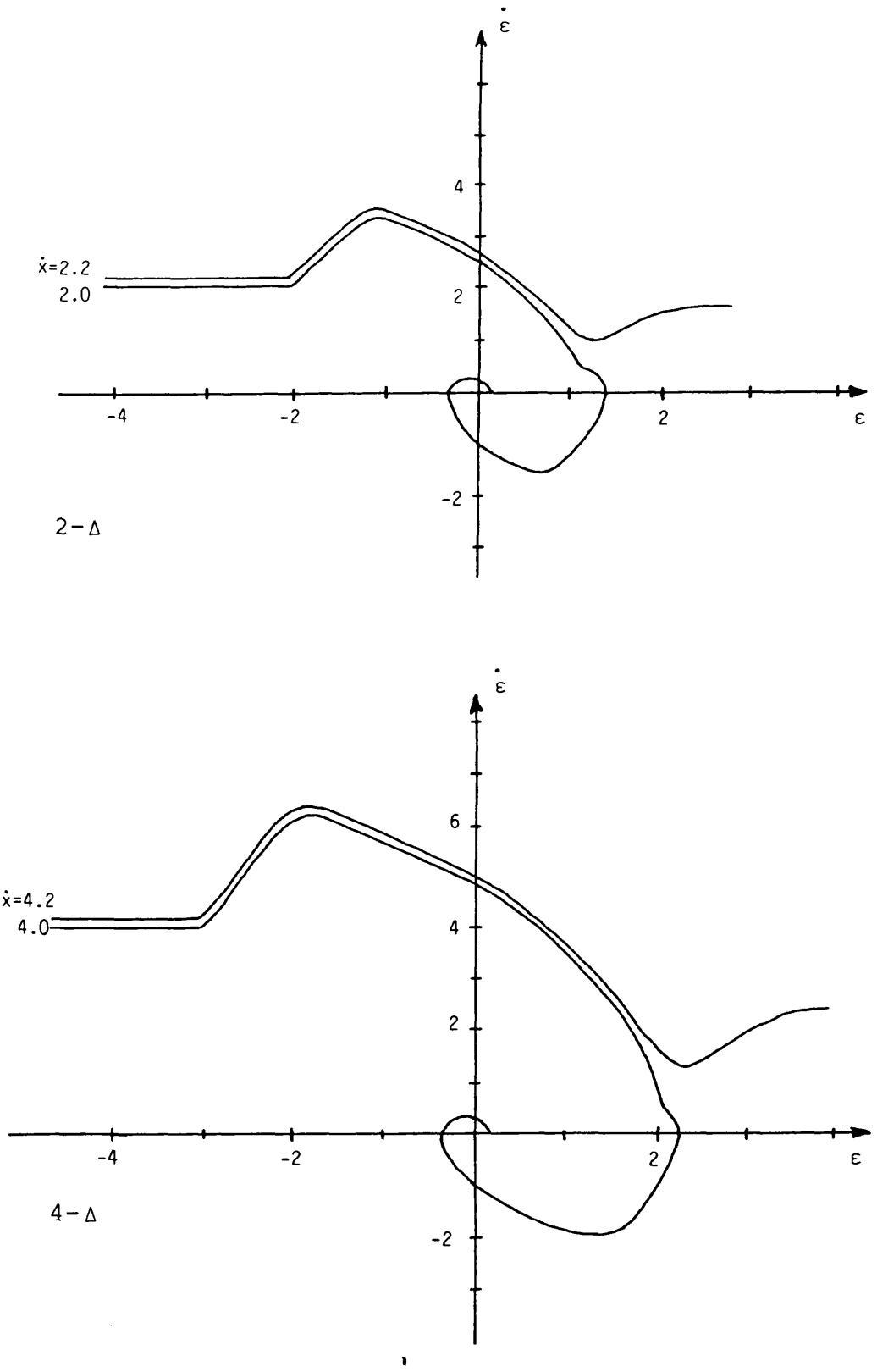


Figure 3.20 Experimenttal acquisition trajectories of standard 2-Δ, 4-Δ, 2-3Δ, 3-2Δ and 1-3Δ delay lock loop.

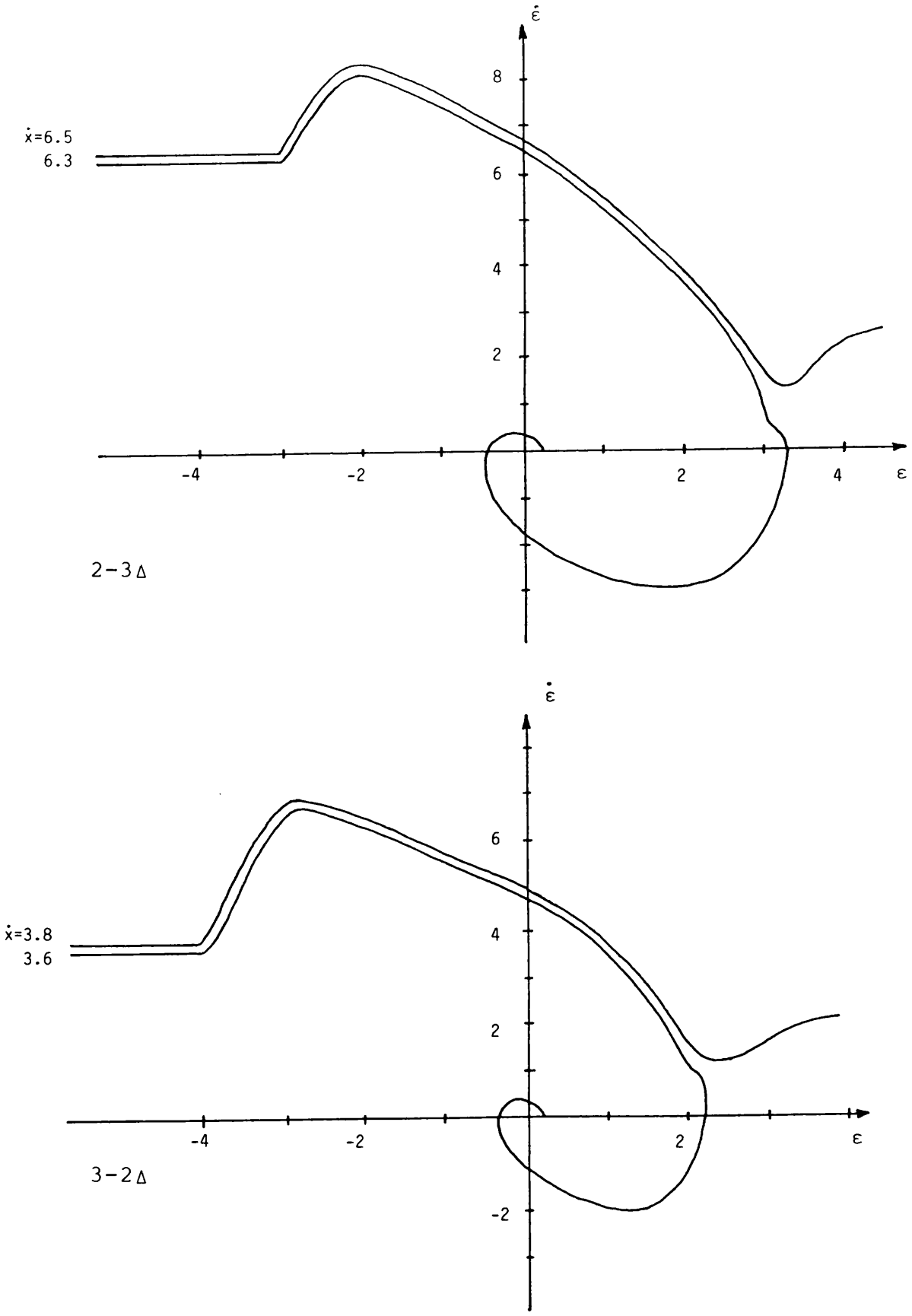


Figure 3.20 continued.

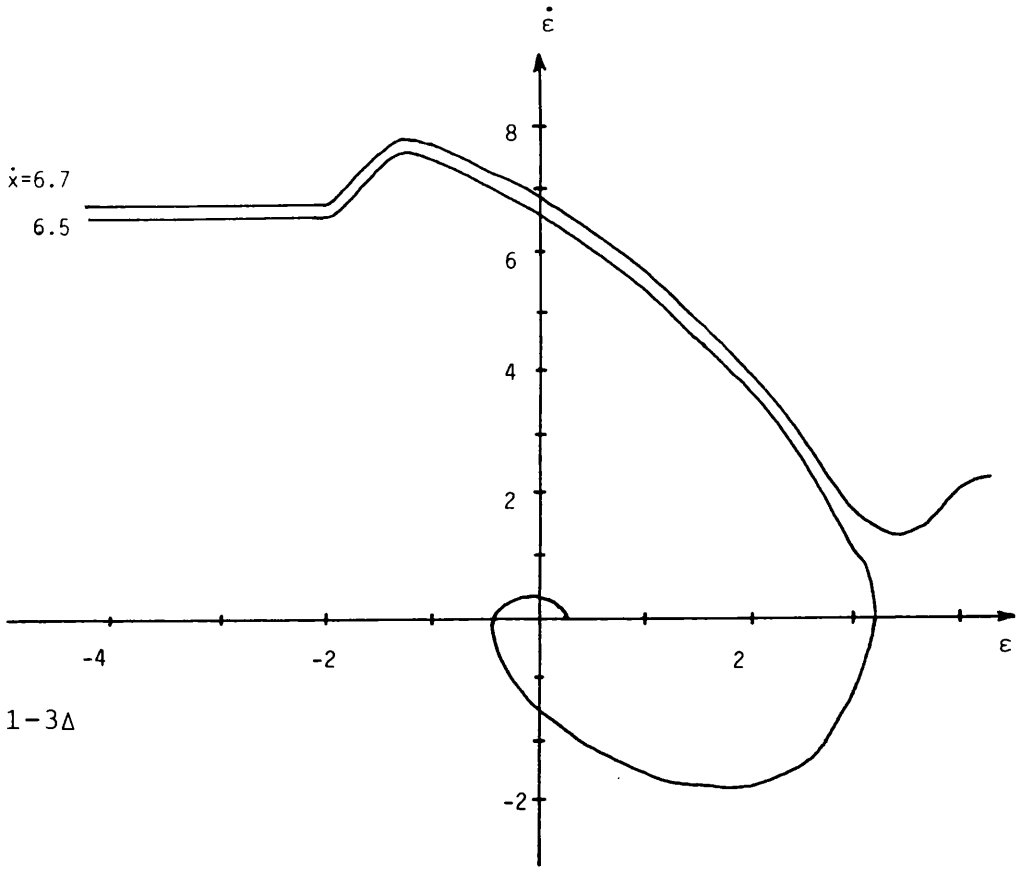


Figure 3.20 Continued

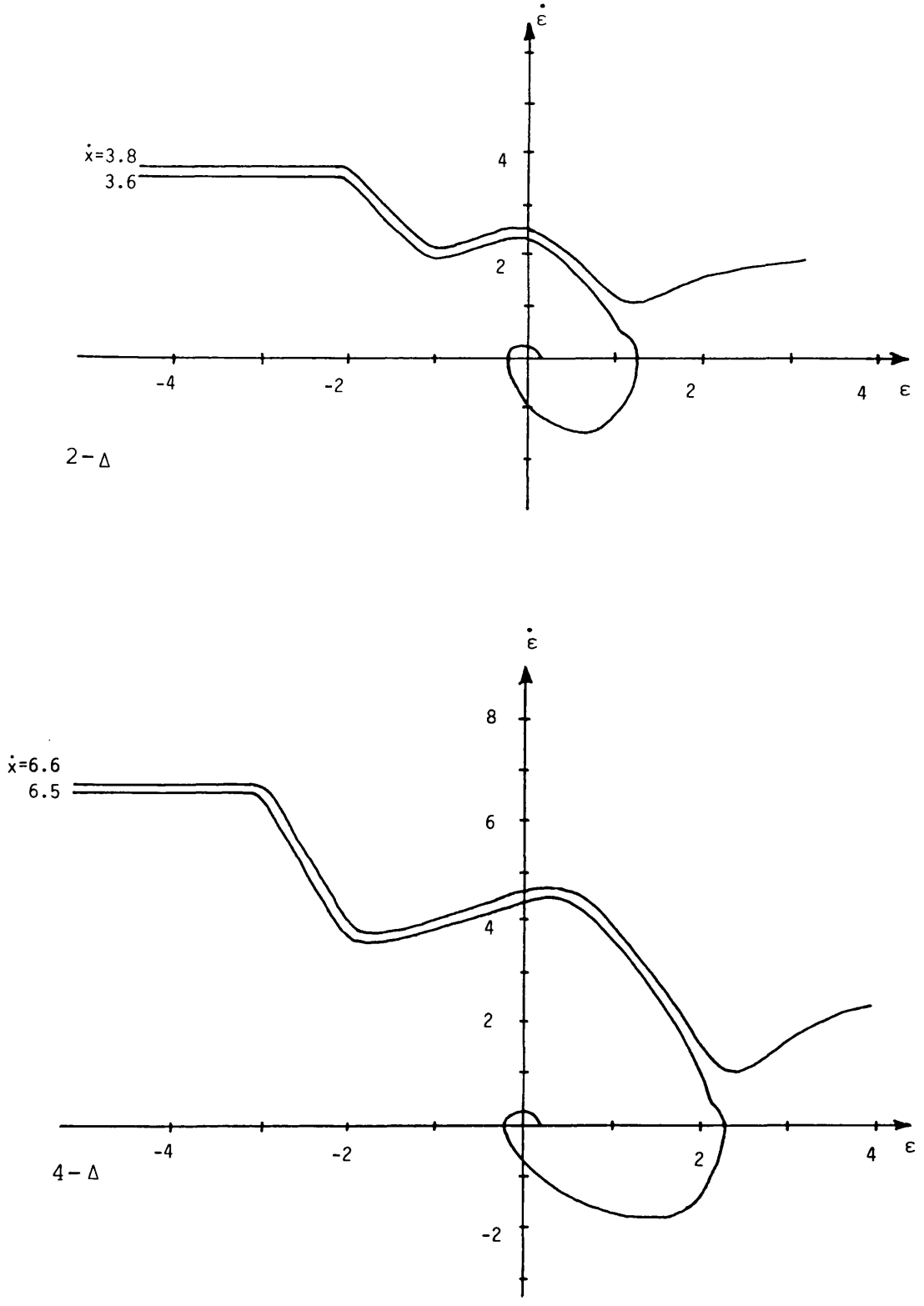
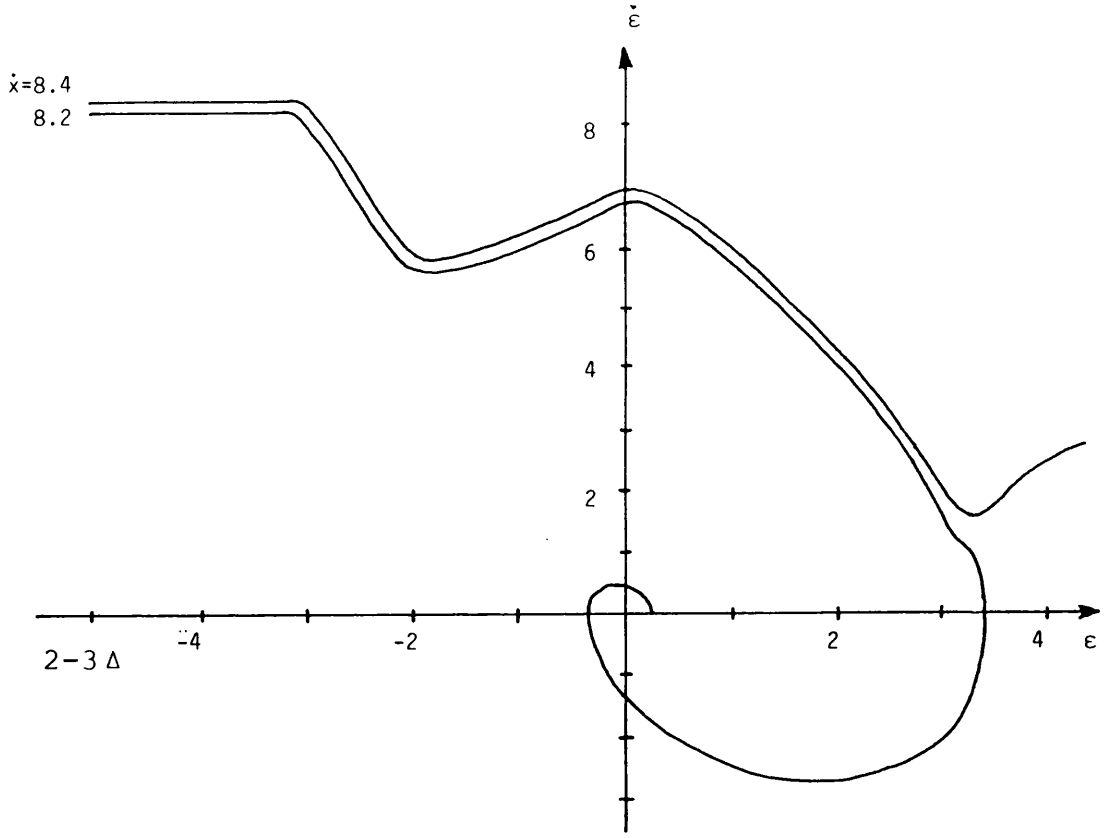


Figure 3.21. Experimental acquisition trajectories of switched 2-Δ, 4-Δ, 2-3Δ, 3-2Δ and 1-3Δ delay lock loop.



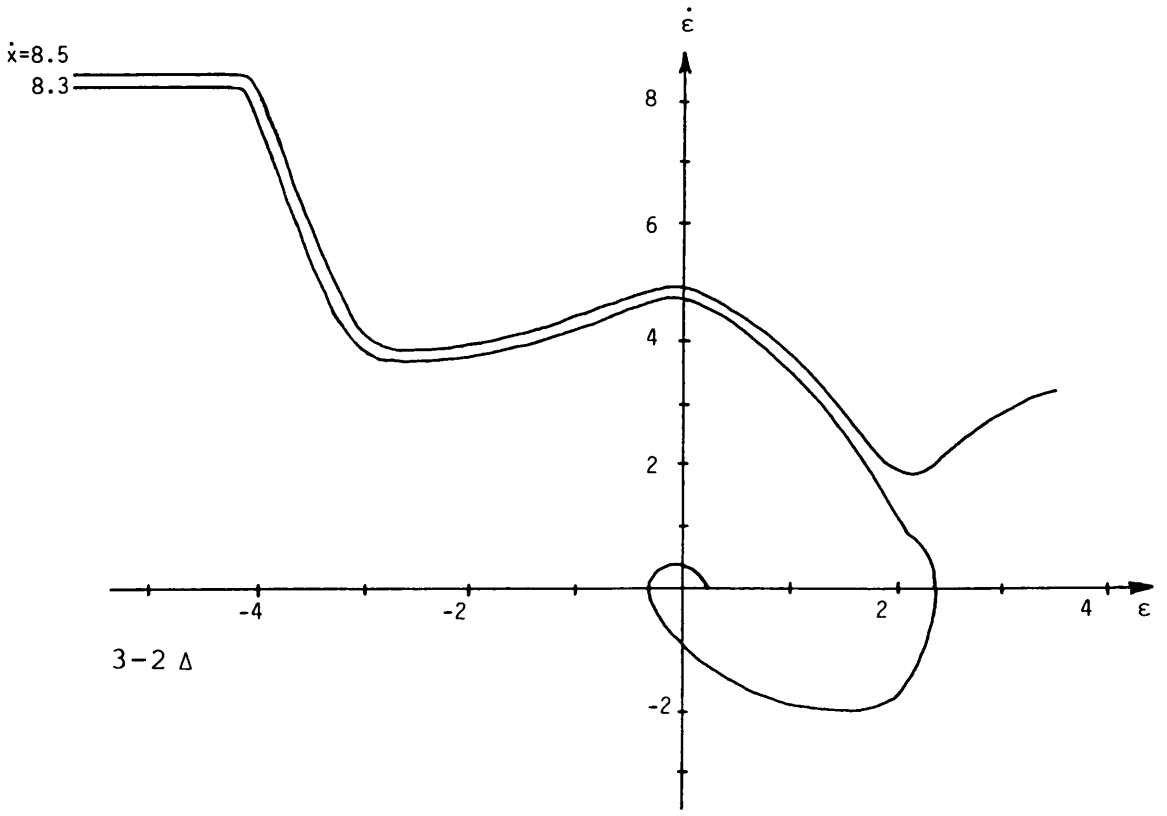


Figure 3.21. Continued.

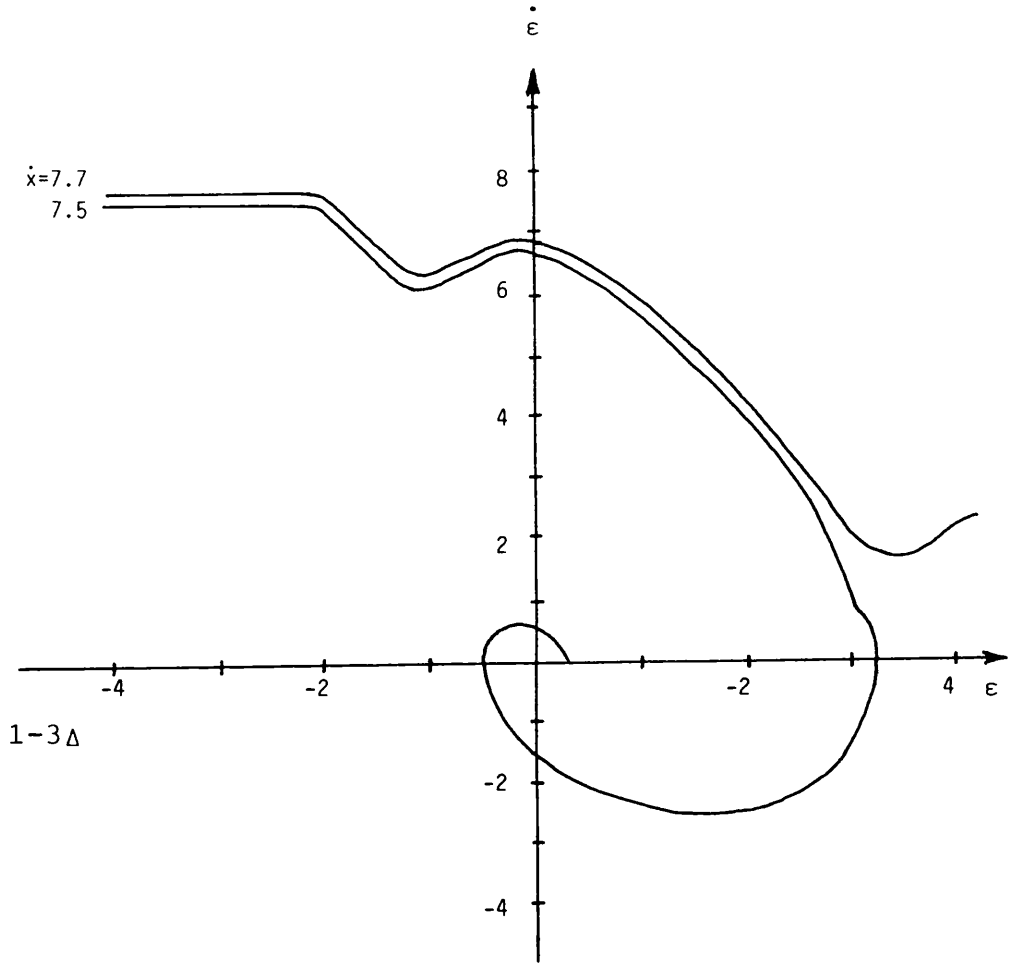


Figure 3.21. Continued.

Type of Loop	Standard Theoretical M.S.R.	Standard Experimental M.S.R.	Switched Theoretical M.S.R.	Switched Experimental M.S.R.
2-Δ	2.0	2.0	5.1	3.6
4-Δ	4.0	4.0	9.9	6.6
2-3Δ	6.3	6.3	12.2	8.2
3-2Δ	3.6	3.6	12.5	8.3
1-3Δ	6.5	6.5	9.5	7.5

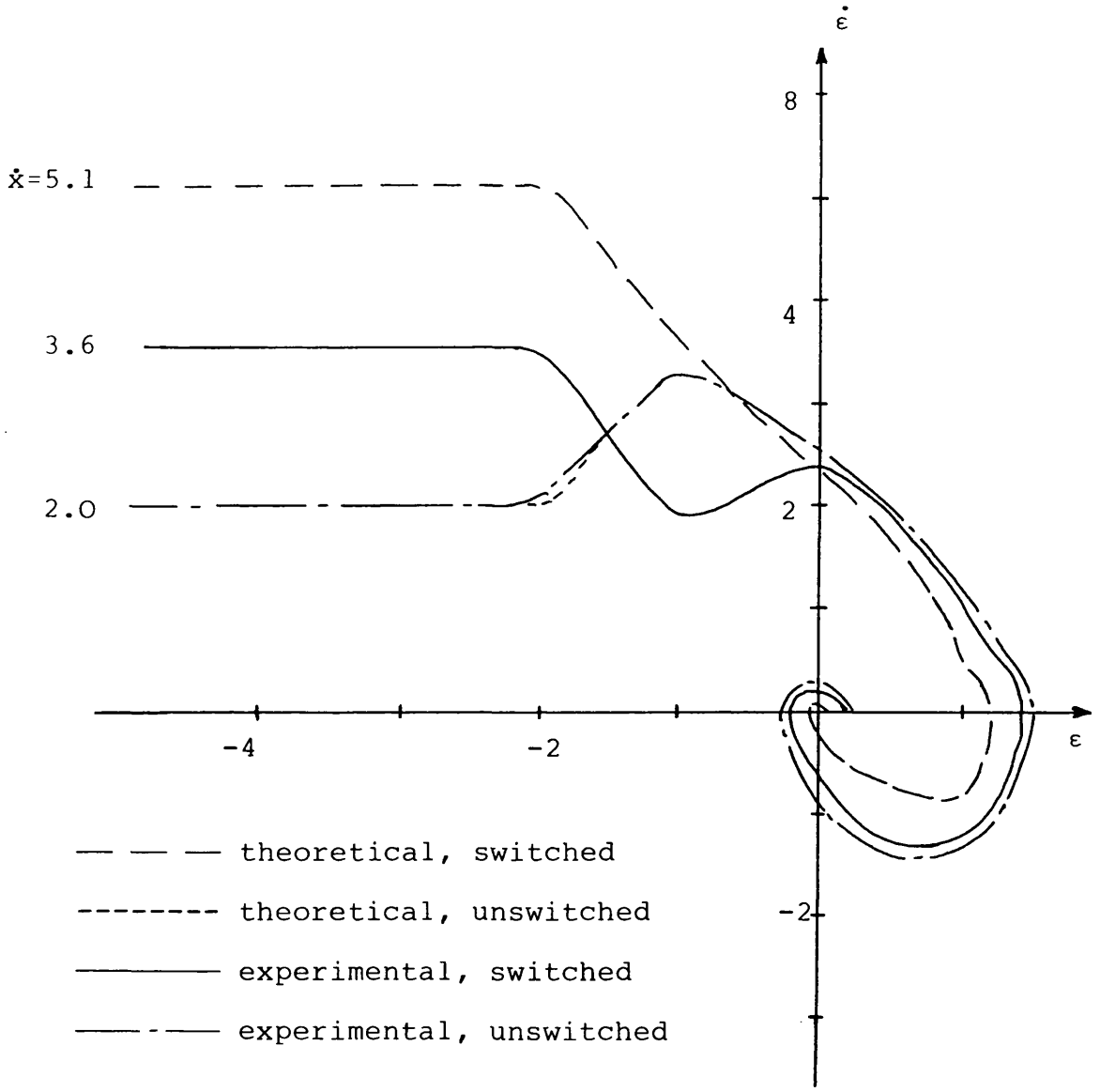
Table 3.1 Summarised maximum search rate for various delay lock loops

The experimentally determined acquisition trajectories of the standard 2Δ, 4Δ, 2-3Δ, and 1-3Δ loops are shown in Figure 3.20. It is clear that there is excellent agreement between the experimental trajectories and the theoretical trajectories, shown earlier and the maximum search rates are also in good agreement as shown in Table 3.1.

Using the analysis technique described earlier, the theoretical and experimental acquisition trajectories of the switched 2Δ, 4Δ, 2-3Δ, 3-2Δ and 1-3Δ loops were calculated and measured as shown in Figure 3.21. The maximum values of normalised initial search rate, $\dot{x}_{s\ max}$ are tabulated in Table 3.1. The maximum search rates found experimentally are slightly lower than those predicted theoretically. The reasons for this will be discussed in the next section. Nevertheless, there is an 80% improvement in the search rate of the 2-Δ loop and a 130% improvement in the search rate of a 3-2Δ loop when compared with the unswitched, or the standard version, in spite of an approximately 33% difference between the theoretical and experimental search rate. The switched 3-2Δ loop is over four times faster than the standard 2-Δ delay lock loop.

3.3.2 Comments on the Performance of Experimental and Theoretical Switched Loops

Figure 3.22 compares the theoretically predicted acquisition trajectories of switched and unswitched 2-Δ and 4-Δ delay lock loops with their corresponding experimental trajectories [26]. It is clear that the unswitched 2-Δ and 4-Δ loops give an experimental performance very close to that observed theoretically. However, the maximum initial search rate, leading to acquisition, the experimental

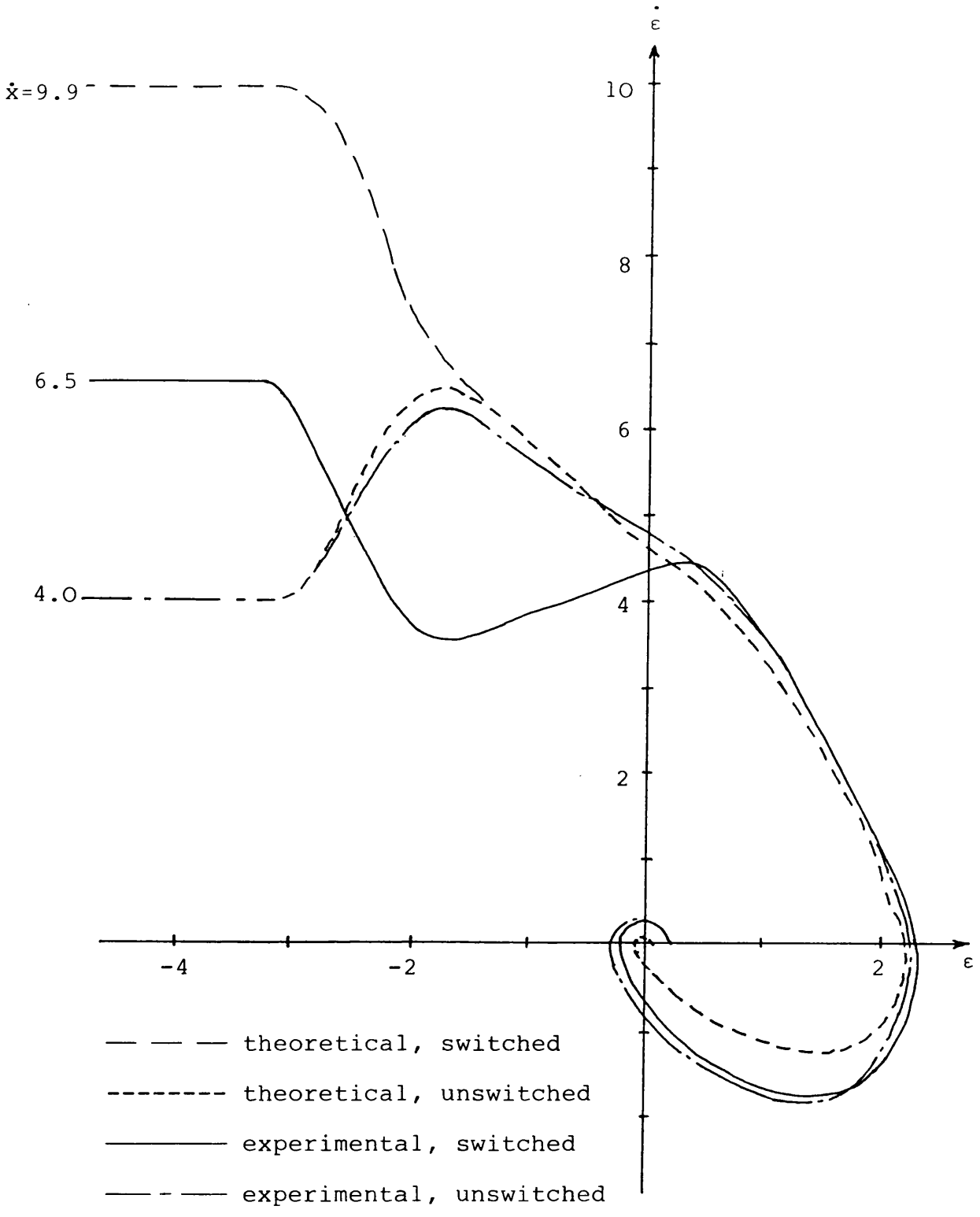


a)

Figure 3.22 Comparison of the acquisition trajectories of standard and switched loop

a) 2-Δ loop

b) 4-Δ loop



b)

Figure 3.22 Continued.

switched loop is less than the corresponding theoretical value. Considering the acquisition trajectories, both switched loops show a small degree of acceleration immediately after switch over, but their trajectories in the right half of the plane are almost identical to the unswitched and theoretical results, indicating that for a given damping factor ξ it is the value of $\dot{\varepsilon}$ at $\varepsilon=0$ (i.e. $\dot{x}$ at $x=0$) which is the critical parameter to ensure acquisition.

The causes of this acceleration in the experimental trajectories have been examined, and it is found that two main factors conspire to give the reduction in performance. The two major factors are:

i) Imperfect Correlation Statistics: The characteristics given in Figure 3.13 assume a very slow slip-rate. In practice, the slip-rate between the sequences may be quite high. This causes rounding of the discriminator characteristics. Ormondroyd and Comley [22] have shown that if the slip rate is in excess of 1.4 bit/sequence the correlation performance between sliding codes is significantly worsened with the injection of spurious correlations. Clearly in these high acquisition speed loops decorrelation effects become more important.

ii) Step Change: The time dependence of the error voltage and rate of change of error voltage of the experimental loop are shown in Figure 3.23. It is seen that immediately after switching the phase of the sequence $\overline{S_{i+1}}$ that the rate of change of the error signal increases momentarily. This corresponds to the slight acceleration of the search process in Figure 3.22. This is due entirely to the filtered step change in error voltage. Also the time taken to establish the new voltage level and the reponse of the voltage

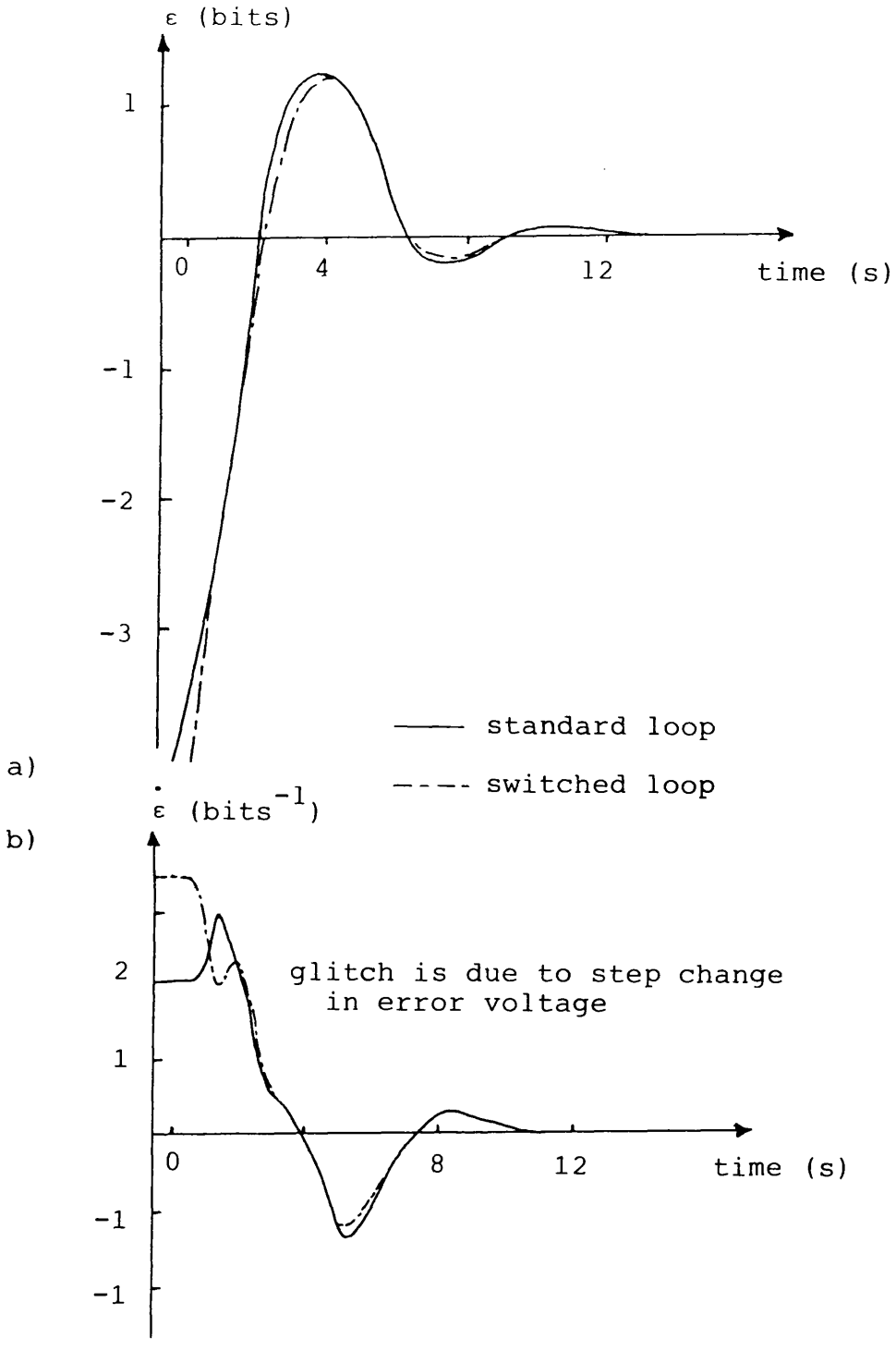
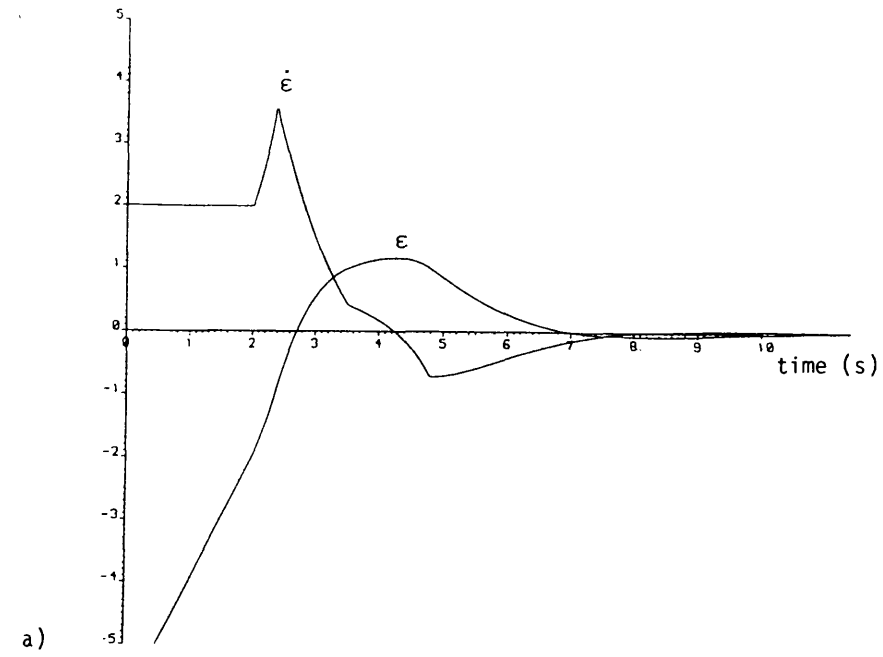


Figure 3.23. Experimental acquisition transients vs time for standard and switched 2-Δ delay lock loop.



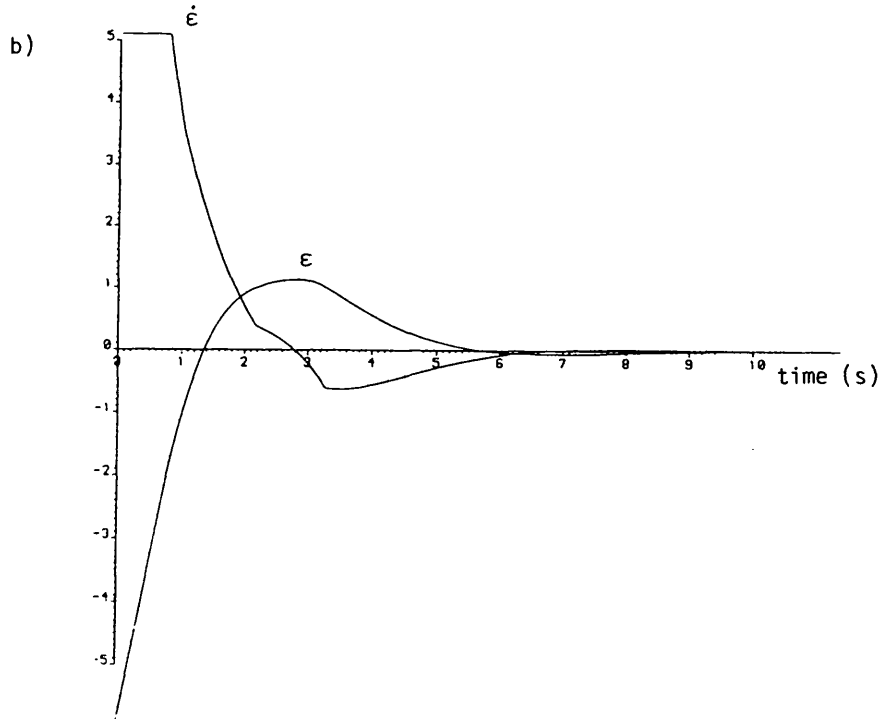


Figure 3.24. Theoretical acquisition vs time for a) standard 2-Δ loop, b) switched 2-Δ loop.

controlled oscillator. In the theoretical analysis, used in the comparison, the step change in the discriminator characteristic was not allowed for. This is confirmed by the theoretical transient values x and $\dot{x}$ shown in Figure 3.24. The reason for this is due to the lumped nature of the model which is assumed to be perfectly linear. The experimentally determined acquisition trajectories of switched 2Δ, 4Δ, 2-3Δ, 3-2Δ and 1-3Δ are shown in Figure 3.21.

3.3.3 Modified Switched Delay Lock Loop

It is possible to get the full benefit of the switched delay lock loop (in terms of maximum initial search rate) by a modification to the structure of the loop to remove the offset voltage after switching. The new loop is detailed in Figure 3.25 for the 2-Δ delay lock loop. The technique is applicable to other, wide-Δ and 1-Δ delay lock loops.

The difference between this loop and the switched loop, is the use of DPCO switch SW1, SW2 and a simple summing junction applied to the active loop filter to provide a level shifting network. The analogue voltage ($-V_o$) is generated by the peak hold/comparator circuit connected to the delay error output from the loop, as shown in Figure 3.26.

The operation of the loop is as follows. When the loop is acquiring initial synchronisation, sequence S_{i+1} is inverted to give the discriminator characteristic of Figure 3.13 (b), as before. This is achieved by the state of switch SW1. At the same time the state of switch SW2 ensures that 0V level offset is fed to the level shifting network in the loop filter and the voltage controlled oscillator idles at a slightly higher frequency than the clock

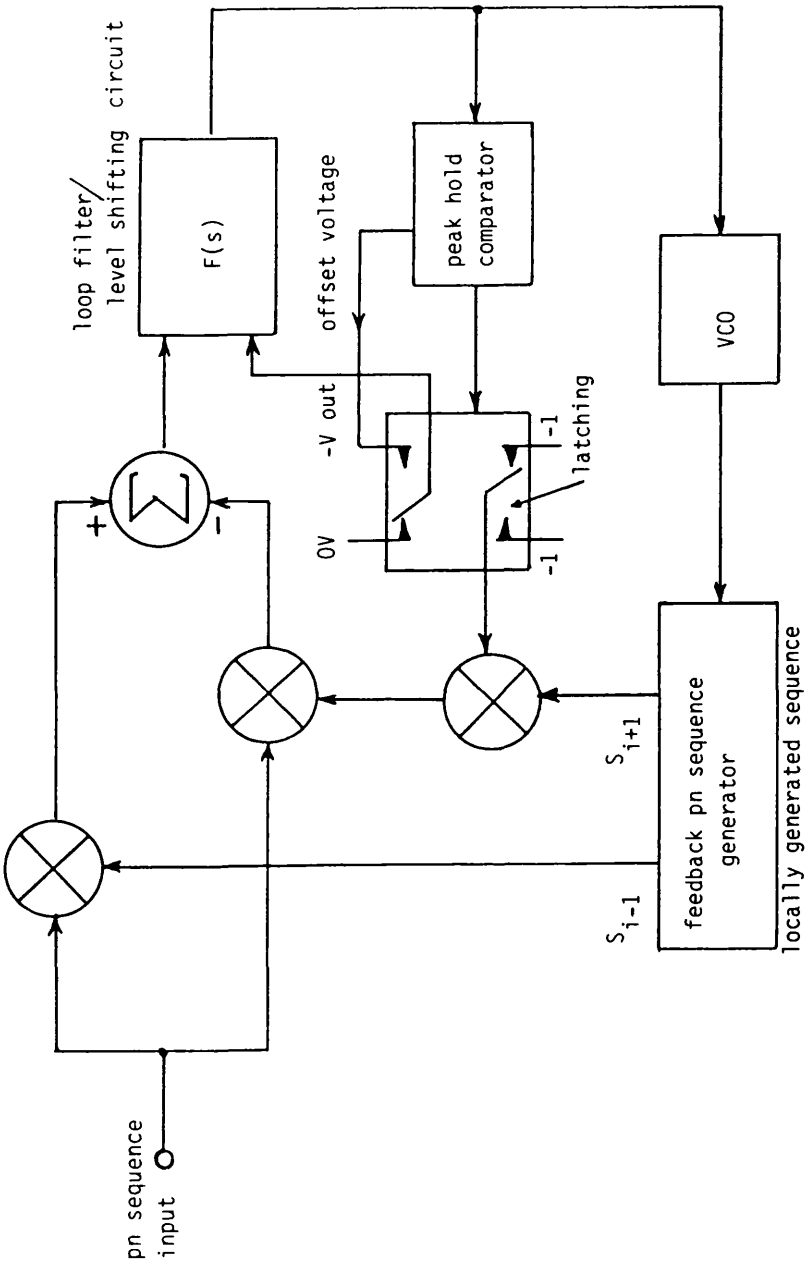


Figure 3.25. Schematic circuit diagram of a modified 2-Δ DLL.

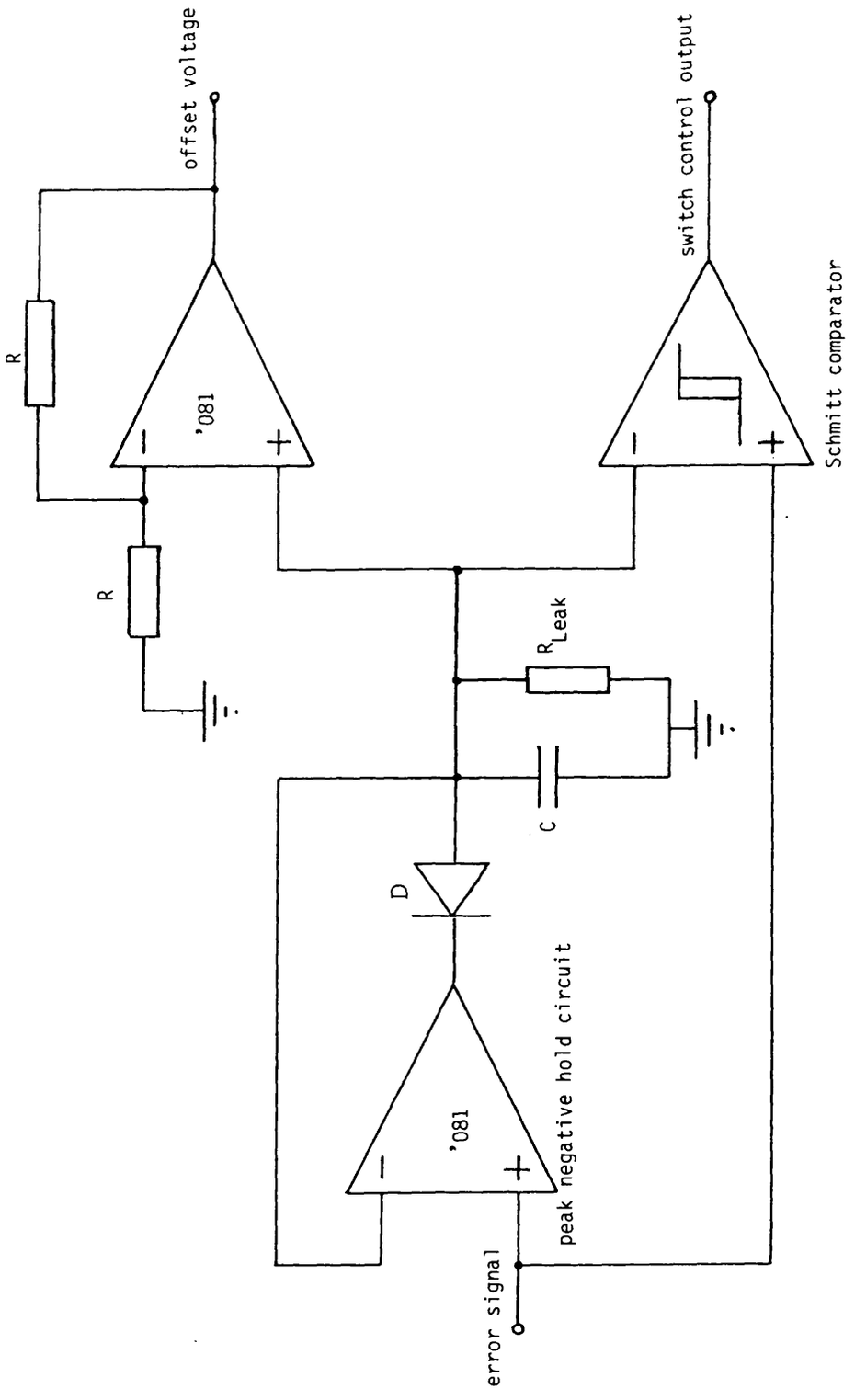


Figure 3.26. Peak hold/comparator circuit.

frequency of the received sequence to perform the epoch search. During acquisition the delay error voltage is reduced and the voltage controlled oscillator frequency reduces towards that of the received sequence. When the sequences are within 1 bit of synchronisation the delay error voltage starts to rise. At this point the peak hold/comparator circuit changes state, switching over the states of SW1 and SW2. Switching SW1 causes the sequence $\overline{S_{i+1}}$ to revert to its normal non-inverted state, and the discriminator characteristic changes to that shown in Figure 3.18(a). At the same time $-V_o$ is fed to the level shifter. $-V_o$ is twice the value of the peak hold voltage at changeover and this corresponds exactly to the change in mean level of the discriminator characteristics. The result is that the step offset which occurs in the original switched loop no longer occurs and there is no acceleration in search velocity after switchover.

Figure 3.27 compares the experimental and theoretical acquisition trajectories at the modified switched 2-Δ and 4Δ delay lock loops. It is clear that there is now negligible difference in performance between experimental and theoretical loops.

The modified loop requires little more hardware than the switched loop because for automatic operation of the loop the peak hold/comparator circuit would be required anyway, and SW1, SW2 are both situated in one integrated circuit.

The modification has an associated benefit. Offsetting the voltage controlled oscillator to cause the loop to search the sequence epochs can cause a small amount of loop stress [23] which prevents exact phase synchronisation if the loop gain is small. For

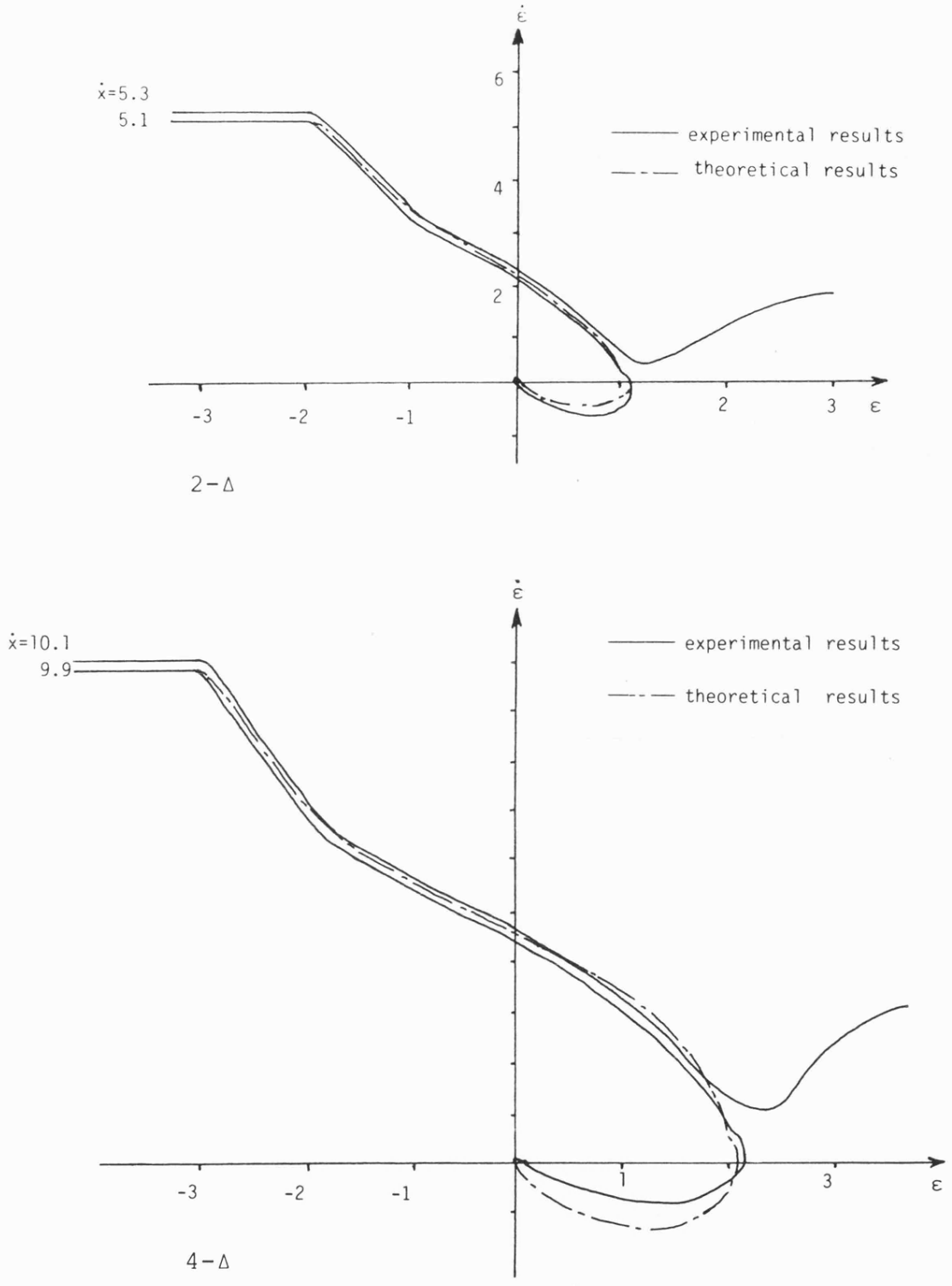


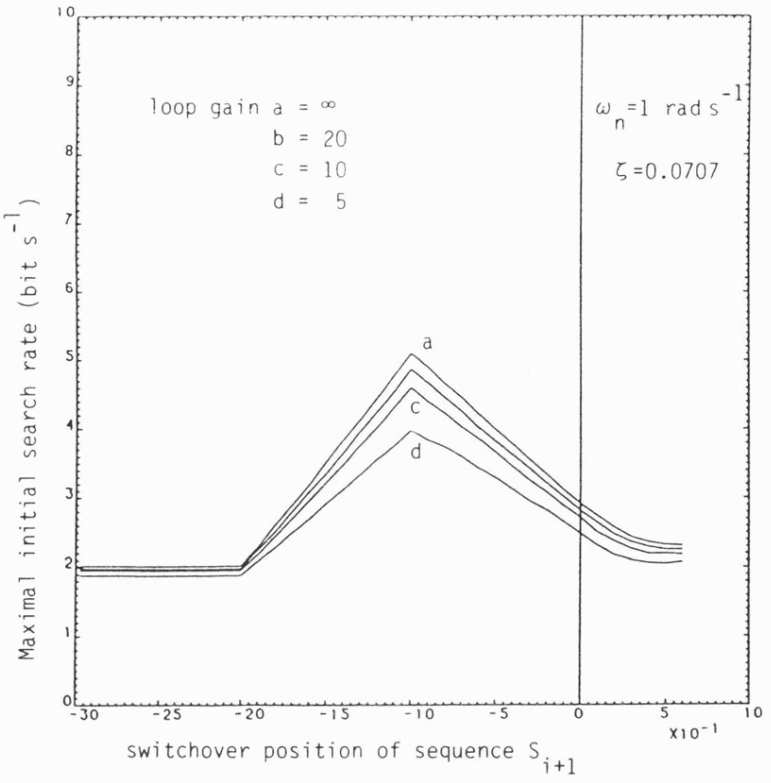
Figure 3.27. Theoretical and experimental acquisition trajectories of modified switched delay lock loop.

most systems loop stress would not be a problem, if however, very accurate phase synchronisation is required it is necessary to remove the loop stress. The addition of the offset voltage $-V_o$ can be used to counter the built-in loop stress of the delay lock loop.

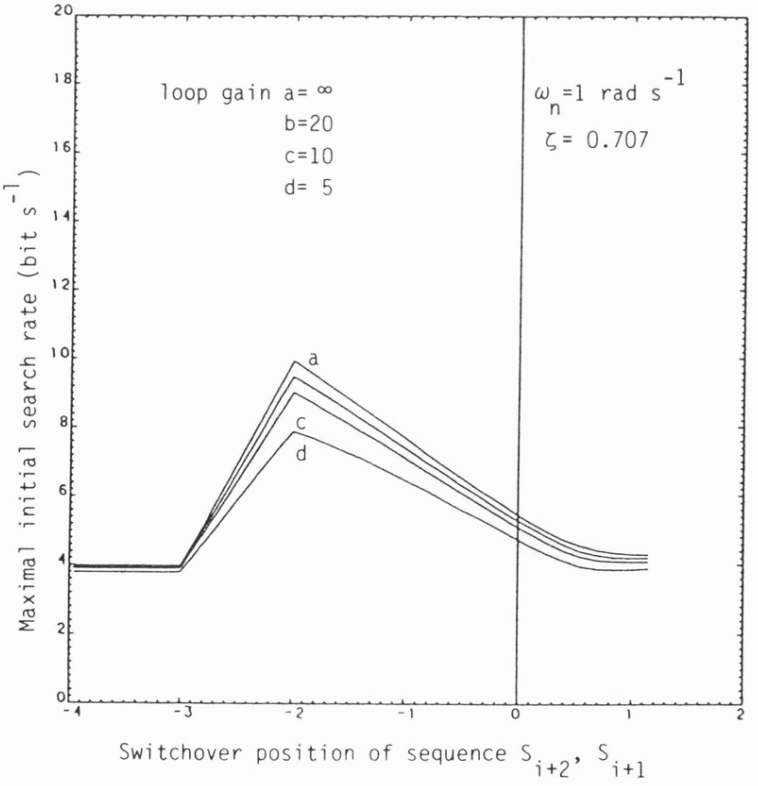
3.3.4 Effect of Switchover Position and Gain on the Value of Maximum Initial Search Rate

The maximum initial search rate is dependent upon the relative phase between the sequences when $\overline{S_{i+1}}$ is inverted. Figure 3.28 shows the effect of switchover position of $\overline{S_{i+1}}$ on the maximum search rate of 2-Δ and 4-Δ delay lock loops, corresponding to the acquisition of lock. The phase reference is with respect to the in-lock condition. It is clear that the maximum search rate is achieved when the codes are switched over at the peak negative value of the discriminator characteristics. Although not shown, this was found to be true for all the loops tested, including the asymmetric n-mΔ delay lock loops, except the switched 1-Δ loop. The reason for this is because at this switchover position the discriminator characteristic has no positive slope. If the loop is switched at any other relative phase the discriminator characteristic has a region of positive slope and a consequent acceleration of the search process during pull-in.

Also shown in Figure 3.28 is the effect of the loop gain, G, and the maximum search rate as a function of switchover position. It is apparent that reducing the gain reduces the maximum initial search rate (The natural frequency ω_n and the damping factor ξ are maintained constant at 1 rad/sec and 0.707 respectively). This is expected since the amplitude of the N-shaped error curve is affected by the value of the gain. The smaller the gain the less the amplitude.



a) 2-Δ DLL



b) 4-Δ DLL

Figure 3.28 Effect of the switchover position of the sequence $S_{\overline{i+1}}$ on the maximum rate a) 2-Δ DLL, b) 4-Δ DLL

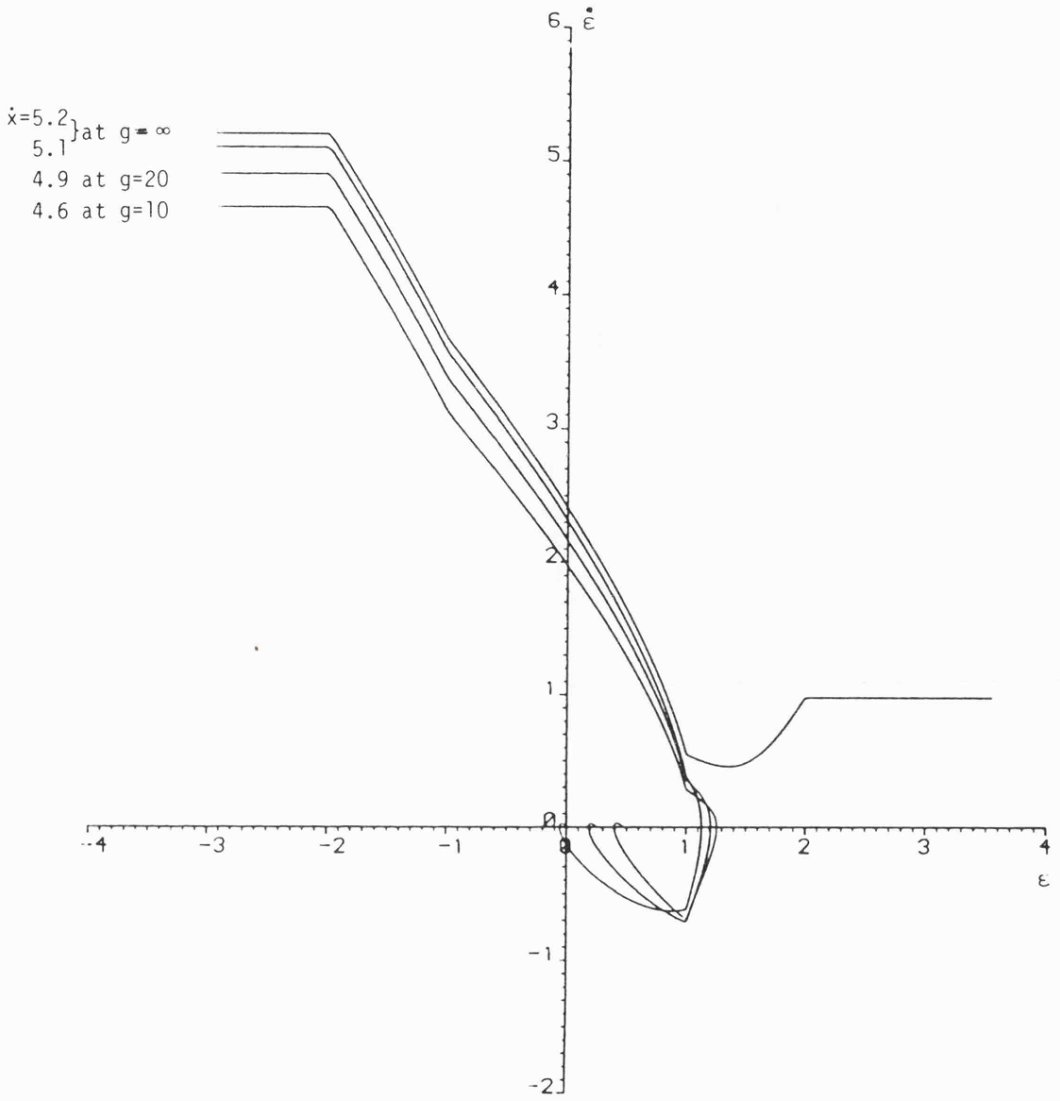


Figure 3.29. Theoretical acquisition trajectories of modified switched DLL for different loop gain.

In turn a small reduction of the negative peak amplitude value causes the maximum search rate to reduce by a small amount as well, because it reaches a value which is slightly above the threshold value when the switch changes over. For the standard delay lock loop, it was found by Spilker and Neilsen [10, 21] that the maximum initial search of the delay lock loop is approximately the same for $G = \infty$ and $G = 10$. The reason is that the reduction of the positive peak is considered to be an advantage as explained earlier, but the reduction of the negative peak is a disadvantage, and it seems to cancel the effect of the other keeping the maximum initial search rate the same as for a high gain delay lock loop.

Similarly increasing the damping ratio is also expected to increase the maximum search rate, from which lock may be ultimately achieved. This problem will be considered in the next section.

Figure 3.29 shows the effect of loop gain g on the acquisition trajectory of the modified switched DLL. The results have similar characteristics to those considered earlier.

3.4 FURTHER MODIFICATIONS TO THE DELAY LOCK LOOP

3.4.1 Effect of Damping Ratio on Maximum Initial Search Rate

It is obvious from equation 3.11 that the loop gain and the damping ratio have an effect on the acquisition trajectory of a delay lock loop. Traditionally, a damping ratio of $\xi = 0.707$ is considered an optimum value for delay lock loop design because it enables the loop to pull in quickly and track step changes in delay error with minimum overshoot. However, this value does not necessarily optimise the maximum initial search rate of the loop prior to pull-in. As the search time is very much longer than the pull-in time it is necessary

to optimise the search rate, even if this is at the expense of the pull-in time. Holmes [12] has suggested that one method of achieving this improvement is to maintain ξ=0.707 but allow ω_n to have a high value during acquisition, which is slowly reduced after lock has been achieved. This has the obvious disadvantage that the loop has a wide noise bandwidth during acquisition, which significantly reduces the probability of acquiring lock [27]. A further disadvantage is that this type of loop can be forced out of lock by switching ω_n too quickly. Although increasing the damping ratio ξ may also worsen the noise bandwidth, to some extent there is a region of where the noise bandwidth is hardly affected as shown in figure 3.30 [23,28]. It is seen that the noise bandwidth B_L has minimum value for ξ=1/2, in which case B_L/ω_n = 1/2. For the commonly used damping ratio of ξ=0.707, B_L/ω_n = 3/4 $\sqrt{2}$ = 0.53. Between the limits of $0.3 < \xi < 1.3$ the loop bandwidth never exceeds its minimum value by more than 40 per cent (less than 2-dB noise power). B_L, ω_n, and ξ are related to each other by the relationship [23].

$$B_L = \frac{\omega_n}{2}\left(\xi + \frac{1}{4\xi}\right) \text{ Hz} \qquad 0 < \omega < \infty \qquad 3.14$$

Using the computer simulation of the acquisition behaviour of the delay lock loop, described earlier, it was found that the maximum initial search rate is approximately proportional to the damping ratio. As a consequence a technique alternative to modifying ω_n is to increase the damping ratio of the loop during acquisition phase, and to change it back to ξ= 0.707 after lock, without affecting ω_n.

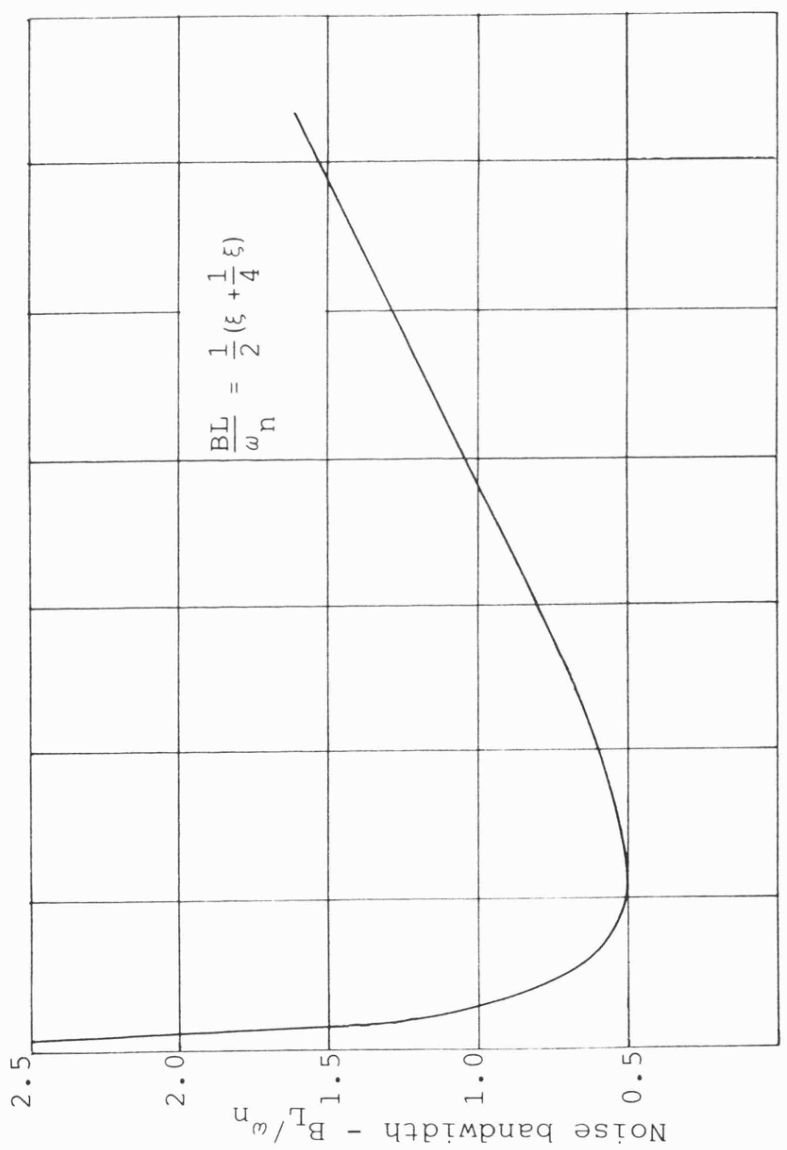


Figure 3.30. Loop-noise bandwidth (for high-gain, second order loop)

In the first instance, the technique is applied to a standard delay lock loop configuration.

3.4.2 Application of a Switched Active Filter to a Standard Delay Lock Loop

Figure 3.31 shows the technique applied to a ranging receiver. The natural frequency of the loop is given by:

$$\omega = \left[\frac{G}{R_1 C}\right]^{\frac{1}{2}} \text{ rad/sec} \qquad 3.15$$

and the damping ratio is:

$$\xi = \left[\frac{R_2 C}{2}\right] \omega_n \qquad 3.16$$

The loop natural frequency depends entirely on the dc gain (G) and the filter cut off frequency ω_{LPF} ($=1/R_1 C$). This is kept constant throughout the acquisition process. However, the damping ratio can be modified by altering the value R_2 by means of the switched resistor R_3.

During initial acquisition the damping ratio is high and the maximum search rate is high. The switch, SW, is controlled by the simple pulse rate discriminator or diode pump circuit which detects when the locally generated sequence, S_i is in phase with the received sequence. Thus once lock is achieved the switch is closed and R_2 is reduced to a value appropriate to $\xi = 0.707$ so that advantage can be taken of the lower damping ratio when the loop is in lock.

When using this technique it was found that it was possible to switch ξ abruptly before lock had occurred. However, to ensure

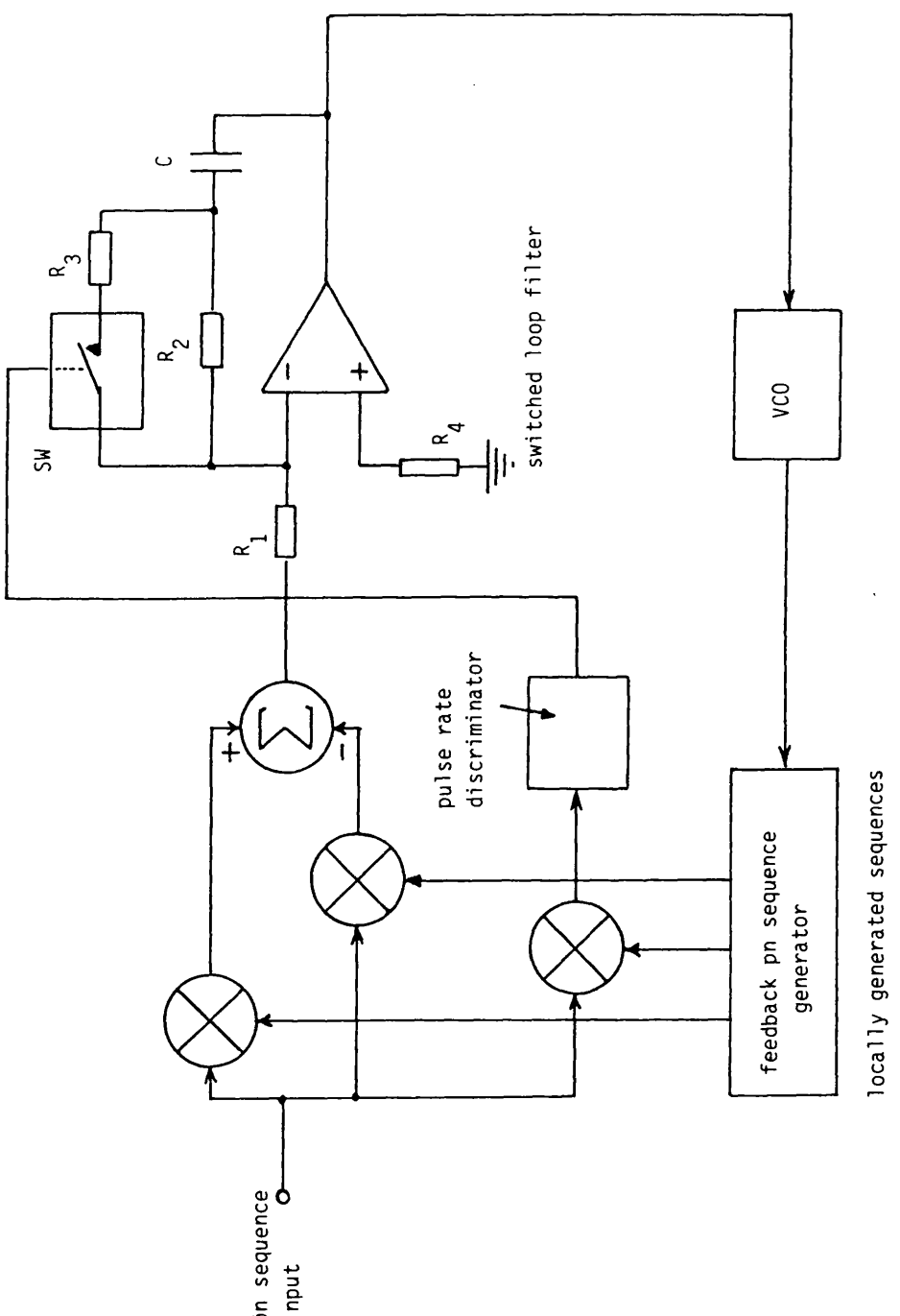


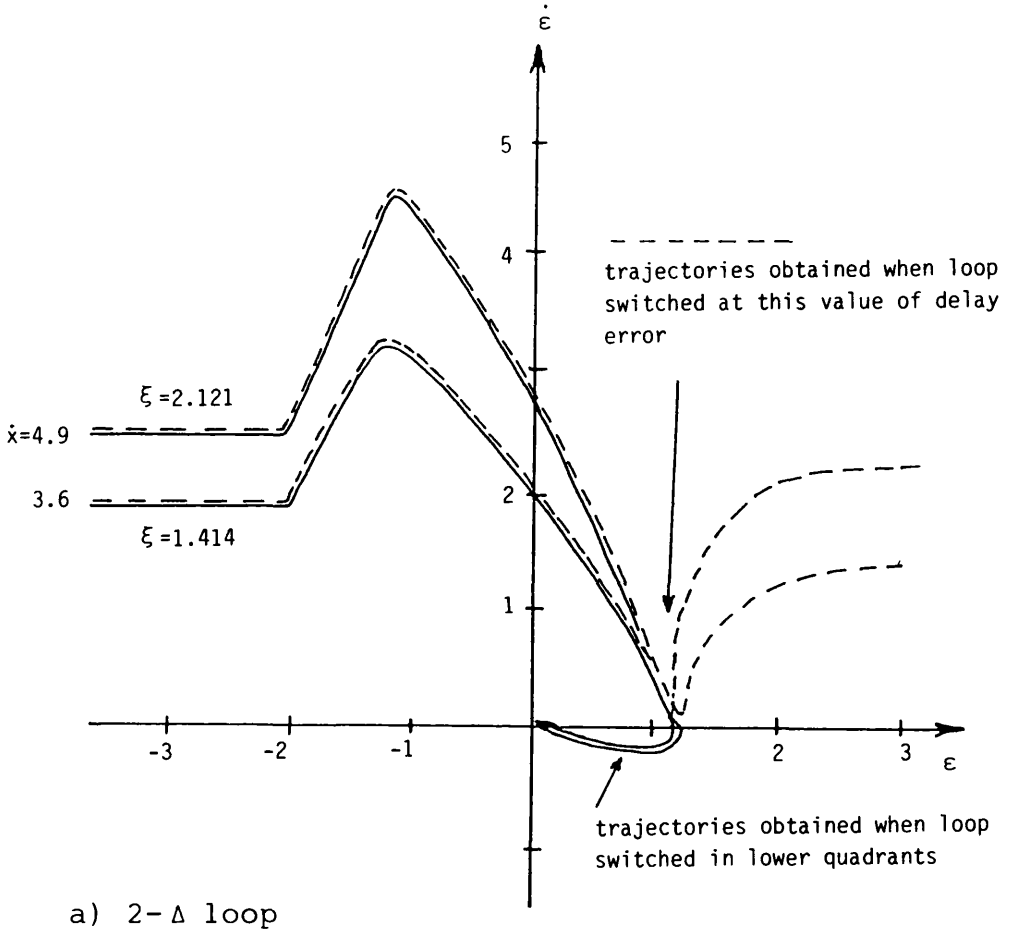
Figure 3.31. Schematic circuit diagram of 2-Δ DLL using switched active filter

subsequent locking of the loop it was necessary to switch the value of ξ when the trajectory was in the lower quadrants of the phase plane. When the initial search rate was at the maximum allowed it was not possible to achieve lock if ξ was switched in the upper quadrants of the phase plane. Nevertheless the fact that ξ may be switched abruptly, is a significant advantage over switching ω_n slowly.

Figure 3.32 shows the experimental acquisition trajectory for the maximum initial search rate of switched filter 2-Δ and 4-Δ delay lock loops for damping ratios of 1.414, and 2.121. The theoretical results are in **very** close agreement. The solid curves represent the trajectories for the case where the filter is switched in the lower quadrants of the phase plane and the dashed curves show the effect of reducing the damping ratio just before the trajectory enters the lower quadrant for the same initial rate. Lock is not achieved. It is also clear that the maximum initial search rate is significantly higher for a high value of damping ratio.

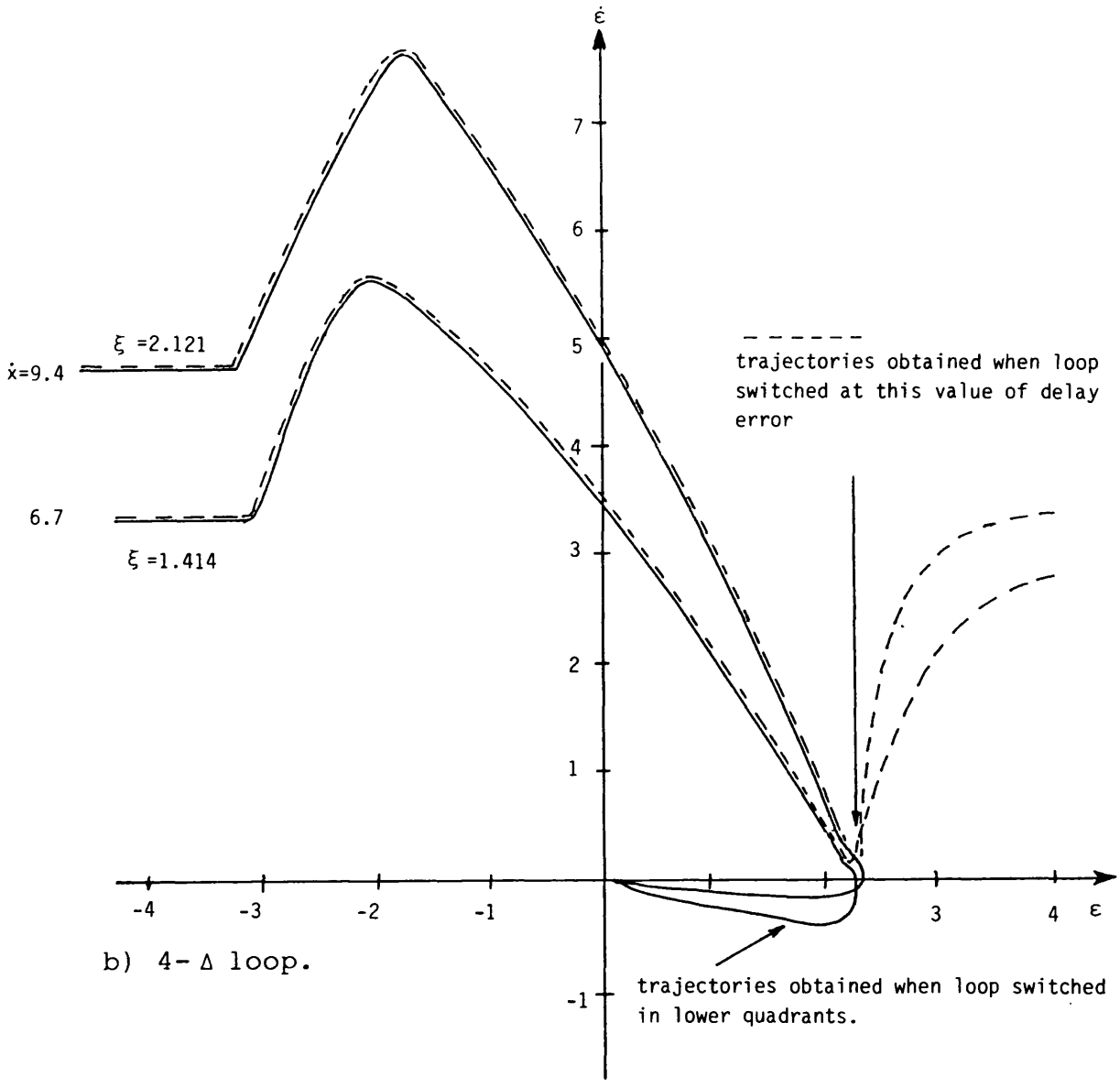
Figure 3.33 compares the theoretical and experimental maximum search rates as a function of the initial value of damping ratio for the 2-Δ and 4-Δ switched filter loops. The difference between theoretical and experimental results is due to slight non-linearities in the voltage controlled crystal oscillator of the delay lock loop.

Although the pull-in time of the delay lock loop increases with high damping ratios, this increased locking time can in no way be compared with the very long acquisition time which is actually reduced considerably by this technique.



a) 2-Δ loop

Figure 3.32. Experimental acquisition trajectories for maximum initial search rate of a switched filter DLL for ξ=1.414, 2.121



b) 4- Δ loop.

Figure 3.32 Continued.

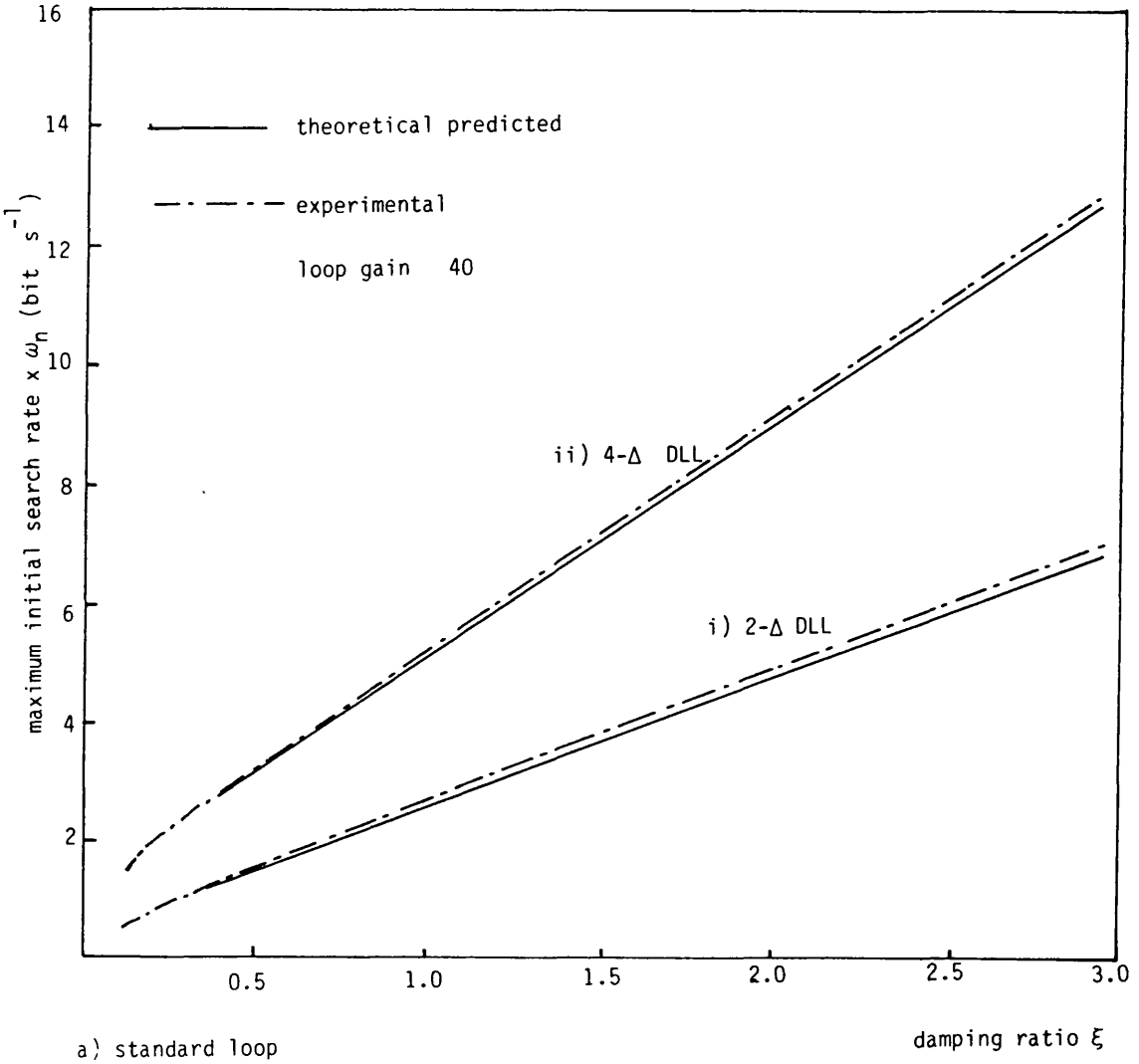
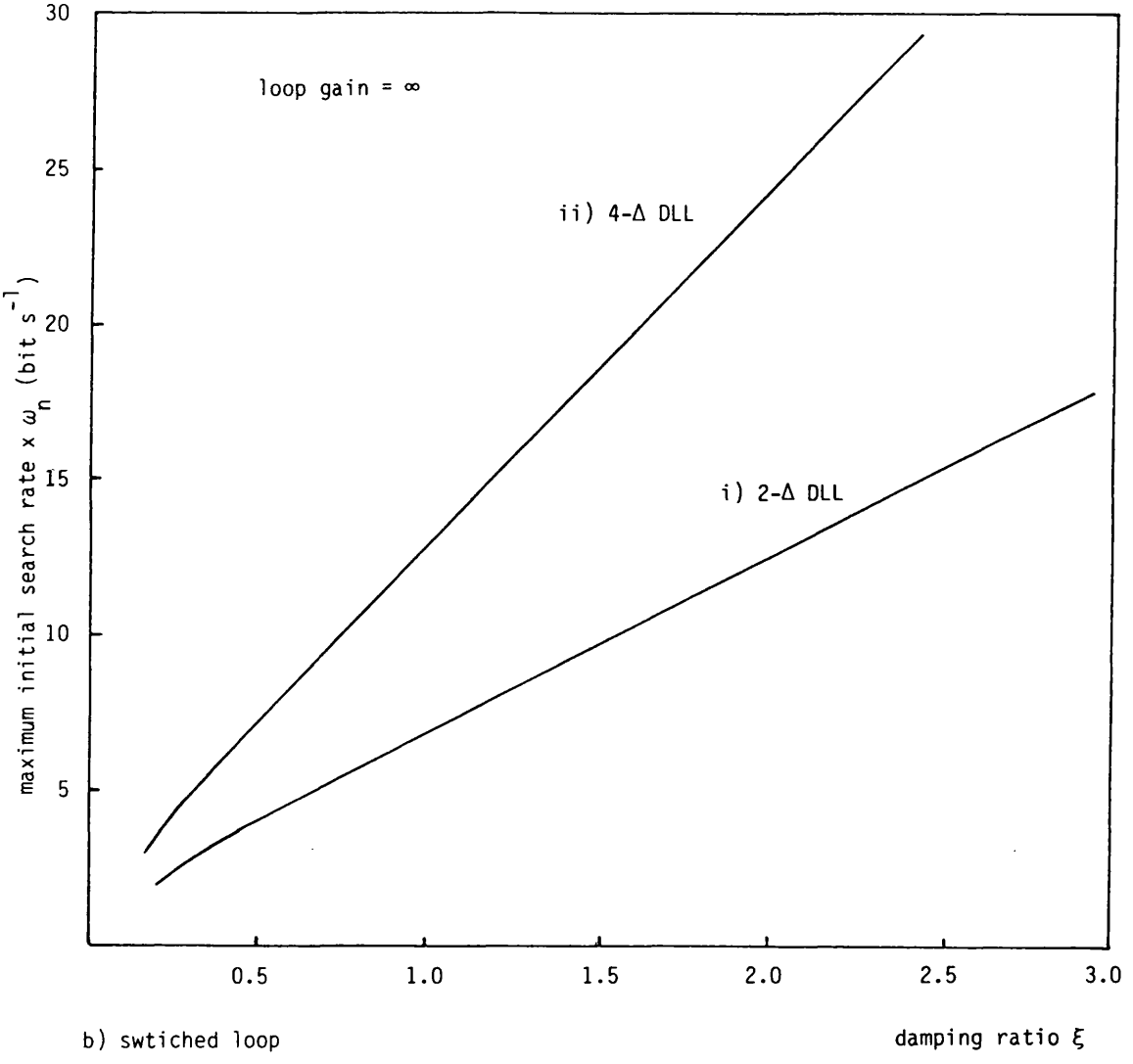


Figure 3.33. Comparison of the theoretical and experimental values of maximum initial search rate as a function of damping ratio for 2-Δ and 4-Δ DLL

a) Standard loop

b) Switched loop



b) swtiched loop

Figure 3.33. Continued.

3.4.3 Application of Switched Active Filter to a Modified Switched Delay Lock Loop

Figure 3.34 shows a schematic diagram of the application of the switched loop detailed in Section 3.3.3. As in the previous section the pulse rate discriminator controls the value of damping ratio used around the loop, whilst the DPCO switch controls the state of the sequence S_{i+1} and the offset voltage applied to the delay lock loop.

During acquisition the normal state of the loop is with zero offset voltage, large damping ratio and the sequence S_{i+1} in inverted mode. When the discriminator reaches its maximum negative value the loop discriminator characteristic is switched without affecting the damping ratio. When the loop is locked the damping ratio is finally switched to its normal value of 0.707.

The technique has been implemented experimentally for 2-Δ and 4-Δ delay lock loops. Figure 3.35 shows the experimental acquisition trajectories for the case of the maximal initial search rate for three cases of initial damping ratio. It is seen that the maximum initial search rate is now substantially above the corresponding standard loop (typically 6.5 times the original maximum initial search rate for an initial damping ratio of 2.121). Although not plotted the theoretical results are in excellent agreement with the experimental results.

It should be noted that the switched filter was only incorporated in the modified switched loop, discussed in Section 3.3.3 rather than the simpler switched loop described in Section 3.3.1. It was found that increasing the damping ratio in the switched loop of Section 3.3.1 caused a marginal worsening of the

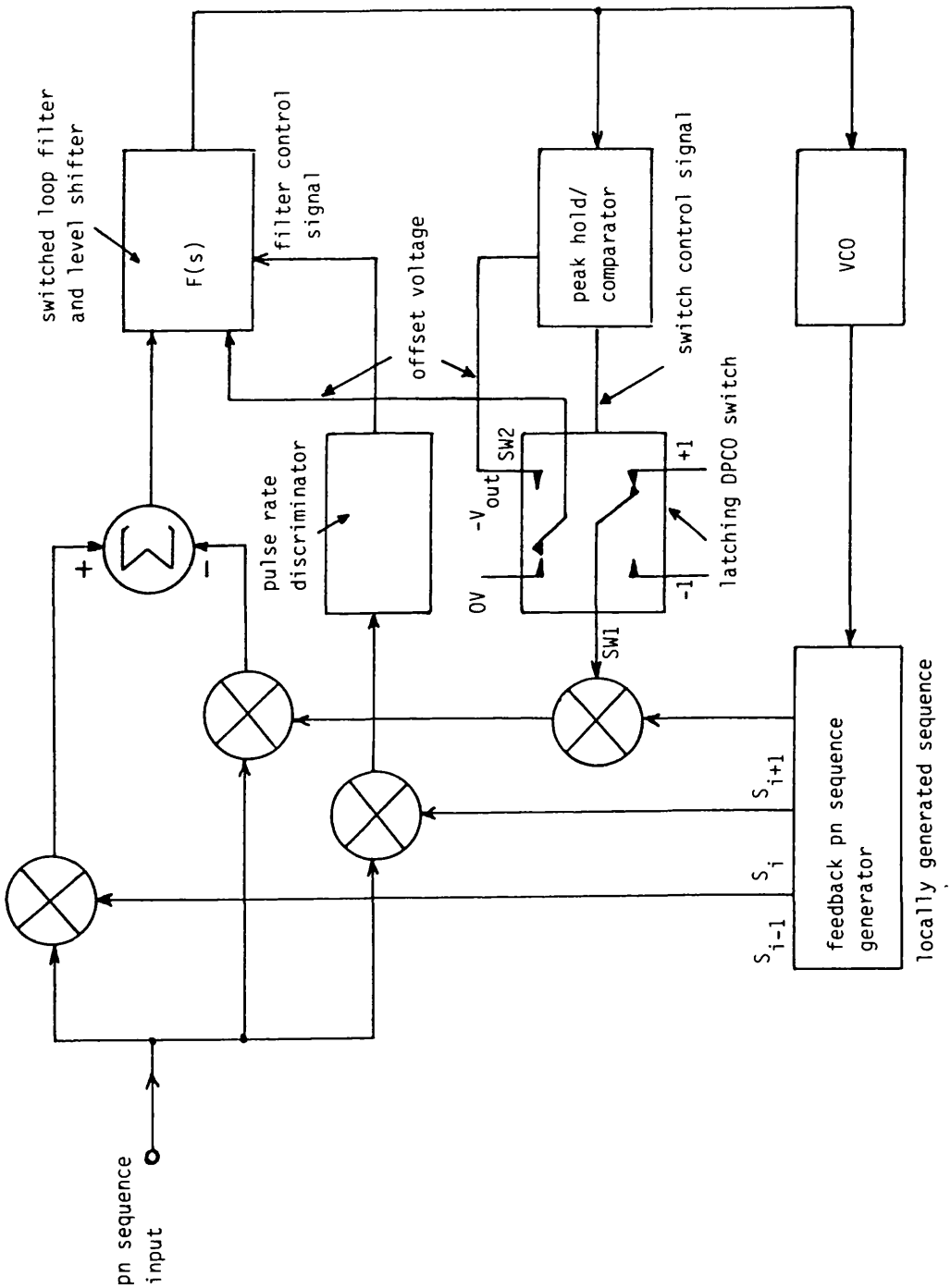


Figure 3.34. Schematic circuit diagram of a modified switched 2-Δ DLL employing active filter switching.

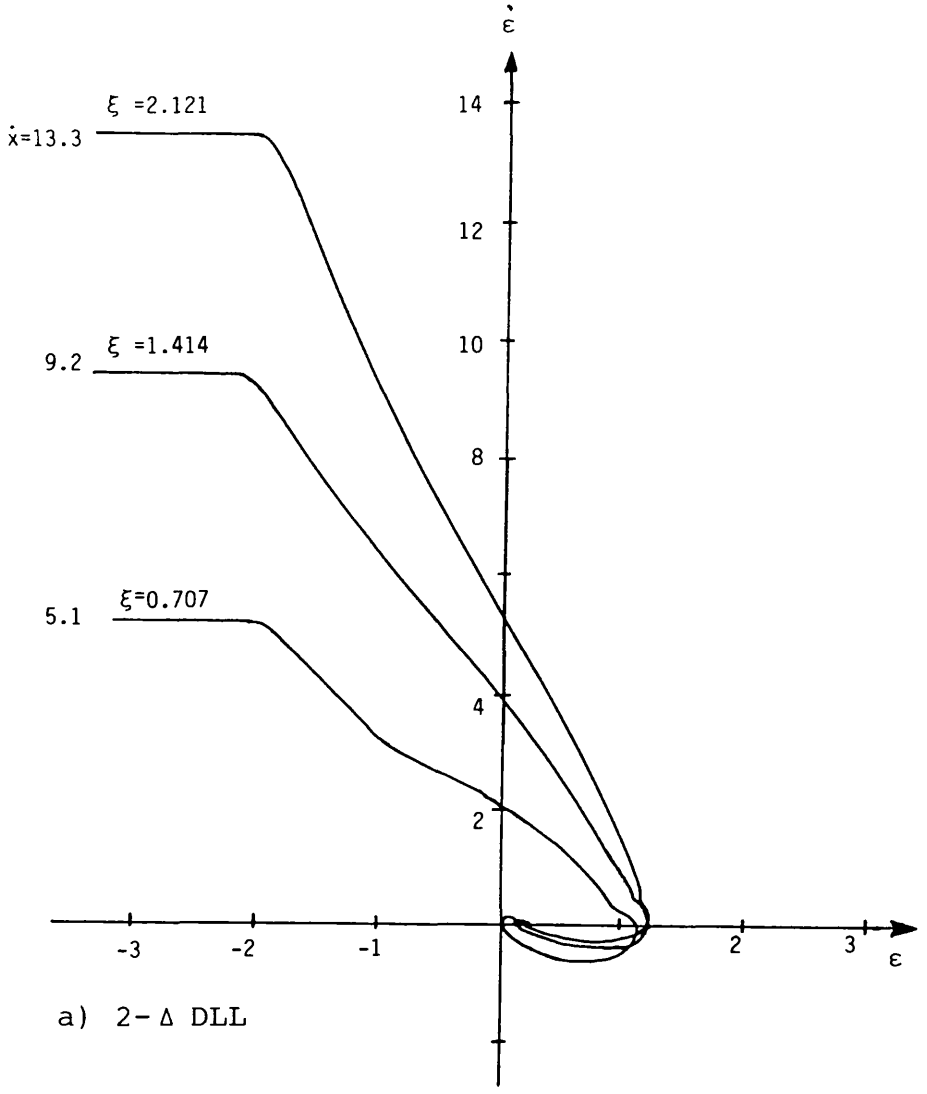
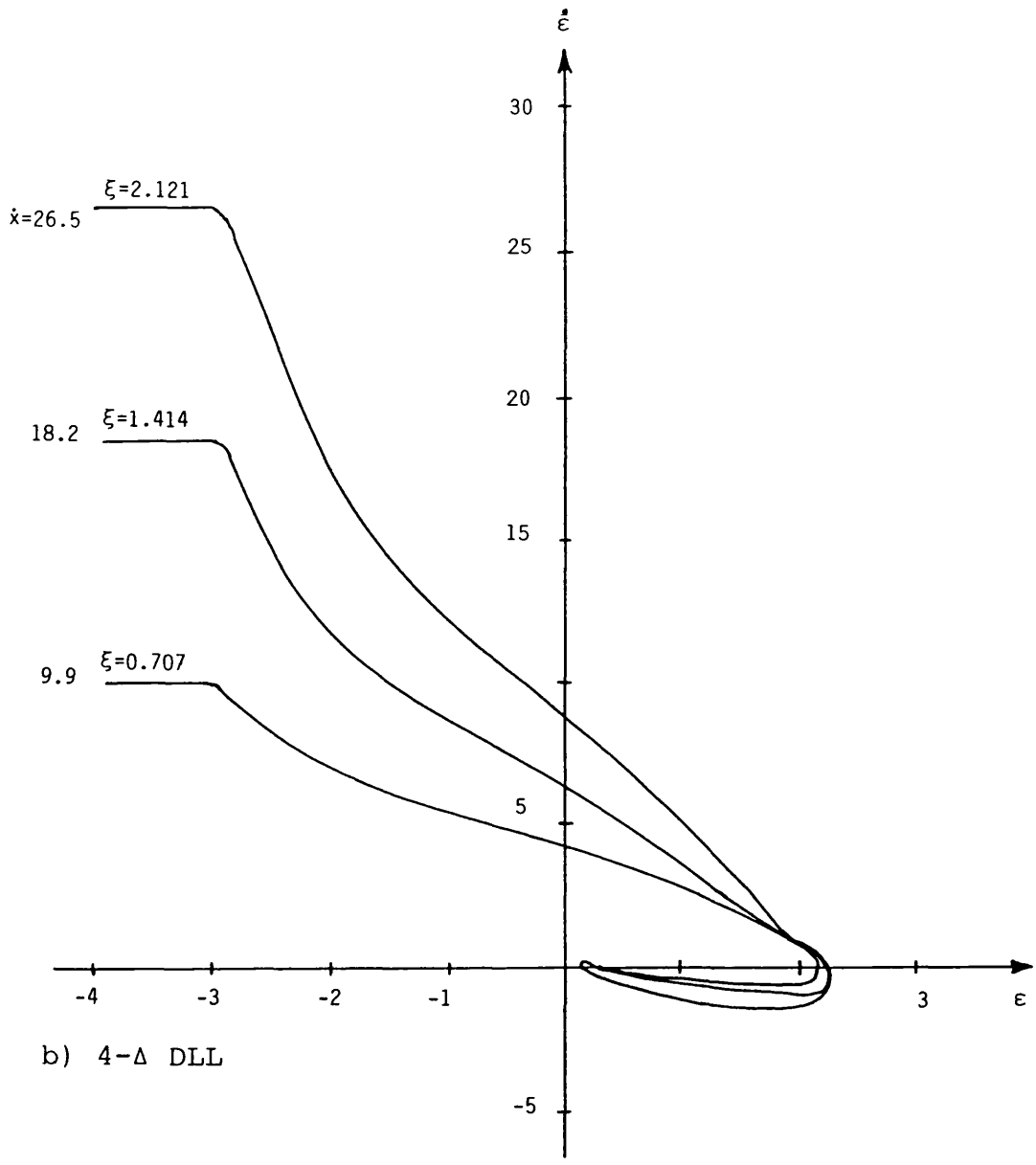


Figure 3.35. Experimental acquisition trajectories of the modified switched loop with switched active filter for three initial values of damping ratio.

a) 2-Δ DLL

b) 4-Δ DLL



b) 4-Δ DLL

Figure 3.35 Continued.

maximum search rate. This is due to the effect of the filter on the step change in discriminator characteristics. Modification of the filter parameters modifies the proportion that the discriminator characteristic has a negative slope relative to a positive slope and this reduces the maximum initial search rate. By removing the step change full advantage of the switched filter could be taken.

For the 2-Δ delay lock loop the maximum normalised initial search rate increased from 5.1 at $\xi=0.707$ damping ratio to 9.2 and 13.3 at $\xi=1.414$ and $\xi=2.121$ damping ratio respectively.

It will be seen that there is an increase of x4.1 in the search rate for every 0.707 increase in the damping ratio. For the 4-Δ loop the maximum slipping rate reaches 18.2 and 26.5 at 1.414 and 2.121 damping ratio respectively instead of 9.9 at 0.707 damping ratio. There is also an increase of about x8.2 in search rate for each 0.707 increase of the damping ratio.

Figure 3.36 shows the effect of sequence switchover position on the maximum search rate as well as the effect of the loop gain G and the damping ratio ξ for both 2-Δ, 4-Δ delay lock loops.

Several points are found in these plots:

a) The maximum search rate is affected by the damping ratio more than the gain, for both switched loops, where switchover SW = -2.0 to 0.5. for 2-Δ loop, SW = -3.0 to 1.0 for 4-Δ loop, and standard loop, where SW < -2.0 for 2-Δ loop, SW < -3.0 for 4-Δ loop.

b) The gain has a very small effect on the maximum search rate for the standard loop, while it has some effect for the switched loop.

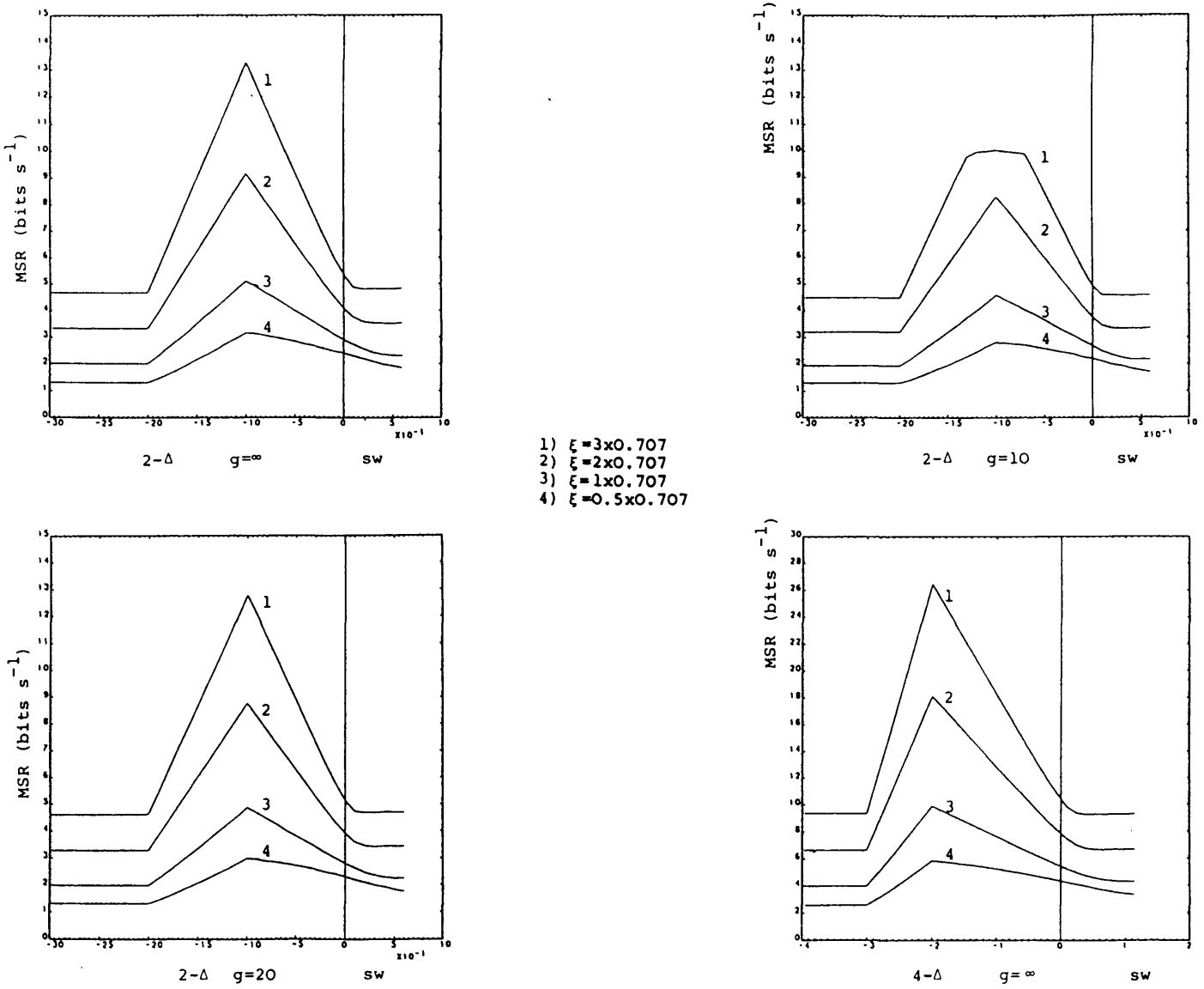


Figure 3.36. Effect of the switchover position of S_{i+1} , s_{i+2} on the maximum search rate of 2-Δ and 4-Δ DLL.

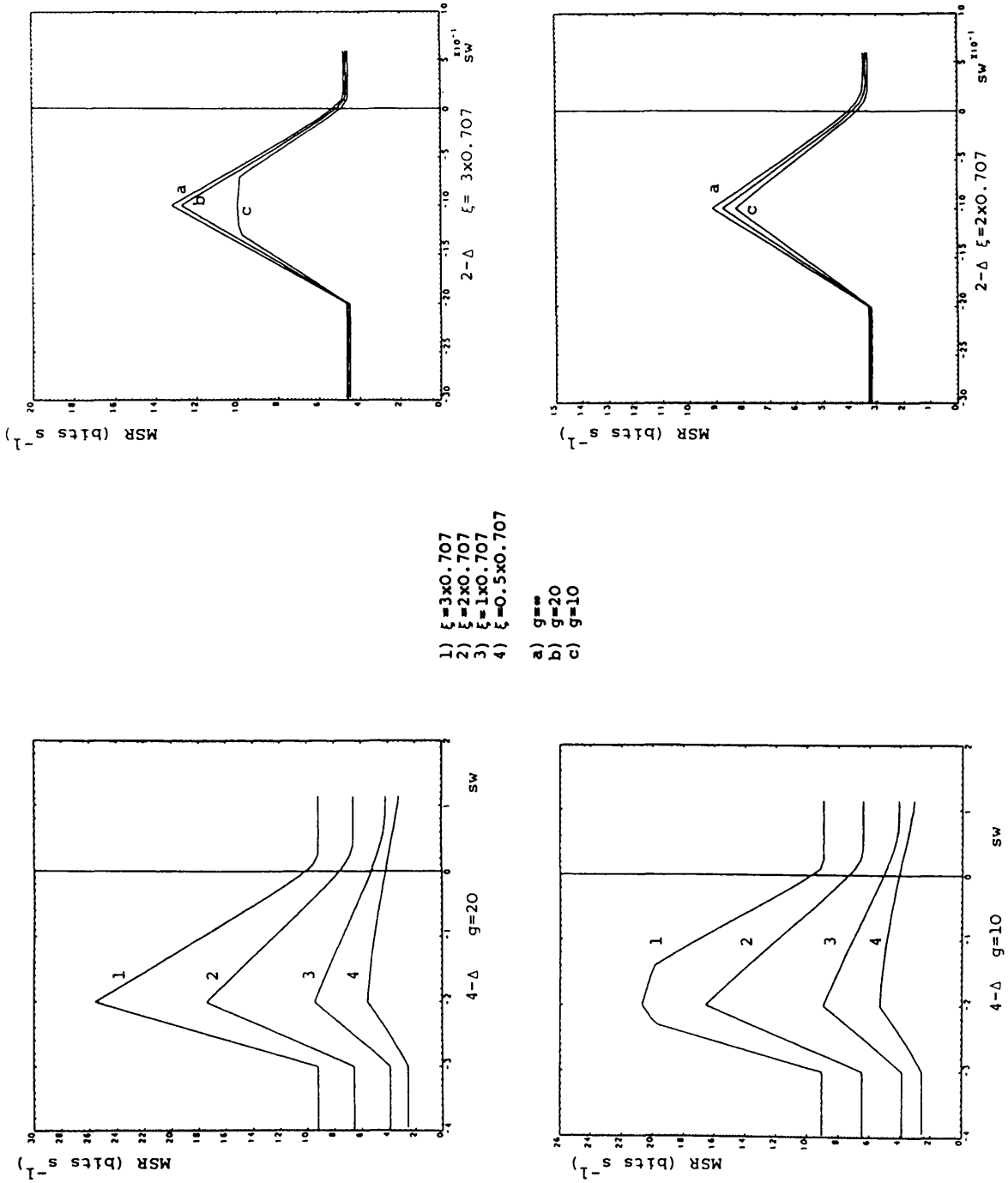


Figure 3.36 Continued.

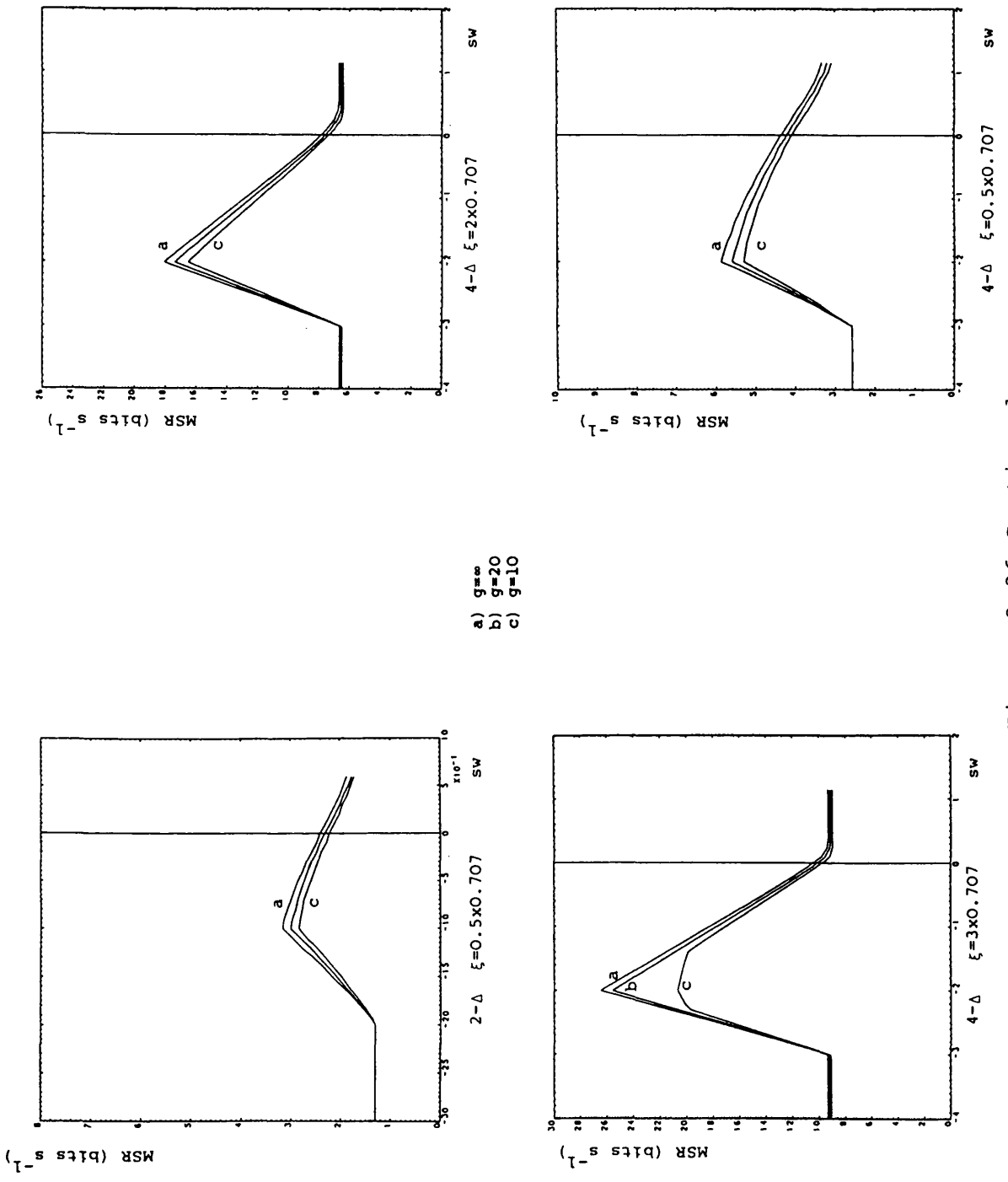


Figure 3.36 Continued.

c) The damping ratio has a significant effect on the standard loop, and also a larger effect on the switched loop.

d) For the switched loop the maximum search rate, in the region of SW = -1.0 to 0.5, for 2-Δ loop and SW = -2.0 to 1.0 for 4-Δ loop is higher than that in the region of SW = -1.0 to -2.0 for 2-Δ loop and SW = -2.0 to -3.0 for 4-Δ loop respectively.

e) For the case were the gain G is low (g=10) and the damping ratio is high (ξ = 3 x 0.707) the maximum search rate falls below the expected value for the switched loop near SW = -1 for 2-Δ loop and SW = -2 for 4-Δ loop. In fact after careful examination of this particular case, it was found also that the synchronisation point is not near the origin of the phase plane plot where $\varepsilon \approx 0$, but near $\varepsilon \approx 1$ for 2-Δ loop and $\varepsilon \approx 2$ for 4-Δ loop. The reason for this is that the value of the rate of change of the error voltage reduced very sharply causing the loop to stay at this point for a very long time.

3.5 EFFECT OF THE WIDTH OF THE DISCRIMINATOR CHARACTERISTIC ON THE MAXIMUM AND MINIMUM SEARCH RATE OF A SWITCHED LOOP

It is clear that increasing the width of the discriminator characteristic increases the maximum initial search rate of both the standard and the switched delay lock loops. The solution to equation (3.13) was obtained for the maximum initial search rate of the general asymmetric (n-m)Δ delay lock loop.

It was found that the maximum search rate may be expressed as:

$$\dot{V}_{max} \approx (2.22m + 2.6n + 0.273)\,\omega_n \qquad 3.17$$

for the case of optimum switchover position, $G \longrightarrow \infty$ and ξ = 0.707.

V_{max}	m	n
2.7	0.5	0.5
5.1	1.0	1.0
7.3	2.0	1.0
7.65	1.0	2.0
9.5	3.0	1.0
9.9	2.0	2.0
10.05	1.0	3.0
12.20	3.0	2.0
12.50	2.0	3.0

Table 3.2 Maximum initial search rate for different delay lock loops

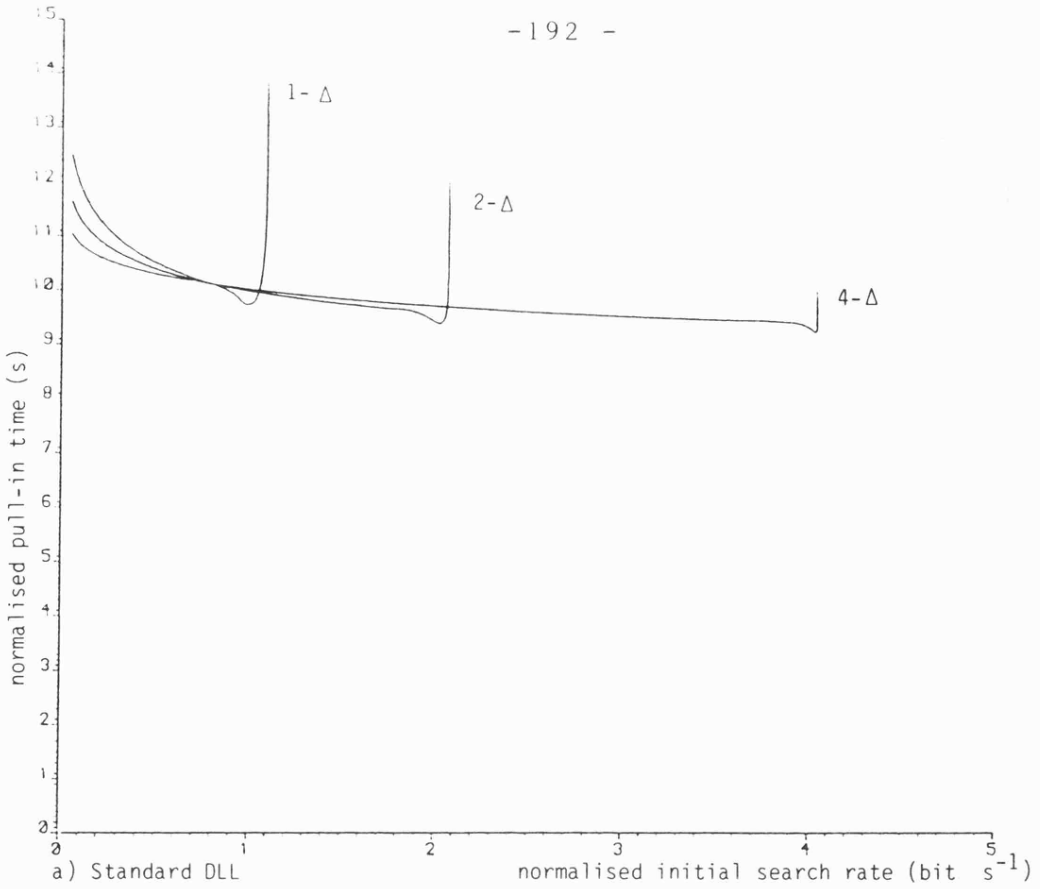
This may be contrasted with equation (3.13) for the unswitched loop. Whereas a large value of n, relative to m, reduces the maximum search rate of the standard delay lock loop, for the case of the switched loop, widening the discriminator characteristic of the loop invariably increases the maximum initial search rate, because there is no positive slope to the discriminator characteristic.

A secondary, but equally important aspect of the switched loop is that by using an initial search rate less than the maximum given by equation (3.17), but which is greater than for the standard loop, the probability of acquisition will be greater when the loop is operated in noisy conditions.

Table 3.2 shows the maximum initial search rate of different symmetric and asymmetric delay lock loops which shows a perfect agreement with equation (3.17).

3.6 EFFECT OF INITIAL SEARCH RATE ON THE PULL-IN TIME OF A STANDARD AND SWITCHED DELAY LOCK LOOPS

It is quite possible to modify the numerical solution technique of equation 3.10 so that the pull-in time of the delay lock loop can be found. Pull-in time is defined here in the inset diagram of Figure 3.37. Figure 3.37 shows the effect of initial search rate on the pull-in time of standard and switched delay lock loops. The characteristics are similar for each type of loop, and the pull-in times are approximately the same, even for wide Δ loops. The reason for this is that although the initial search rate of a wide loop is large, the trajectory is correspondingly larger. The shape of characteristics is particularly interesting. For the standard delay lock loop, for very slow initial search rates the pull-in time will



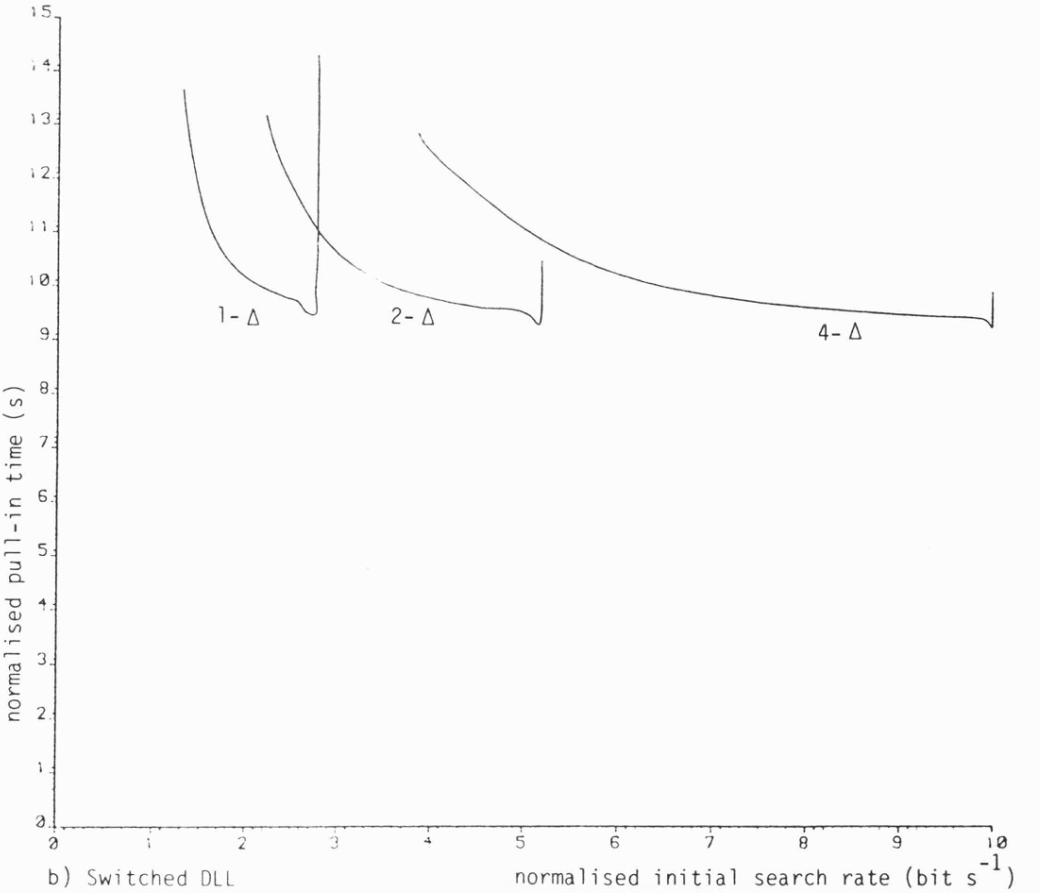


Figure 3.37. Effect of the initial search rate on the pull-in time of 1-Δ, 2-Δ and 4-Δ DLLs in a) standard configuration, b) switched configuration ($G=\alpha$, $\xi=0.707$).

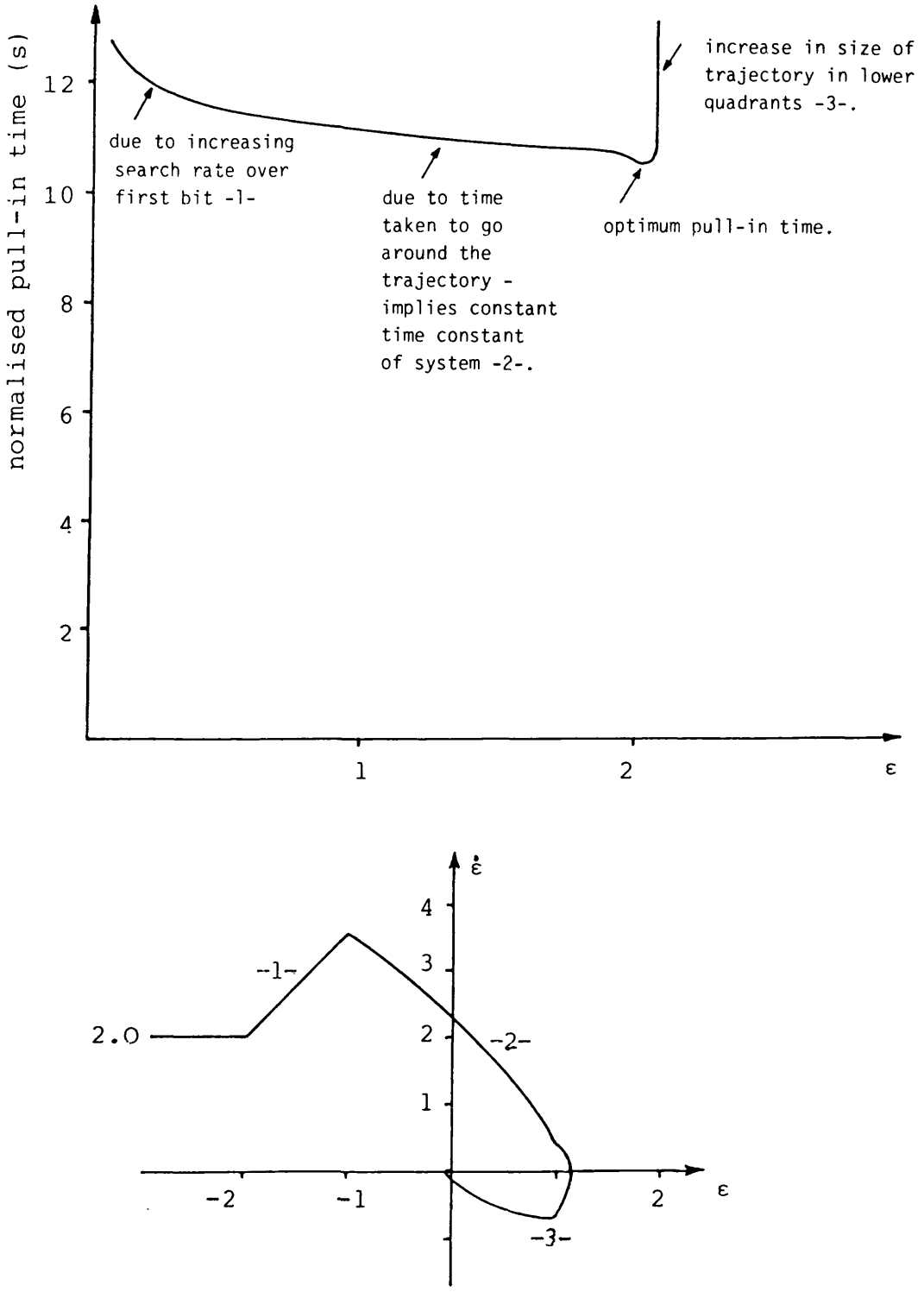


Figure 3.37. Continued.

be slow, irrespective of any loop acceleration. As the initial search rate is increased the pull-in time is reduced. However, the reduction does not follow a simple hyperbolic path because as the initial search rate is increased the acquisition trajectory increases in size. For normalised initial search rates above 1 $bits^{-1}$ the pull-in time remains relatively constant as the acquisition trajectory increases in proportion to the search velocity. For initial search velocities close to the maximum allowed, expansion of the acquisition trajectory in the upper quadrants of the phase plane ceases, giving rise to the small dip in the characteristics. However, for further, very small increase in search velocity, careful examination of the acquisition trajectories reveals that the trajectory expands significantly in the lower quadrant of the phase-plane only. This results in an increase in the pull-in time. As the initial search rate becomes extremely close to the maximum the pull-in time becomes a very lengthy process.

For the case of the switched loops it is seen that there is a minimum search velocity which is necessary to ensure lock. For search rates above this minimum the characteristics are similar to those of the standard delay lock loop. The initial reduction in pull-in time with increasing search rate is "softer" in this case because the switched loop does not accelerate, which obviously speeds up the pull-in time.

The reason for the minimum initial search rate is illustrated in Figure 3.38 for the 2-Δ delay lock loop. At low search rates the trajectory is such that $\dot{x}$ reduces to zero before x exceeds -1 bit, i.e. the epoch search stops or reverses before the codes come into

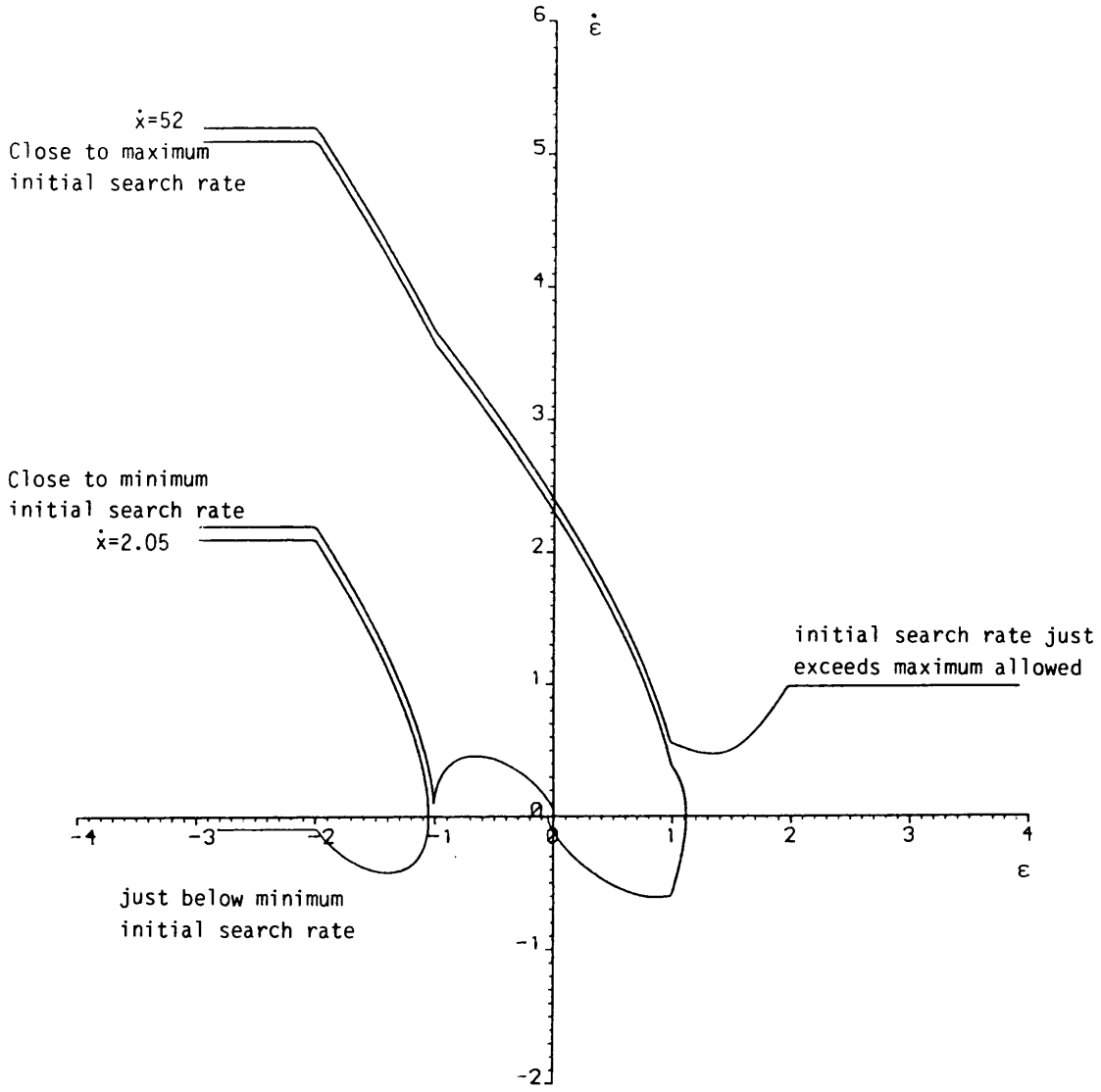


Figure 3.38. Acquisition trajectories of modified switched loop for initital search rate below and above the minimum allowed.

coarse synchronisation. If the initial search velocity is just larger than this minimum, Figure 3.38 shows that the trajectory just exceeds x=-1. The loop then switches over and the loop is forced to pull-in.

If the initial search rate is larger than the maximum allowable, Figure 3.38 shows that lock cannot be achieved.

3.7 MEAN ACQUISITION TIME IN NOISELESS CONDITIONS

In the previous sections it has been stressed that there is a maximum initial search rate from which acquisition may ultimately be achieved. If this value is exceeded lock on the first pass of the two sequences does not occur. Up to this point the mean acquisition time is:

$$T_{max} = (L/2)\,\dot{x}_s\,\omega_n + \text{Pull in time}$$

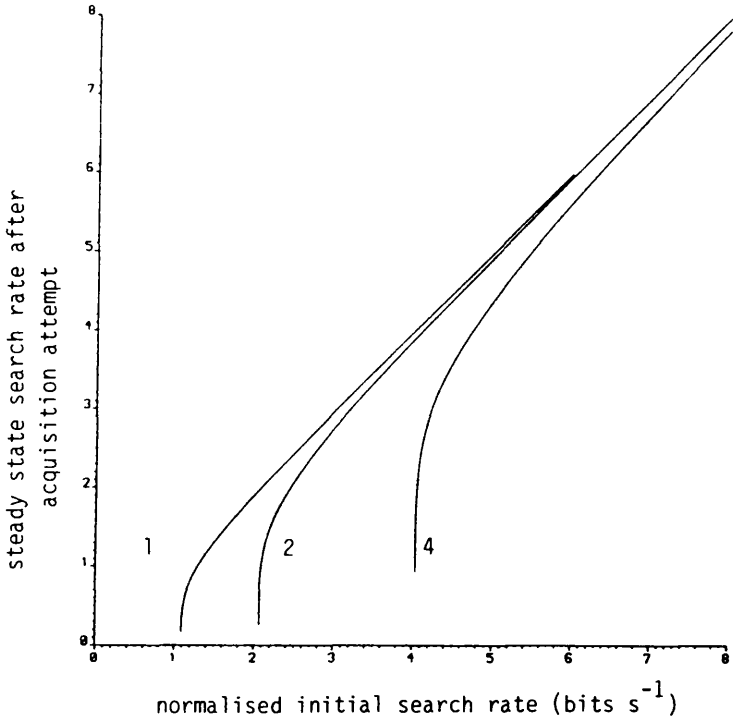
where the pull-in time has been plotted for various loops in the previous section as a function of x, and L is the sequence length.

However, it will be seen from the acquisition trajectories that even if lock is not achieved on the first pass it may be possible to acquire lock on subsequent passes. The reason for this is that when the loop gain is very high the search rate at the end of the attempted acquisition process is lower at the value before acquisition is attempted. This lower value is maintained by the "memory" of the loop (only when g is very high) until the sequence next slides past the phase synchronisation condition and acquisition with this lower search velocity can be re-attempted. As the loop gain g is reduced the "memory" is also reduced and the search velocity gradually increases during the subsequent epoch search until it is the same value as the original search velocity. In this case

each acquisition attempt is an independent trial.

Considering the case where $g \rightarrow \infty$ figure 3.39 (a) shows the steady state search rate after an acquisition attempt as a function of the initial search for 1Δ, 2Δ, and 4Δ DLLs under noiseless conditions. (The effect of noise on the maximum initial search rate will be given in Chapter 6). This information can be used to calculate the number of passes of the sequence required for lock to be achieved. This is shown in Figure 3.39 (b). It is clear that it is possible to acquire lock when $\dot{x}_s > \dot{x}_{s\ max}$ but the number of passes required rises very sharply and for the case where $\dot{x}_s = 2\dot{x}_{s\ max}$ approximately 10 passes are required. When calculating the mean acquisition time the pull-in time from the 10 attempted pull-ins would have to be included. In the previous section it has been shown that pull in can become a very lengthy process when $\dot{x}_s \approx \dot{x}_{s\ max}$. It is thus interesting to see whether it is better to allow x_s to be greater than $x_{s\ max}$ on the basis that the second serial search time may be accomplished faster than one pull-in attempt. Figure 3.39 (c) shows the mean acquisition time of a 1023 bit long sequence for 1Δ, 2Δ, and 4Δ DLLs when $\xi = 0.707$ and $\omega_n = 1$ rad s^{-1}.

The ranging receiver application may be considered as a special case. In the majority of cases the delay lock loop will be used in multi-access communication systems in which the pseudo noise sequences are data modulated. This technique will be discussed in Section 3.8.



a)

b)

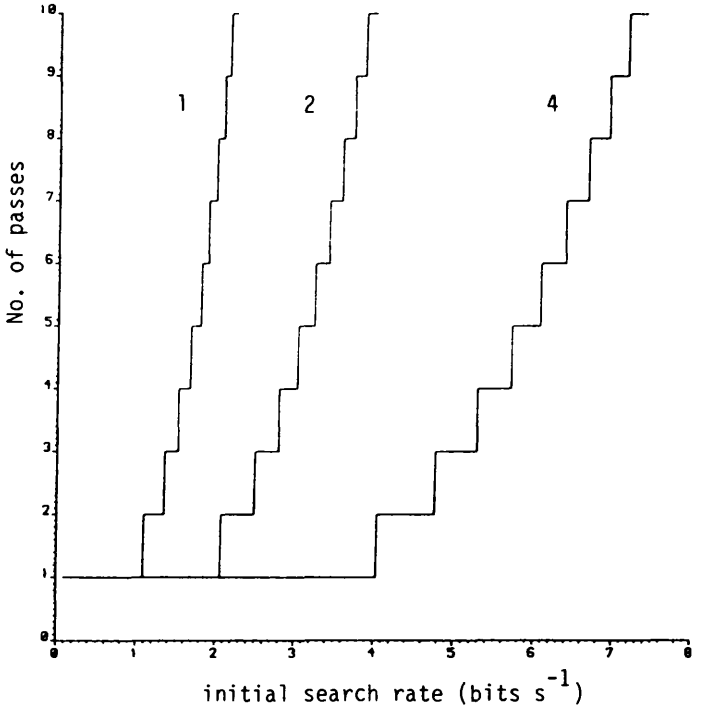
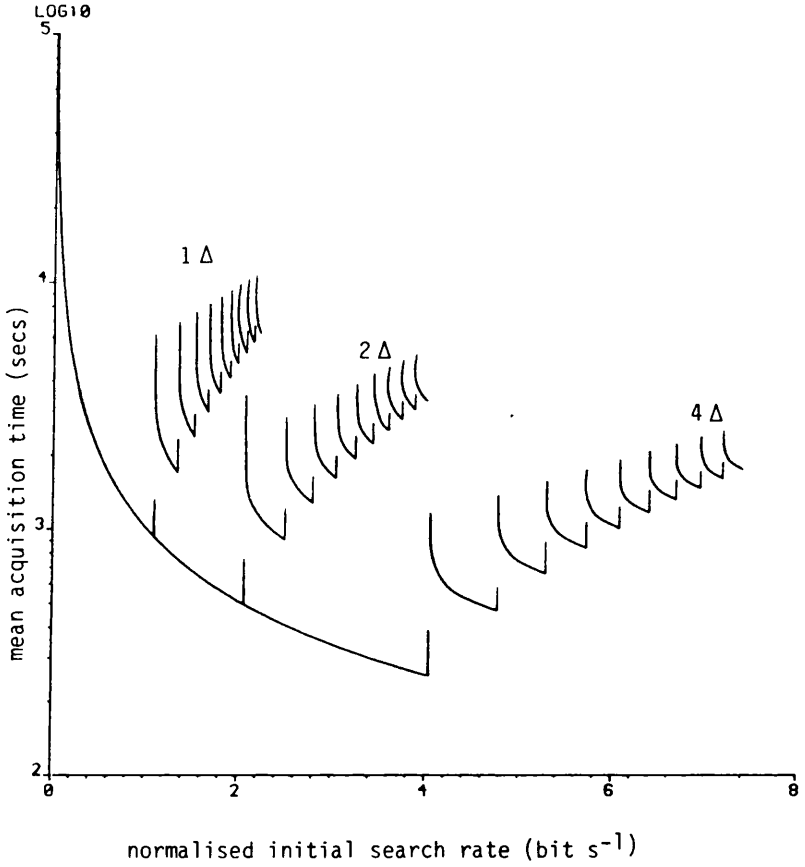


Figure 3.39

a) Effect of the normalised initial search rate (for $\dot{x}_s > \dot{x}_{s\,max}$) on the steady state search rate after the acquisition attempt (for $g \to \infty$, ω_n=1 rad s^{-1}, and ξ=0.707) for 1Δ, 2Δ, and 4Δ loops.

b) Graph of the number of acquisition attempts needed before lock is achieved as a function of normalised initial rate $\dot{x}_s > \dot{x}_{s\,max}$ for 1Δ, 2Δ and 4Δ loops ($g \to \infty$, ω_n = 1 rad s^{-1} and ξ= 0.707)



c)

Figure 3.39 (Continued)

c) Effect of the normalised initial search rate on the mean acquisition time for $\dot{x}_s > \dot{x}_{s\ max}$ for 1Δ, 2Δ, and 4Δ loops ($g \rightarrow \infty$, ω_n = 1 rad s^{-1} and ξ=0.707).

3.8 APPLICATION OF SWITCHED DELAY LOCK LOOPS TO SPREAD SPECTRUM COMMUNICATION SYSTEMS

3.8.1 Introduction

The delay lock loops thus far described have been intended for use in ranging receiver applications. Data modulated direct-sequence spread spectrum systems commonly use sequence inversion keying in which the data is modulo-2 added to the high speed pseudo noise sequence. To achieve the necessary processing gain the data rate is much less than the chip rate of the pseudo noise sequence. Generally, each data bit has the same period as one entire pseudo noise sequence period and is clocked coherently with the start of each sequence. However, the data may be transmitted asynchronously, if desired. The effect of modulated data on a delay lock loop synchroniser is to change the polarity of the N-shaped discriminator characteristic whenever the data changes polarity. The data rate is much higher than the loop filter bandwidth, and as a consequence the mean value of error signal fed to the voltage controlled oscillator is zero if the data is assumed to be random. A common technique of overcoming this problem is to use an envelope detector in each arm of the delay lock loop to maintain the polarity of the individual early and late correlations. A requirement of these detectors is that they should demodulate the data linearly (rather than square low) otherwise the loop has reduced gain at the optimum position of lock [14]. Although such techniques are viable for simple 1-Δ and 2-Δ delay lock loops they become less viable as the size of the loop increases involving more separate correlations.

Davies and Al-Rawas [18] and Ormondroyd and Shipton [14] have

separately proposed data feedback techniques to remove the need for envelope detection. In this technique, an estimate of the data is obtained from the spread spectrum data correlator. This is fed back to the data modulated pseudo noise sequence applied to the delay lock loop synchroniser where it is modulo-2 added to produce a "clean" pseudo noise sequence devoid of modulation. It will be apparent that the data correlator first requires the local pseudo noise sequence to be in phase with the received data modulated signal before it can supply an accurate data estimate to the synchroniser. However, the delay lock loop idles, such that the loop performs an epoch search when out of lock. If the epoch search is sufficiently slow the data estimate can be obtained as the two sequences slide past each other through phase synchronisation. This can be fed to the synchroniser, and the data modulation removed. The loop then "snaps" into synchronisation. The in-lock performance of this loop is given in [14]. The penalty of this type of crude data feedback delay lock loop is a reduction in the maximum initial search rate. In wide-Δ loops the problem is less acute because there is a correspondingly longer time to feed the estimate back to the delay lock loop during pull-in.

This problem exists because the data estimate can only be made when the locally generated sequence, S_i, comes within ± 1 bit of synchronisation of the received sequence, dictated by the correlation function of the pseudo noise sequence. If a reliable data estimate can be made before the loops start to acquire lock then there should be no reduction in the maximum search rate.

Thus, for a general $(n-m)\Delta$ delay lock loop a reliable estimate should be available for $(n+m+2)$ bits. This may be achieved quite

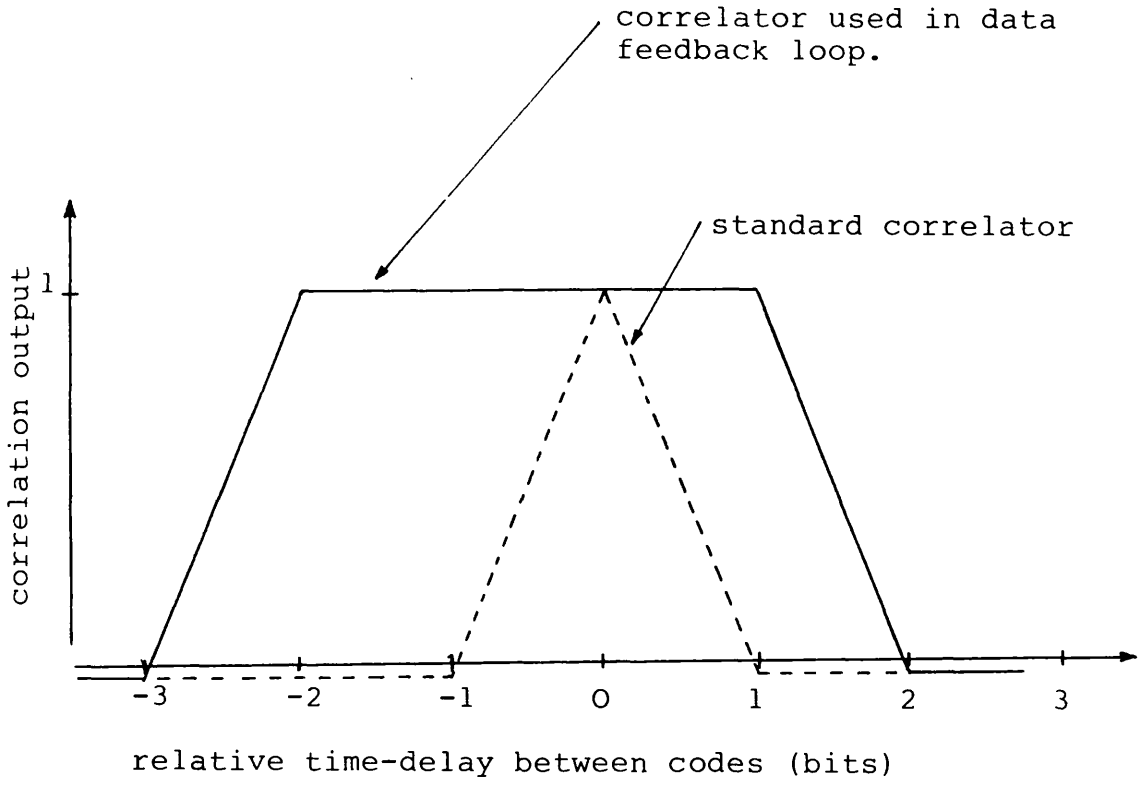


Figure 3.40. Extended data correlation characteristics necessary to employ the data feedback technique

easily with minimum extra hardware by performing multiple data correlations in parallel using several early and late local sequences generated by the feedback shift register. Figure 3.40 illustrates the technique applied to a switched 2-Δ delay lock loop and shows the extended correlator characteristics, compared with a standard correlator. It is clear that the data estimate is available to the delay lock loop over a range of delay errors beyond that of the normal correlator. It is not necessary for this new correlator characteristic to be symmetrical because the loop acquires lock during the search procedure and delay errors of +2 bit are not achieved in a 2-Δ delay lock loop. However, it is obvious that the range over which the data can be recovered may be extended to the limit set by the length of the feedback shift register.

3.8.2 Switched Delay Lock Loop Using Data Feedback

The technique is shown in Figure 3.41. The delay lock loop incorporates the data correlator as well as the synchronisation and tracking loop, which may be of any type described earlier. Considering the data correlator section, the low pass filter on the data correlator has a cut off frequency equal to the data rate and the zero crossing detector is used to restore the shape of the data bits.

It will be seen that the configuration of the switched 2-Δ delay lock loop is slightly different from that shown earlier, in that the S_{i-1} correlation is not performed until after the summing operation. This is permissible because the mixing operation is linear, and its effect is to keep the number of multiplier ICs to a minimum. In this loop configuration the arithmetic sum of the locally generated

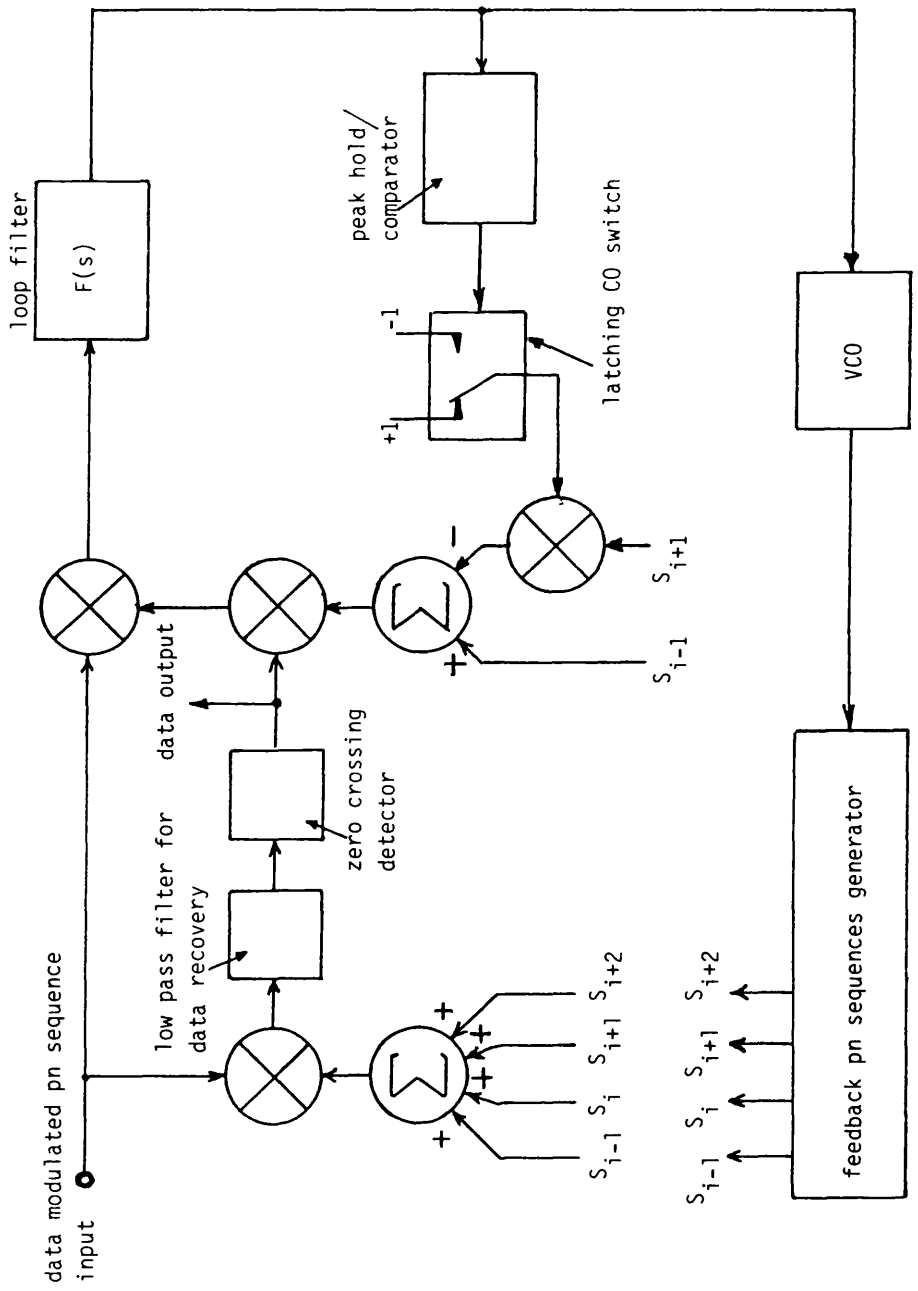


Figure 3.41. Application of switched DLL to a data modulated PN sequence using data feedback

sequences, $(S_{i+1} + S_{i-1})$ is first modulated by data which is then correlated against the data modulated received signal, using the loop filter to perform the integration process. The discriminator characteristics are identical to those shown in Figure 3.18.

Two types of data source were used with the experimental switched delay lock loop with data feedback. The first type of data was clocked synchronously with the pseudo noise sequence and had a data bit period equal to the sequence period. The second type of data had the same nominal data rate, but was clocked asynchronously with respect to the pseudo noise sequence. The pseudo noise code was a 1023 bit maximal length sequence clocked at 1 MHz in the transmitter. For the purpose of these tests a standard unswitched delay lock loop is compared with the switched delay lock loops outlined in Section 3.3.1 and 3.3.2. The loop natural frequency, ω_n was set to 1 rad per sec and the damping ratio, $\xi = 0.707$. The low pass filter, used to remove the data estimate from the data correlator, was set, in the first instance, equal to the data rate (977 bit per sec) to minimise pulse distortion. The data source was generated from a maximal length sequence generator.

Figure 3.42 shows the experimental acquisition trajectories of unswitched and switched delay lock loops with both synchronous and asynchronous data feedback. The acquisition trajectories show that there is no significant difference between synchronous and asynchronous data. They also show that the data has no effect on the maximum initial search rate when data feedback is used, and that in every case the maximum initial search rate is the same as the theoretical predicted value found earlier in the chapter.

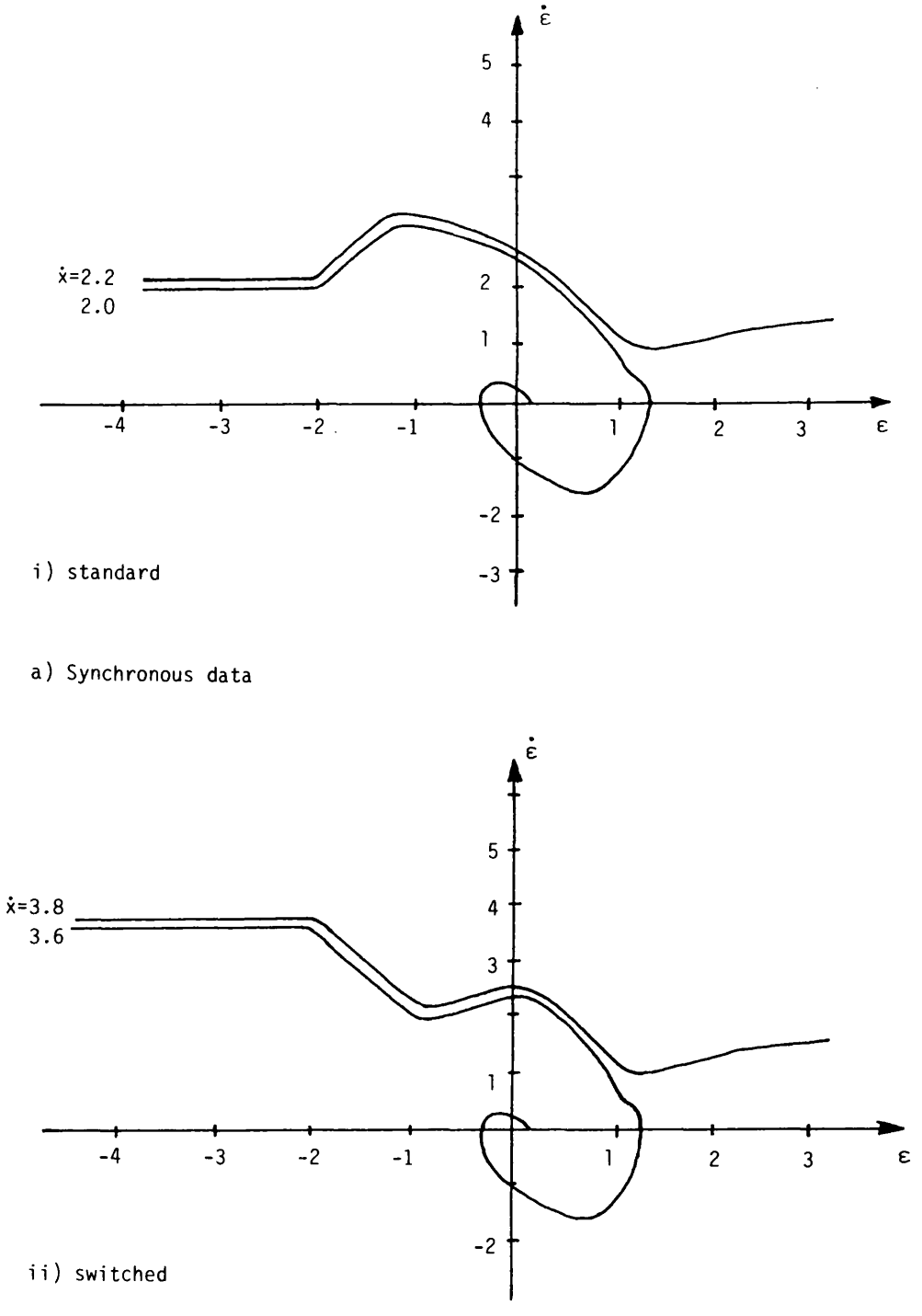
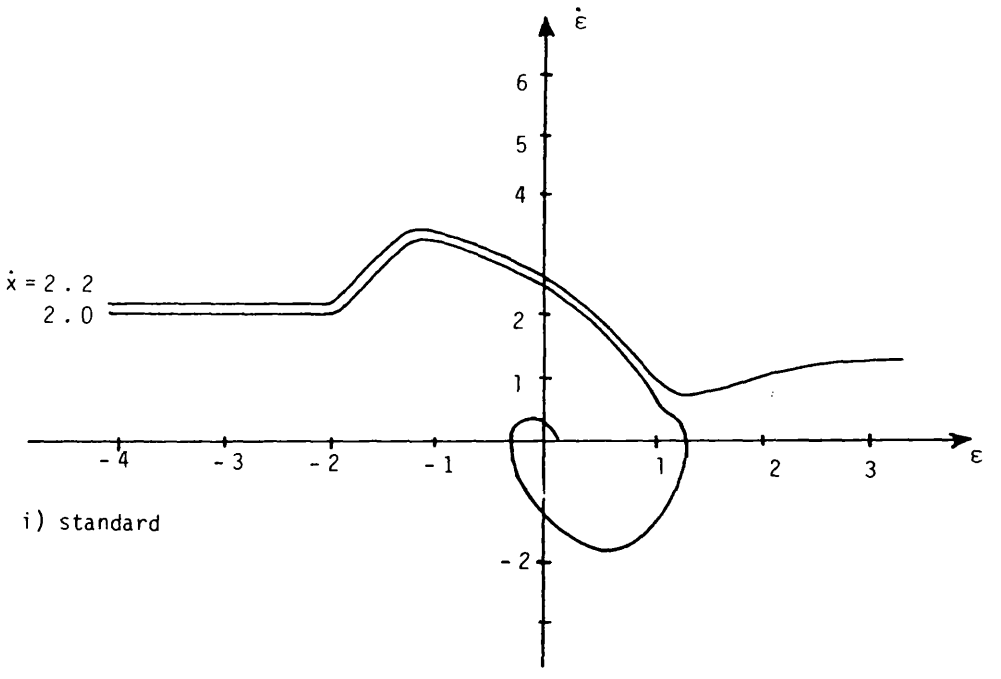


Figure 3.42 Experimental acquisition trajectories of standard and switched 2-Δ delay lock loop using data feedback

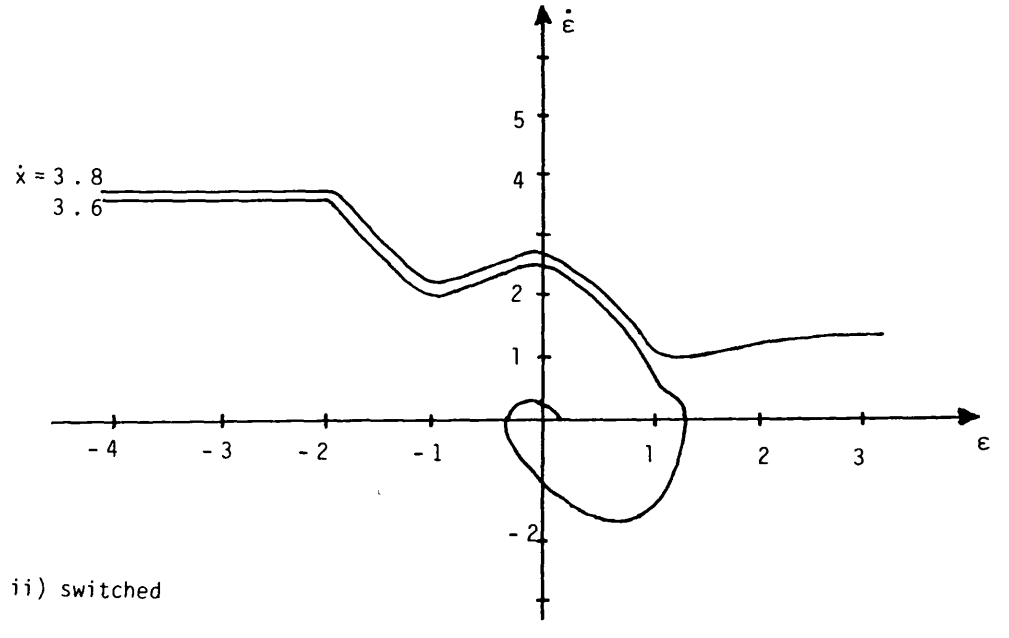
a) synchronous data

b) asynchronous data



i) standard

b) Asynchronous data



ii) switched

Figure 3.42 Continued.

	with data feedback			without data feedback		
	standard loop	switched loop	modified switched loop	standard loop	switched loop	modified switched loop
No data	2.0	3.6	5.1	2.0	3.6	5.1
Synchronous data	2.0	3.6	5.1	2.0	3.6	5.1
Asynchronous data	2.0	3.6	5.1	2.0	3.6	5.1

Table 3.3. Comparison of the normalised maximum initial search rate (rad s^{-1}) for standard and switched variants of the delay lock loop with and without data feedback for synchronous and asynchronous data.

Table 3.3 compares the values of maximum initial search rate found for the types of delay lock loop listed.

It is important here to emphasise that the natural frequency of the loop and the maximum search rate were measured while the bandwidth of the low pass filter which is located between the first multiplier and the zero crossing detector is equal to the data bit rate (977 Hz).

For the case of 4-Δ delay lock loop used with data feedback it is necessary to widen the data correlator if maximal initial search rate is to be achieved. In this case six data correlator would be performed from sequence S_{i+3} to sequence S_{i-2} inclusive. However, this requires no more hardware, except for extra summing junction in the summing amplifier of the data correlators.

3.8.3 Switched Delay Lock Loop without Data Feedback

Figure 3.43 shows a block diagram of a switched version of the 2-Δ delay lock loop used previously by Ward [20] to track a sequence inversion keying modulated signal. The only addition to the delay lock loop is the switching section.

When the input signal is one bit delayed from the locally generated sequence S_i (i.e. synchronised with S_{i-1}), the output of the correlator in arm 1 is at a maximum positive value, regardless of the polarity of the data.

Similarly when the input signal is one bit advanced with respect to the locally generated sequence S_i (i.e. synchronous with S_{i+1}), the output of the correlator in arm 2 is also at a maximum positive peak value. So by multiplying the positive triangle in this arm by xl before subtracting it from the other signal of arm 1, the usual N-

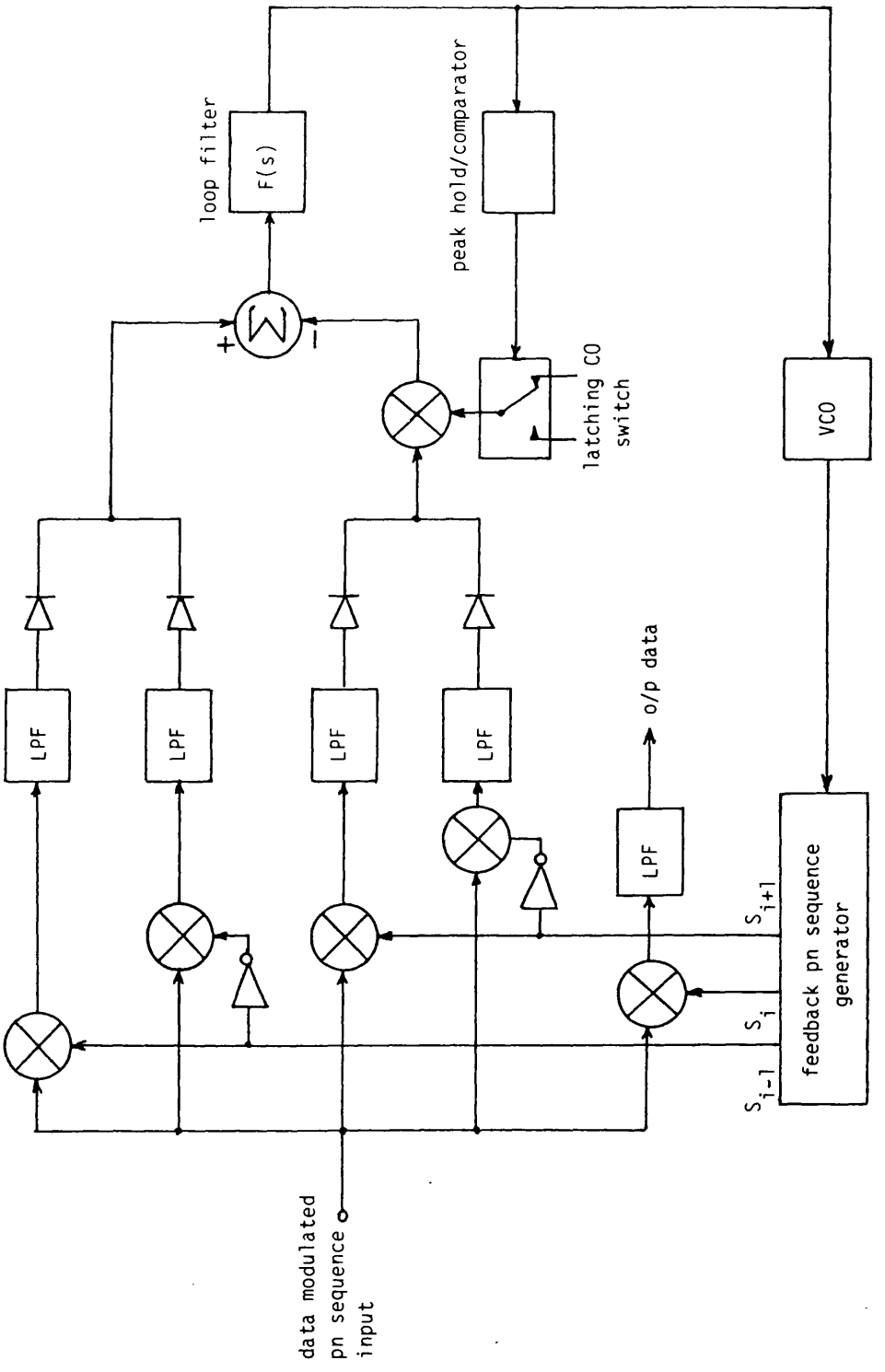


Figure 3.43. Application of switched DLL to a data modulated PN sequence without using data feedback

shape error curve is developed and it is identical to that shown in Figure 3.18a which can acquire synchronisation and maintain tracking in a standard way.

However, if instead, the positive triangle in arm 2 is multiplied by minus one, the switched version of the N-shaped error curve is developed and it is identical to that shown in figure 3.18b, to start the synchronisation process with higher search rate followed by the tracking process as discussed earlier.

The bandwidth of the low pass filter must be chosen carefully. It should be wide enough so that the data can pass to the next stage, and should be narrow enough in order to improve the signal to noise ratio at the rectifier's input.

It was found that the acquisition and tracking behaviour of this delay lock loop is identical to those discussed earlier.

Synchronous and asynchronous data are also used with this loop. Similar experimental results of the acquisition trajectories of the unswitched and switched loops to those shown in Figure 3.42 were obtained with synchronous and asynchronous data, which means that the data has no effect on the maximum initial search rate.

3.9 CONCLUSIONS

A novel delay lock loop [29] has been described which provides a substantial improvement in the maximum search rate obtainable. The performance of the modified delay lock loop compares extremely well with theoretical calculation. It can achieve acquisition of lock from initial search rates which are x2.5 higher than standard delay lock loops at a damping ratio of 0.707, yet has no significant effect

on the pull in time and without worsening the in-lock performance in any way. It has also been shown that controlling the damping ratio during acquisition, in conjunction with this new loop can also yield very large increase in initial search rate. There is an increase of x4.1 and x8.2 in the search rate for every 0.707 increase in the damping ratio for 2Δ and 4Δ loops respectively. The cost in terms of additional hardware is minimal. Finally, two techniques have been applied to standard and modified delay lock loop and it has been found that neither the synchronous nor asynchronous data has any effect on the pull-in properties of the loops described.

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CHAPTER FOUR

TRANSMITTING A MULTILEVEL SEQUENCE IN A DIRECT SEQUENCE SPREADSPECTRUM SYSTEM FOR IMPROVED CODE ACQUISITION

4.1 MULTILEVEL SPREAD-SPECTRUM SYSTEMS

4.1.1 Introduction

The most complex part of a direct sequence spread-spectrum system is the receiver, where synchronisation and tracking have to be achieved before any communication link is established. A great deal of effort has been expended in this area. Two main methods of synchronising the local despreading code to the transmitted signal have been widely used. One is the delay lock loop and the other is the Tau-dither loop. These have been described earlier, and both have found use in ranging and data modulated systems.

In some applications, where it is necessary to employ spread spectrum techniques, the receiver design must be limited in cost, weight and/or size, yet without sacrificing any performance in terms of acquisition performance or in-lock noise performance.

In this section modifications are detailed which allow the receiver to be considerably reduced in complexity and cost, yet which have the same high-speed acquisition performance of the standard delay lock loops detailed in Chapter Three.

The basic idea of the new technique is to transmit a multi-level sequence at the transmitter instead of the conventional two level sequence, and to simplify the delay lock loop accordingly.

This modification could be applied particularly where there is a single transmitter and many receivers which can be jointly or separately addressed from the transmitter (e.g. navigation, satellite

reception, etc.). In this case there will be a large reduction in overall system complexity for a marginal increase in the complexity of the single transmitter.

Although the modification can be applied to **any** standard delay lock loop the technique will be described specifically for the 2Δ and 4Δ variants. For the 2Δ loop the new transmitted sequence will be sequence of **three** levels, whilst for the 4Δ loop the new sequence will be **seven** levels. Other delay lock loops require different level sequences. This section also shows the method of generating these multi-level sequences in the transmitter.

4.1.2 Simplification of the Receiver

In Chapter Three it was shown that the acquisition performance of the delay lock loop was determined by the discriminator characteristics, and that by using several separate correlations with scalar weighted delayed and advanced replica sequences the discriminator characteristics can be broadened, which enables the initial search velocity to be increased yet still keep the filter bandwidth constant. This technique requires the delay lock loop to have several mixers and amplifiers. This can be costly.

Ideally, the transmitted pseudo random sequence, when correlated with the local replica should produce a broad discriminator characteristic using a single correlation. In this way the 'n' arms of the delay lock loop variants, where n = 2, 3, 4 ... can be reduced to a single arm, in a configuration identical to the phase lock loop.

The use of a multi-level pseudo-noise sequence - rather than a binary pseudo-noise sequence, correlated with a conventional binary

pseudo-noise sequence in the receiver can generate such a discriminator characteristic. In the next section, the structure of multi-level sequences which give broad discriminator characteristics when correlated with a binary p-n sequence will be given, together with the spectrum of the transmitted signal. This is, of course, a particularly important parameter in a spread-spectrum system.

4.1.3 Transmitter Modifications

Consider equations 4.1 and 4.2, which represent the output of the correlation network of the receiver's 2-Δ and 4-Δ delay lock loop respectively:

$$\Psi_{2\text{-}\Delta_{cross}} = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} [a(t).b(t)-a(t).b(t+2\Delta)]dt \qquad 4.1$$

$$\Psi_{4\text{-}\Delta_{cross}} = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} \left\{[a(t).c(t)+a(t).\frac{1}{2}c(t+\Delta)]- [a(t).\frac{1}{2}c(t+3\Delta)+a(t).c(t+4\Delta)]\right\}dt \qquad 4.2$$

where a(t) is the received sequence, b(x) and c(x) are the locally generated sequences.

However, equation 4.1 can be rewritten as:

$$\Psi_{2\text{-}\Delta_{cross}} = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} a(t).[b(t)-b(t+2\Delta)]dt \qquad 4.3$$

Thus, by subtracting the two locally generated sequences b(t+2Δ) from b(t) and multiplying the resulting signal by the received signal a(t) it is still possible to get the required N-shape error curve in the receiver's delay lock loop.

Similarly equation 4.2 can be rewritten as:

$$\Psi_{4\text{-}\Delta_{cross}} = \text{limit}_{T\longrightarrow\infty} \frac{1}{2T} \int_{-T}^{T} a(t)\Big\{[c(t) + \frac{1}{2} c(t+\Delta)] - [\frac{1}{2} c(t+3\Delta) + c[t + 4\Delta)]\Big\}dt \qquad 4.4$$

which leaves the four locally generated sequences processed together in the manner shown above and then multiplied by the received signal a(t).

Thus, it is quite possible to transmit a composite or multi-level signal representing the term [b(t)-b(t+2Δ)] in equation 4.3 to obtain the discriminator characteristic of a simple 2-Δ delay lock loop. Equally, it is possible to transmit a multilevel signal respectively $\{[c(t)+ \frac{1}{2}c(t+\Delta)]-[\frac{1}{2}c(t+3\Delta)+c(t+4\Delta)]\}$ to obtain the discriminator characteristic of a simple 4-Δ delay lock loop. These characteristics are achieved by correlating the composite sequence with only a single local sequence d(t), a single multiplier, and a single low pass filter or a loop filter. This means that no modification is necessary to the receiver in order to develop the new delay lock loop system. But the transmitter sequence must be modified to achieve these changes.

Figure 4.1(a) shows a three level signal +A, 0, and -A, as a result of subtracting the maximal length sequence b(t+2Δ) from b(t). Its auto-correlation function is shown in figure 4.1(b). The power spectrum density $S(\omega)$ could be found from the auto-correlation function via the Weiner-Kintchine relationship:

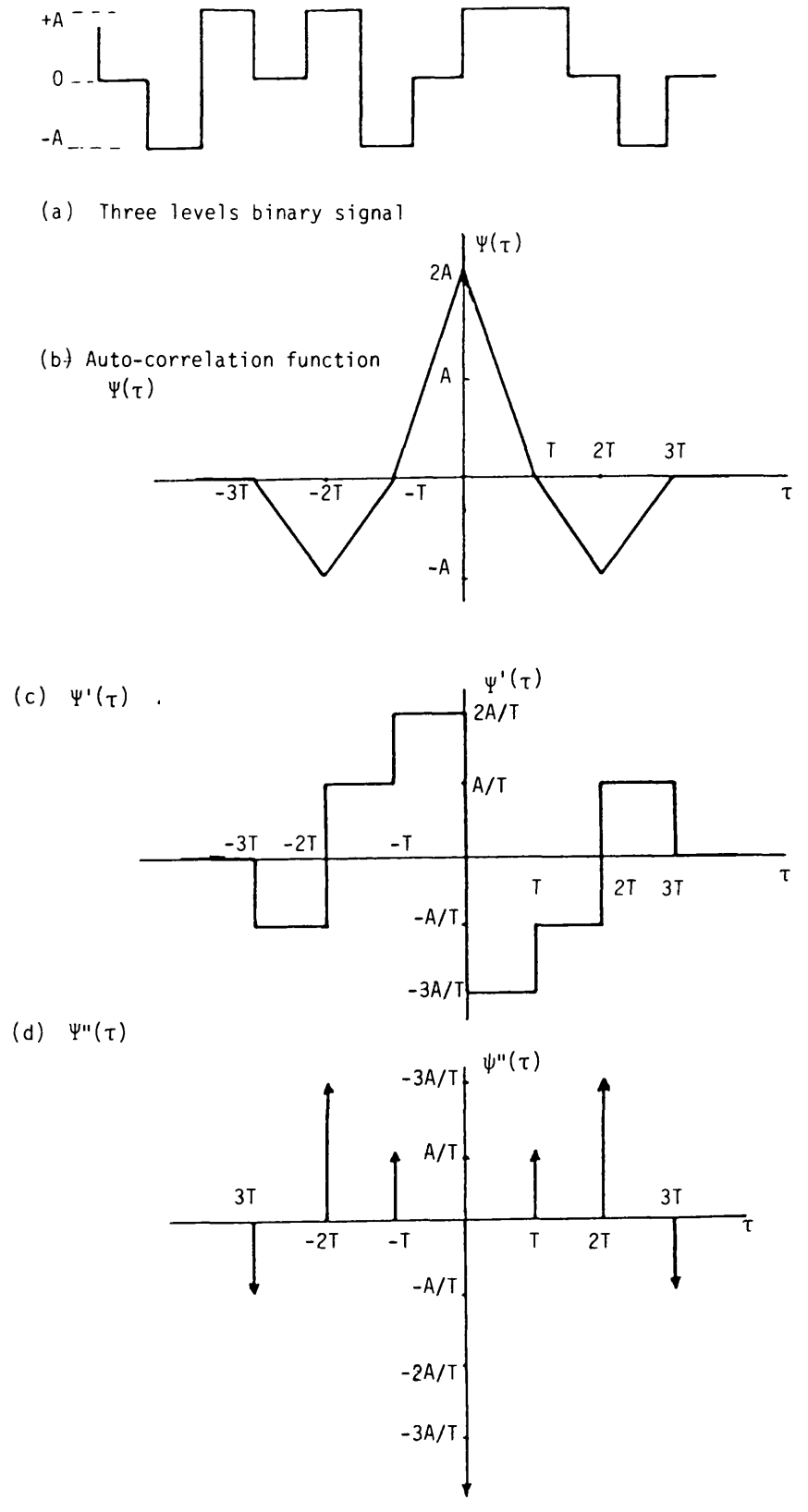


Figure 4.1. Three levels random binary code.

$$S(\omega) = \frac{1}{(j\omega)^2}\left[-A/T(e^{j3\omega T} + e^{-j3\omega T}) + 2A/T\,(e^{j2\omega T} + e^{j2\omega T})\right.$$

$$\left. - A/T\,(e^{j\omega T} + e^{-j\omega T}) - 4A/T\right)$$

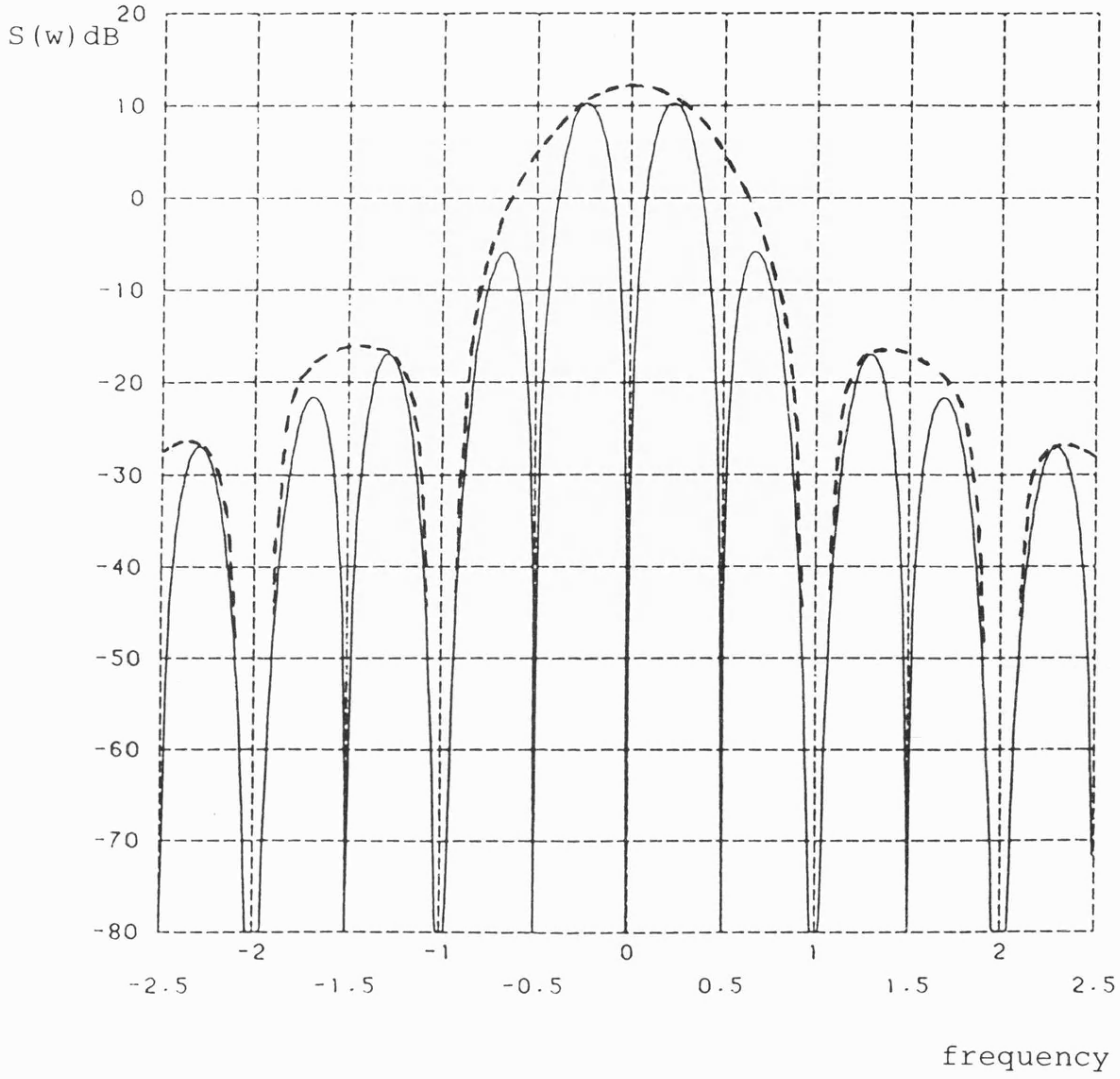
$$= \frac{2A}{\omega^2 T}\left[\text{Cos } 3\omega T - 2 \text{ Cos } 2\omega T - \text{Cos } \omega T + 2\right]$$

$$= AT\left[\left(\frac{\text{Sin } \omega T/2}{\omega T/2}\right)^2 + 8\left(\frac{\text{Sin } \omega T}{\omega T}\right)^2 - 9\,\left(\frac{\text{Sin } 3\omega T/2}{3\ \omega T/2}\right)^2\right] \qquad 4.5$$

The power spectral density of this three level sequence was calculated and this is shown in Figure 4.2. Unlike the power spectrum density of a standard spread spectrum transmitter which usually has zeros at multiples of $2\pi/T$, it appears to have zeros at multiples of π/T. If the traditional bandwidth of spread spectrum transmitted signal is considered, that is $2x2\pi/T$ or $2xR_c$, where R_c is the clock frequency of the maximal length pseudo-noise sequence, it is found that the total power of the new developed transmitted signal is twice the total power of the standard transmitted signal as shown in Figure 4.3. This is not surprising because the transmitted signal level is also larger (2A rather than A). These graphs are particularly important because they show the distribution of power within the main lobe of the transmitted signal.

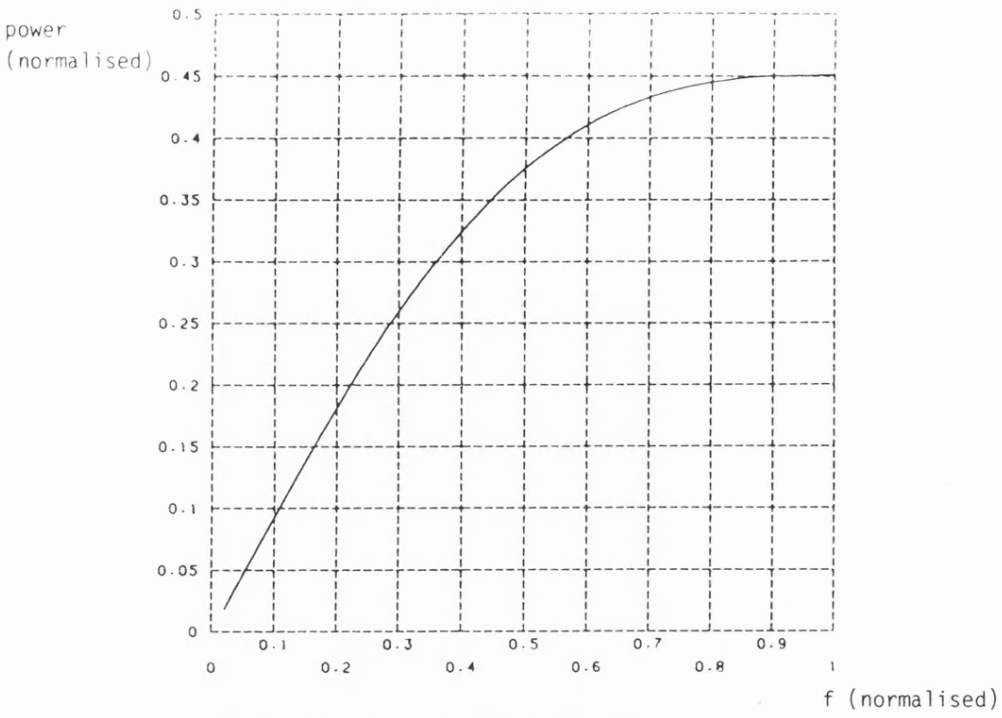
The modified receiver will be explained later on. The generation of the signal which has three levels [+A, 0, -A] is produced in the transmitter by the way shown in Figure 4.4(a).

The baseband output signal (S_{i-2}-S_i, i.e. S_{i-1}-S_{i+1}) is generated and transmitted, however in the receiver only S_i is needed to complete the requirements of the 2-Δ delay lock loop, i.e. to obtain the discriminator characteristics of the 2-Δ delay lock loop.

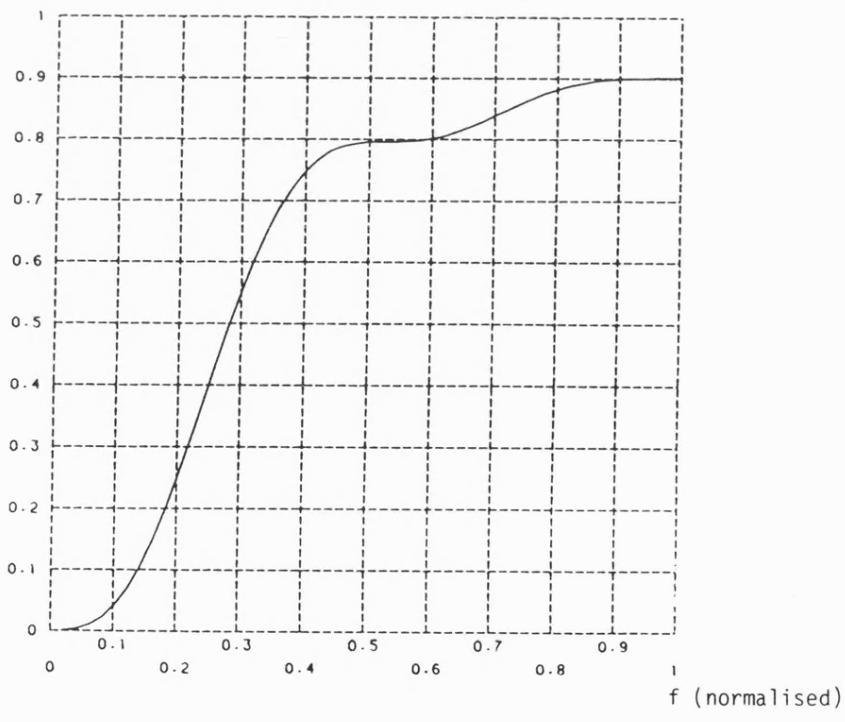


(a) Power spectral density

Figure 4.2. Power spectral density of three level sequences.

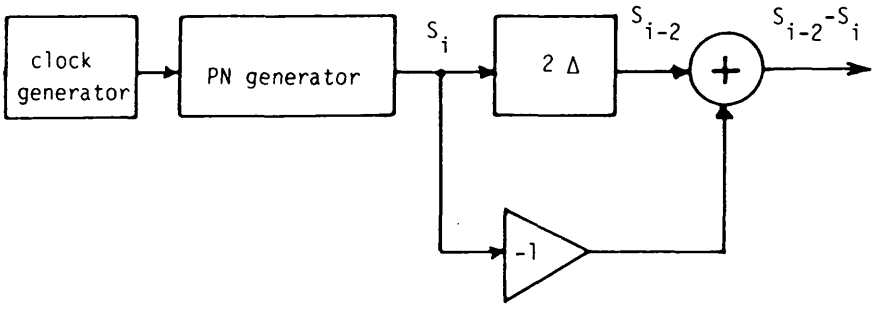


(b) distribution of power in the main bandwidth of a standard 2 levels sequence



(c) distribution of power in the main bandwidth of a three level sequence

Figure 4.3. Power distribution in the main lobe.



a) Three level sequence generator

b) Seven level sequence generator

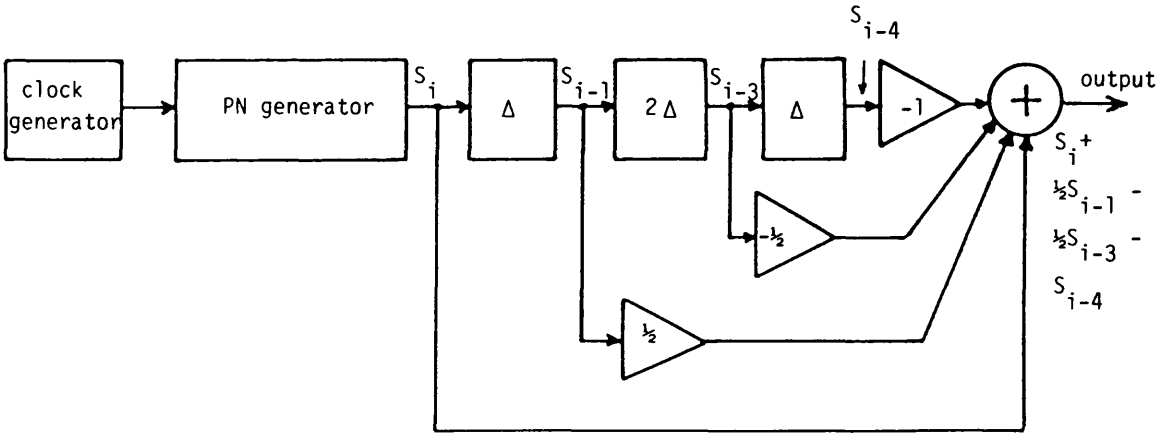


Figure 4.4. Generation of multilevel sequence in the transmitter.

For the 4-Δ delay lock loop the output baseband transmitted signal should be $S_{i-2} + \frac{1}{2}S_{i-1} - \frac{1}{2}S_{i+1} - S_{i+2}$. This signal has seven levels, 3A, 2A, A, 0, -A, -2A, and -3A as shown in Figure 4.5, together with its auto-correlation function.

The power spectrum density $S(\omega)$ of this signal is also found from the auto-correlation function as:

$$S(\omega) = \frac{1}{(J\omega)^2}\,[0.25\ A/T(e^{j\omega T}+e^{-j\omega T})+0.5A/T(e^{j2\omega T}+e^{-j2\omega T})+0.75A/T(e^{j3\omega T}$$

$$+ e^{-j3\omega T})+A/T(e^{j4\omega T}+e^{-j4\omega T})-A/T(e^{j5\omega T}+e^{-j5\omega T})-3A/T]$$

$$= \frac{2.5\ A}{j^2\omega^2 T}\,[0.2\ \mathrm{Cos}\,\omega T+0.4\ \mathrm{Cos}\ 2\omega T+0.6\ \mathrm{Cos}\ 3\omega T$$

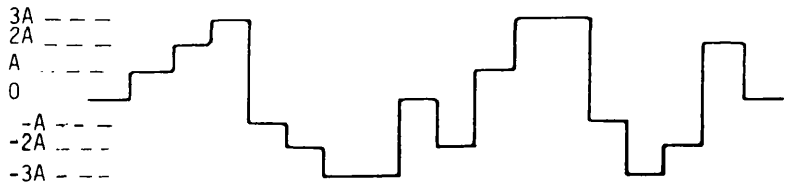
$$+ 0.8\ \mathrm{Cos}\ 4\omega T-0.8\ \mathrm{Cos}\ 5\omega T-1.2]$$

$$S(\omega) = 2.5AT\left[0.1\left(\frac{\mathrm{Sin}\ \omega T/2}{\omega T/2}\right)^2 + 0.8\left(\frac{\mathrm{Sin}\ \omega T}{\omega T}\right)^2 + 2.7\left(\frac{\mathrm{Sin}\ 3\omega T/2}{3\omega T/2}\right)^2\right.$$

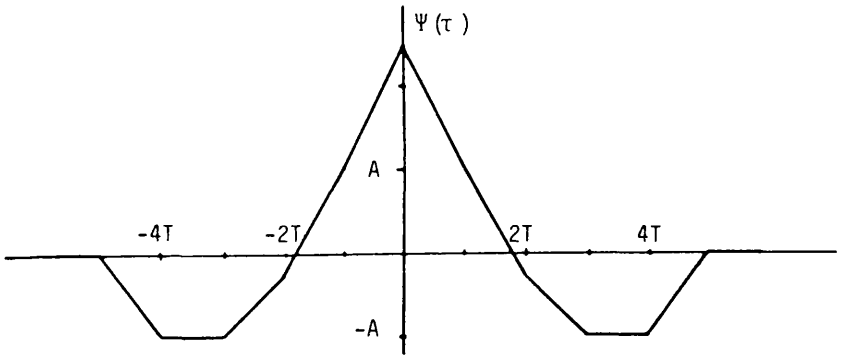
$$\left. + 6.4\left(\frac{\mathrm{Sin}\ 2\omega T}{2\omega T}\right)^2 - 10\left(\frac{\mathrm{Sin}\ 5\omega T/2}{5\omega T/2}\right)^2\right] \qquad 4.6$$

The power spectrum density $S(\omega)$, of this seven level signal is shown in Figure 4.6(a). Again, this shows that the power spectrum density has zeros at multiples of $\pi/2T$, and the total power in the main bandwidth, i.e. $2xR_c$, this time is 2.5 times the total power of the traditional spread spectrum signal, as shown in Figure 4.6(b), which also shows the distribution of the power within the main loop.

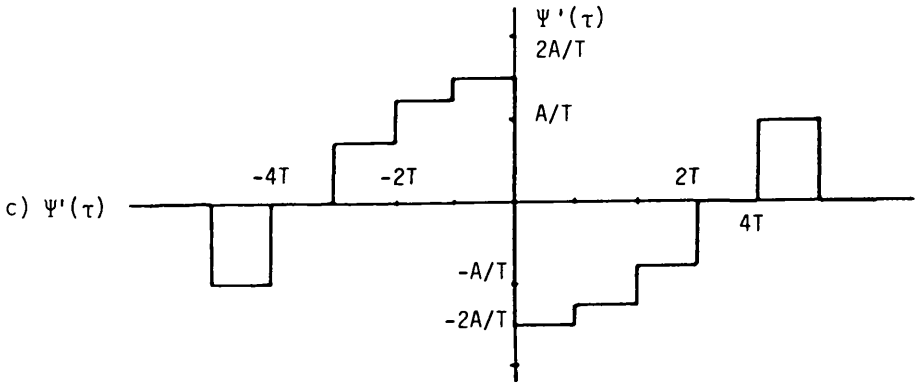
The output signal is produced in the transmitter by the structure shown in Figure 4.4(b). The baseband output signal ($S_i + \frac{1}{2}S_{i-1} - \frac{1}{2}S_{i-3} - S_{i-4}$, i.e. $S_{i-2} + \frac{1}{2}S_{i-1} - \frac{1}{2}S_{i+1} - S_{i+2}$) is transmitted, and in the receiver this signal is correlated or multiplied only by one single sequence S_i.



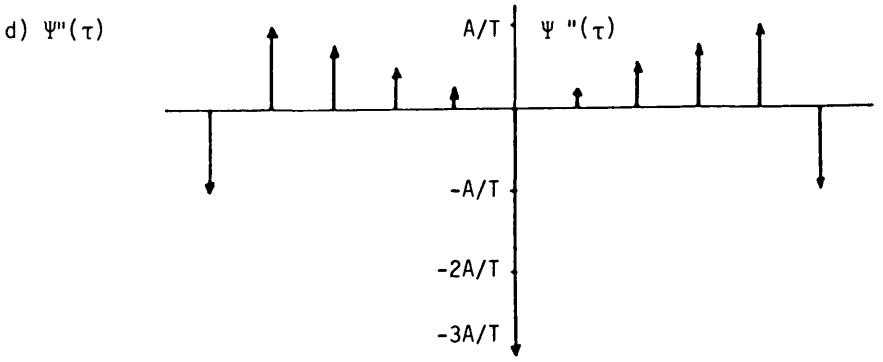
a) Seven levels sequence



b) Auto-correlation function $\Psi(\tau)$



c) $\Psi'(\tau)$



d) $\Psi''(\tau)$

Figure 4.5. Seven levels random binary code.

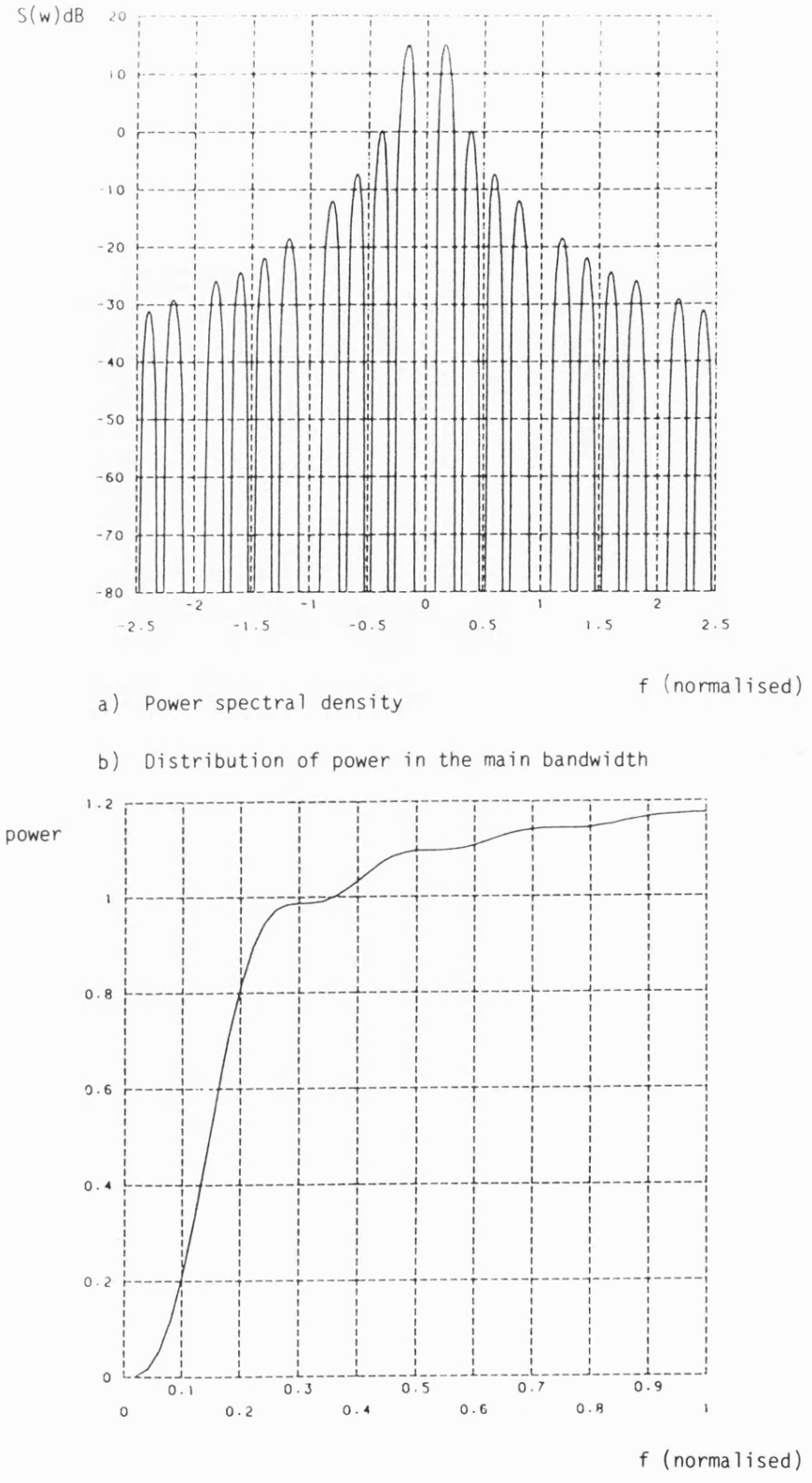


Figure 4.6. Power spectral density of seven levels sequence.

4.1.4 Utilisation of Multi-level Sequences in the Delay Lock Loop

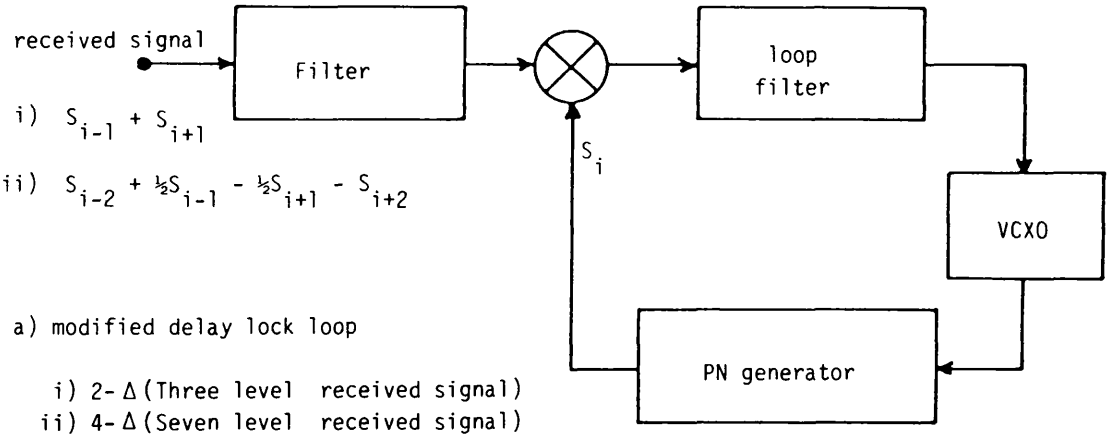
The modified output transmitted signal which has just been described, now no longer requires the several separate correlations in the delay lock loop. This is because part of this delay lock loop has been transferred from the receiver to the spread spectrum transmitter. This is possible because the spread-spectrum system is linear.

Figure 4.7(a) shows a modified delay lock loop capable of achieving synchronisation and maintain tracking for either of the transmitted signals described in Figure 4.4(a), for 2-Δ delay lock loop, or Figure 4.5(b), for 4-Δ delay lock loop. As it is seen from the figure, the loop has only one multiplier, one loop filter, one voltage controlled oscillator, and one local code generator, and has the structure of a phase lock loop with the exception of the type of signal used in each loop.

For the 2-Δ delay lock loop the received signal $[S_{i-1}-S_{i+1}+n(t)]$ correlated with a single local code sequence S_i to produce the 2-Δ N-shaped error curve needed to control the clock of the voltage controlled oscillator as shown in Figure 4.7(b).

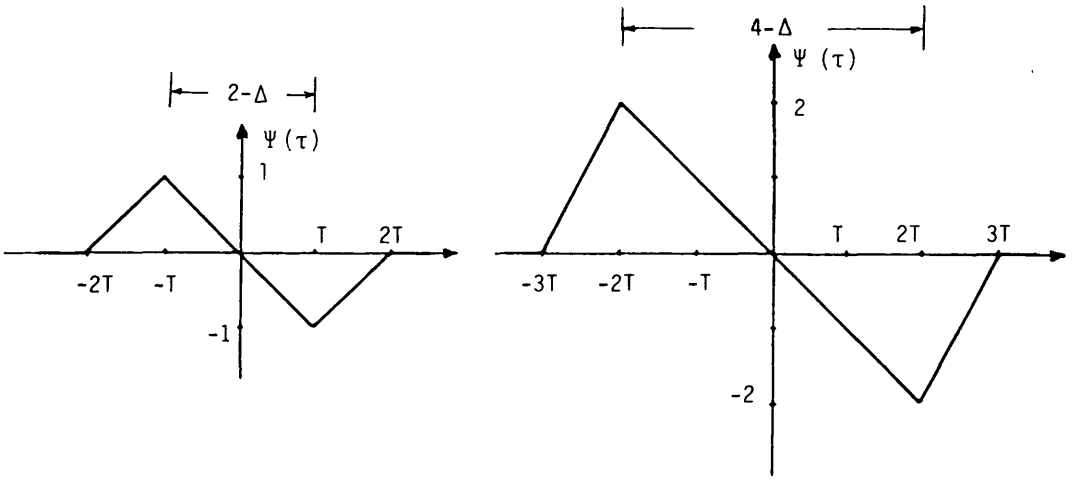
For the 4-Δ delay lock loop the received signal $[S_{i-2}+\frac{1}{2}S_{i-1}-\frac{1}{2}S_{i+1}-S_{i+2}+n(t)]$ is also correlated with a single local code sequence S_i to produce the 4-Δ N-shaped error curve needed as shown in Figure 4.7(b).

The noise term n(t) is also multiplied by a single local code sequence S_i and spread over wide bandwidth and removed by the narrow band loop filter, which also determines the dynamic behaviour and the constant parameters of the loop, such as loop bandwidth, natural



a) modified delay lock loop

i) 2-Δ (Three level received signal)
ii) 4-Δ (Seven level received signal)



b) N-shape error curves.

Figure 4.7. Simplified delay lock loop.

frequency of the loop, loop gain ... etc.

It is also clear that without any change in the simple structure of the loop, it is also possible to change from the 2-Δ to the 4-Δ loop in the receiver or vice versa simply by adding and subtracting the required advanced and/or delayed copies of the PN sequence to the transmitted signal **within the transmitter.** And this is an advantage when the synchronisation or the acquisition time is needed to be short, or in the case where an important message is to be transmitted or under high interference signal or high Doppler shift effect, where the improved acquisition time of the 4-Δ loop when used in noise can be fully exploited.

4.1.5 Experimental Implementation of the New System and the Results

The system is divided into two parts. The first part is the transmitter, in which the multi-level sequence is generated and transmitted while the second part is the receiver, in which a simple delay lock loop is established for synchronisation and tracking.

In the transmitter a maximal length sequence generator produces a sequence of 1023 bits length clocked at 1 Mbs^{-1}. Its experimental power spectral density is shown in Figure 4.8. The main lobe has a bandwidth of twice the clock frequency, i.e. $2x1Mbs^{-1}$

The three level sequence needed to produce 2-Δ DLL characteristics, i.e. $S_{i-1} - S_{i+1}$, is produced in the transmitter by the structure shown in Figure 4.7(a), and part of this sequence is shown in Figure 4.9(a).

The experimental power spectral density of the baseband signal is shown in Figure 4.9(b). This experimental power spectral density is seen to be identical to that calculated in the earlier section.

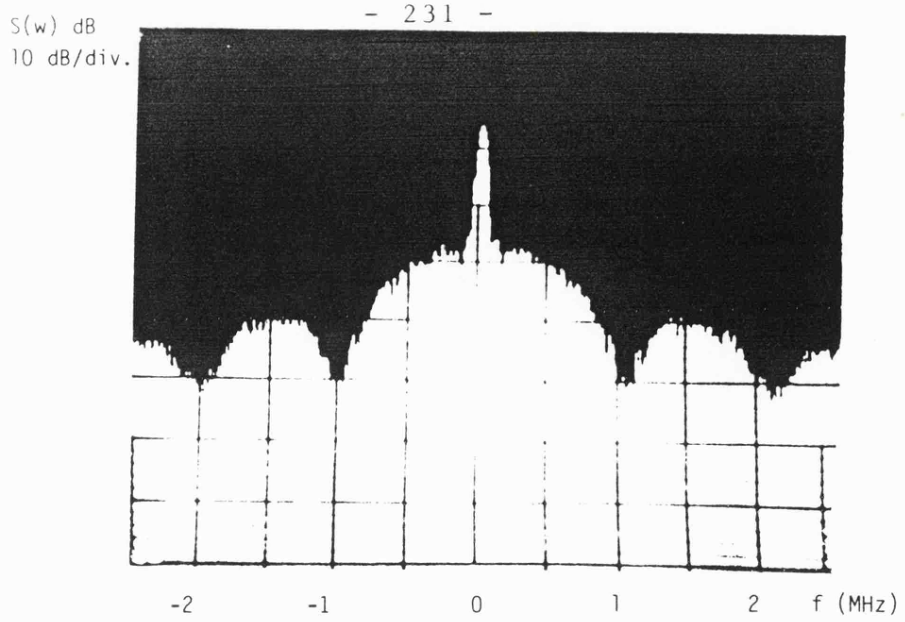
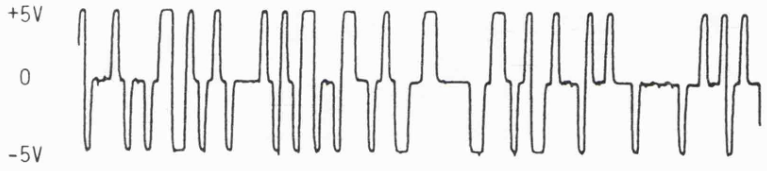
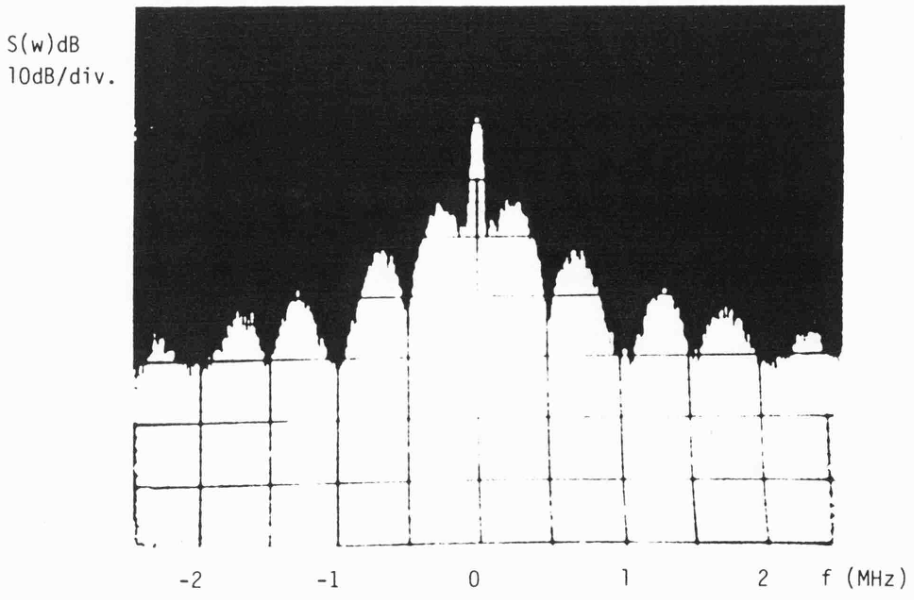


Figure 4.8. Experimental power spectrum of a standard 2-level sequence.



a) Three level sequence



b) Power sepctrum density.

Figure 4.9. Experimental waveform of three levels sequence.

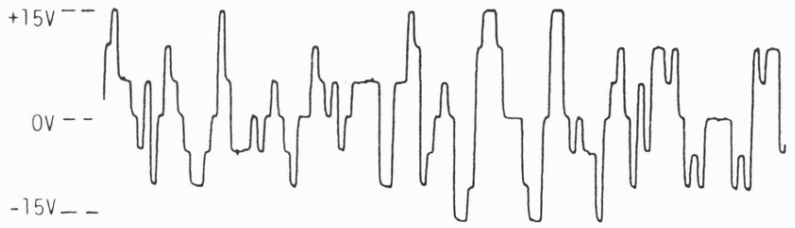
It also shows zero values at every $f_c/2$, that is 0, 0.5, 1, 1.5 ... Mbs^{-1}. This signal is transmitted to a 2-Δ delay lock loop receiver.

However, for the signal transmitted to a 4-Δ delay lock loop receiver, another two sequences are involved with the three level signal in accordance with the structure of Figure 4.4(b). A portion of this seven level resultant transmitted signal is shown in Figure 4.10(a), which consist of 7.5, 5, 2.5, 0, -2.5, -5, and -7.5 volts. Its experimental power spectral density, shown in Figure 4.10(b), is also identical to that calculated and shown in Figure 4.6(a). It has zero values at $f_c/4$, i.e. 0, 0.25, 0.5, 0.75, 1.0 ... Mbs^{-1}.

As it is seen in the earlier section, the delay lock loop in the receiver is quite simple. The same structure shown in Figure 4.7 is implemented here. A simple multiplier is used as a correlator for both 2-Δ and 4-Δ delay lock loop. In the experiments the natural frequency of the loop was taken to be 1 rad s^{-1}, and the damping factor is 0.707. Of course, the local code generator is identical to the transmitted one, and the sequence length is 1023 bits, clocked from the voltage controlled crystal oscillator at a frequency of 1.000002 Mbps for the 2-Δ loop and 1.000004 Mbps for 4-Δ loop to achieve the necessary sequence search rates.

The experimental N-shaped error curves for 2-Δ and 4-Δ delay lock loop are shown in Figure 4.11(a) and (b) respectively. These curves are plotted by opening the delay lock loop and with a slight offset between the received and the local frequency, and stored by a Nicolet digital storage oscilloscope.

The maximum slipping rate of this 2-Δ delay lock loop was found to be the same as for the standard 2-Δ loop described earlier, and it is equal to twice the natural frequency of the loop ($2xS_o$). The



a) Experimental seven levels sequence

b) Its experimental power spectral density.

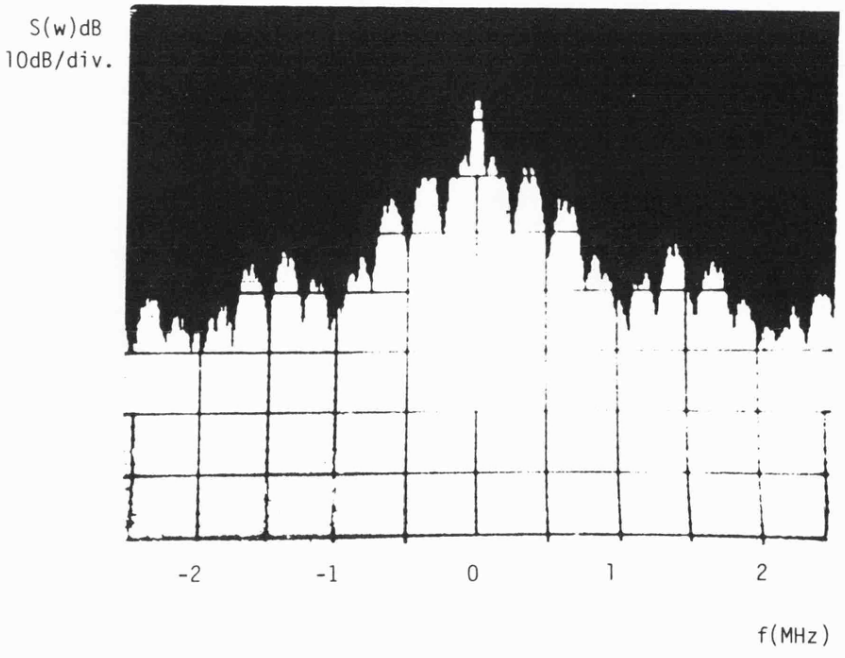
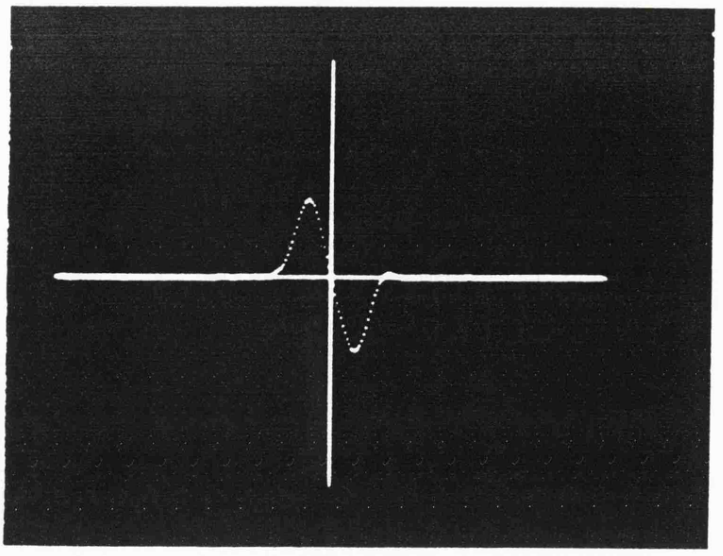
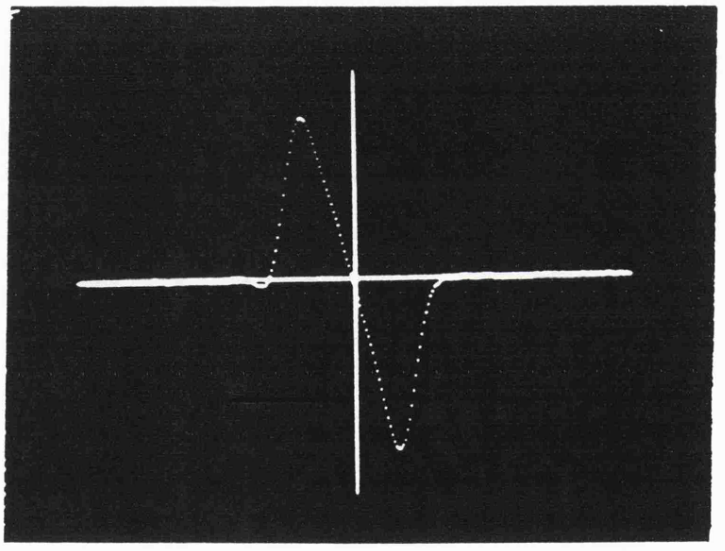


Figure 4.10. Experimental waveforms of the seven levels sequence.



a) 2-Δ DLL



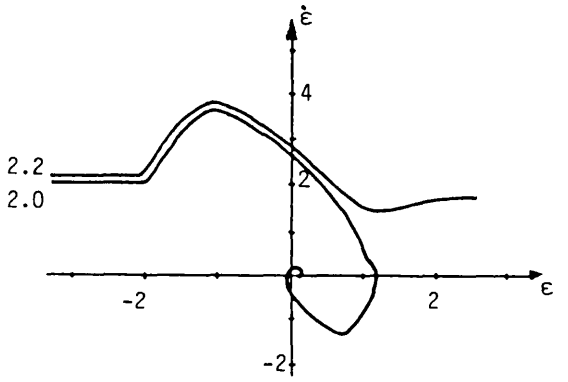
b) 4-Δ DLL

Figure 4.11. Experimental N-shape error curves.

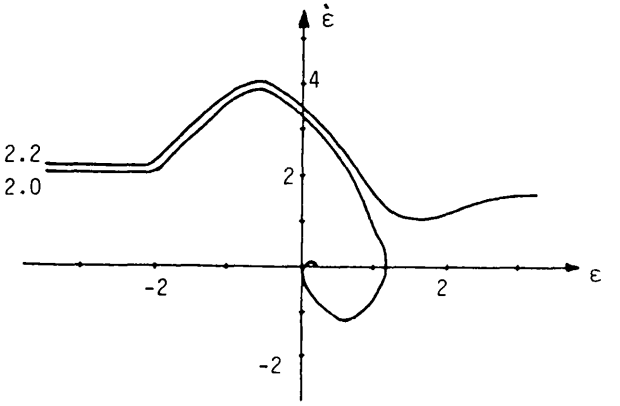
acquisition trajectories are shown in Figure 4.12(a,b,c), under three conditions. The first trajectory in (a) is for a pure input signal. The second trajectory in (b) where a weight Gaussian noise signal was added to the received signal such that the signal to noise ratio was -30.0dB. In (c) the signal to noise ratio was decreased to its minimum vlue of -35.0 dB without affecting the value of maximum allowable slipping rate. The noise and the signal power spectral density were shown in Figure 4.13(a,b) for SNR -30.0 and -35dB respectively. Note. No AGC is used in the receiver.

All the acquisition trajectories have clockwise movement, since when $\dot{\varepsilon}$ is greater than zero ε must increase, whereas when $\dot{\varepsilon}$ is less than zero ε must decrease. Clearly these acquisition trajectories are identical to those obtained previously discussed in Chapter Three for the "true" 2Δ and 4Δ loops and also those by Spilker [1], Nielsen [2], and Davies and Al-Rawas [3]. Although the acquisition trajectories are useful in the understanding of the acquisition process of a code tracking loop, they yield no information about the time taken to settle out the timing error to a small value. An important set of results were obtained on these delay lock loops. These were the maximum allowable search rate or slipping rate from which acquisition of lock could be obtained under both noise free conditions and low signal to noise ratio conditions.

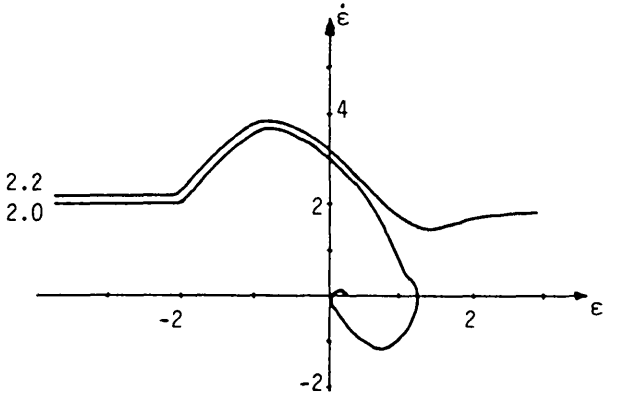
The maximum slipping rate of the simple $4\text{-}\Delta$ delay lock loop using the conventional, multi-arm correlator was found to be the same as that predicted theoretically, which is equal to 4x the natural frequency of the loop ($4 \times S_o$). The acquisition trajectories are shown in Figure 4.14 (a, b,c) for (a) pure input signal, (b) signal to noise ratio equal to -27.0 dB, and (c) minimum allowable signal to



a) No W.G. noise



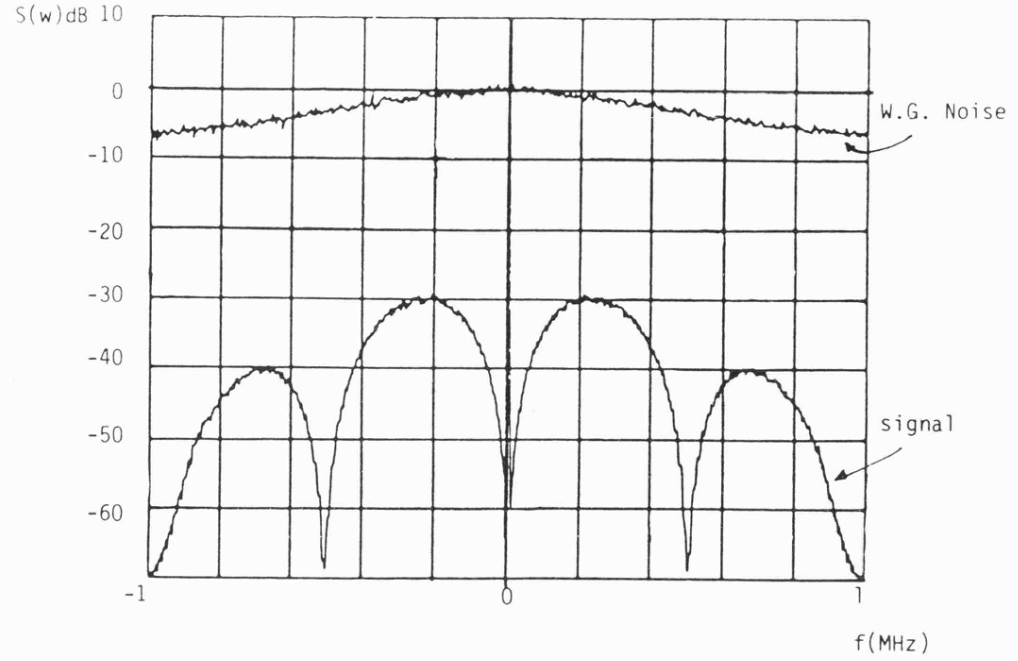
c) SNR = -35 dB



d) SNR = -30 dB

Figure 4.12. Experimental acquisition trajectories of the simple 2-Δ delay lock loop.

Note. No AGC is used in the receiver. Wanted signal power = 25×10^{-9} watts



a) 2-Δ, (S_{i-1} - S_{i+1}) and W.G. Noise, SNR = -30dB

b) 2-Δ, (S_{i-1} - S_{i+1}) and W.G. noise, SNR = -35dB

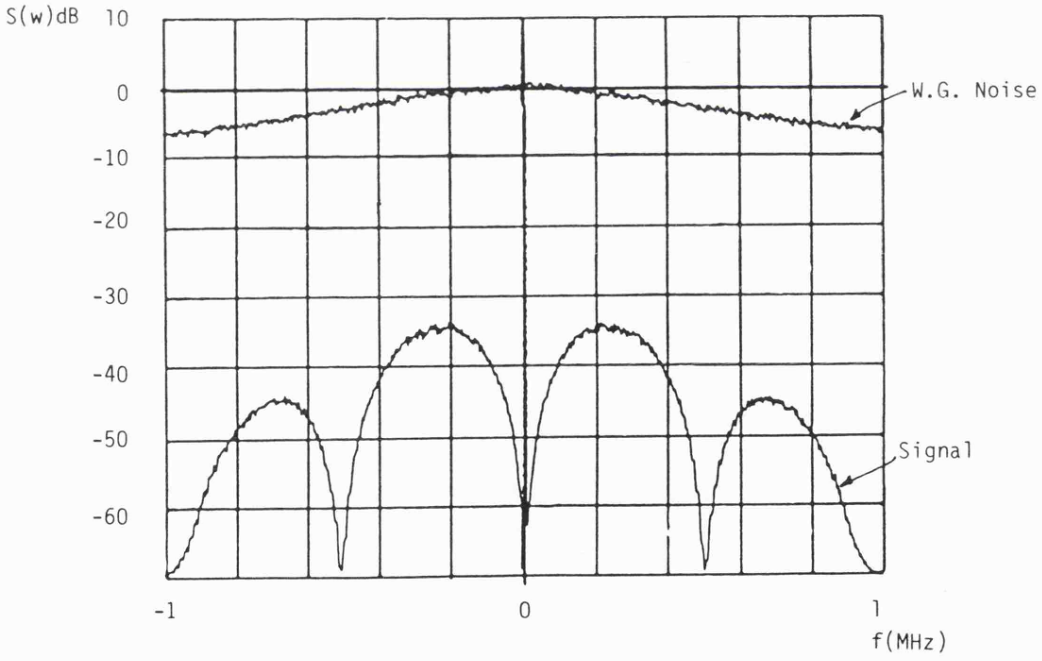
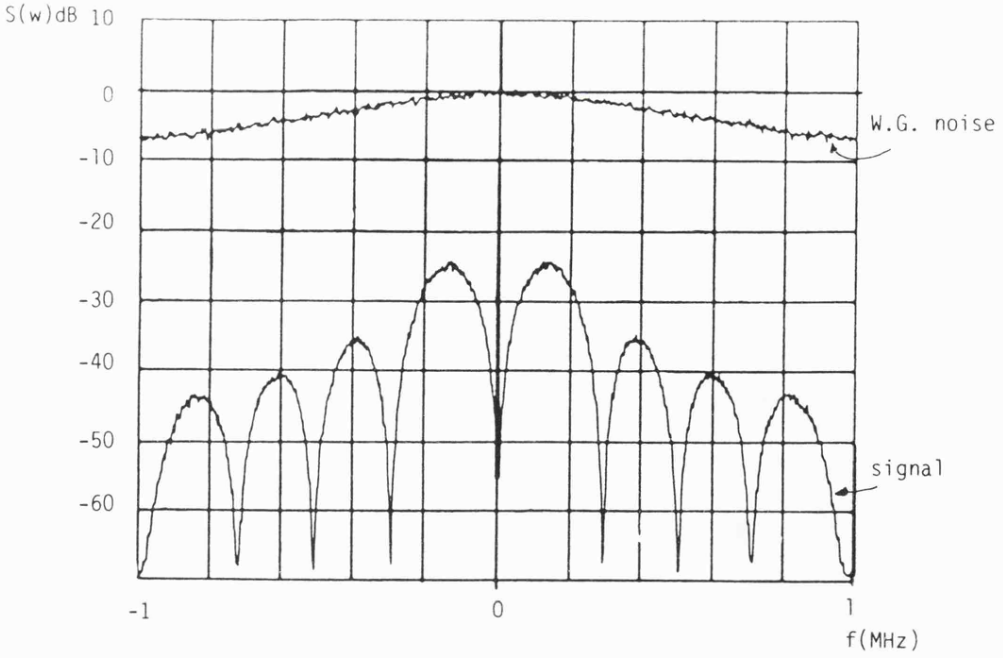


Figure 4.13. Measurements of signal to noise ratio by spectrum analyser.



c) 4-Δ, ($S_{i-2} + \frac{1}{2}S_{i-1} - \frac{1}{2}S_{i+1} - S_{i+2}$) and W.G. noise, SNR = -27dB

d) 4-Δ, ($S_{i-2} + \frac{1}{2}S_{i-1} - \frac{1}{2}S_{i+1} - S_{i+2}$) and W.G. noise, SNR = -30dB

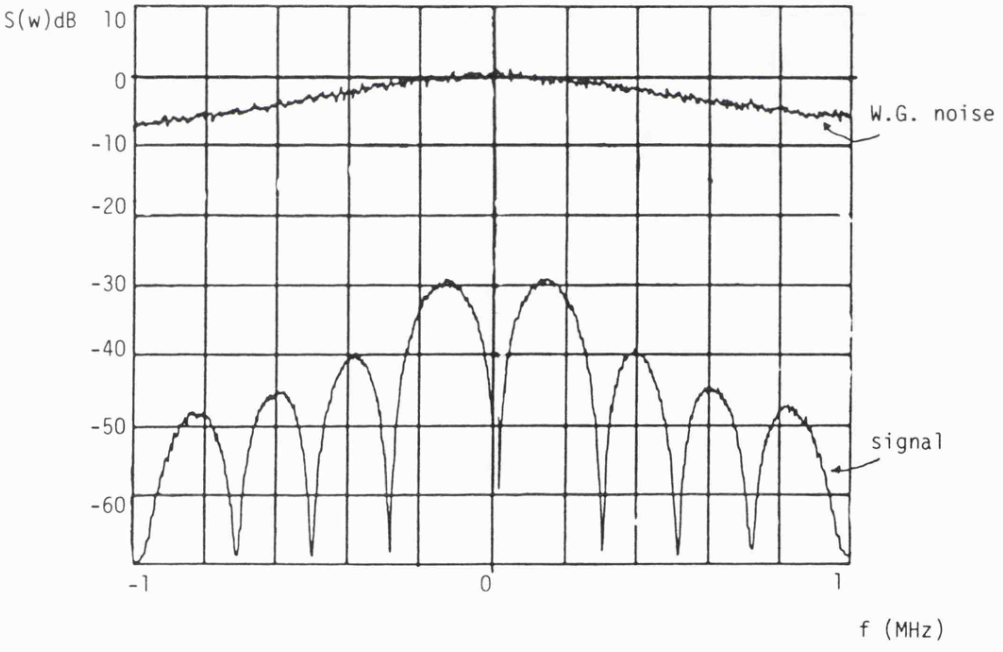
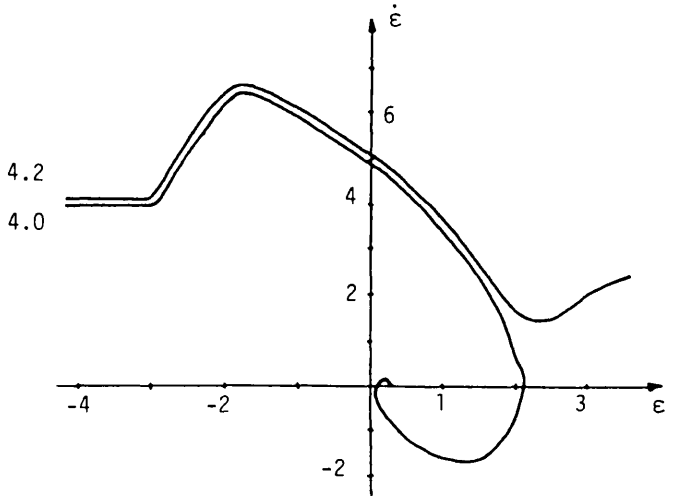
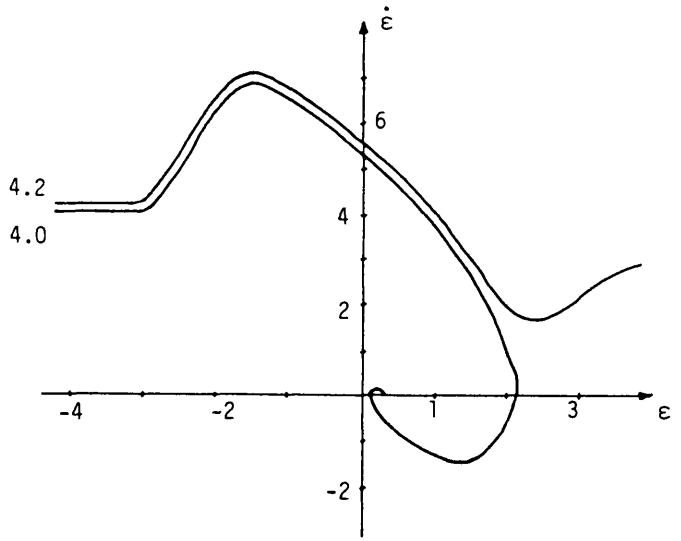


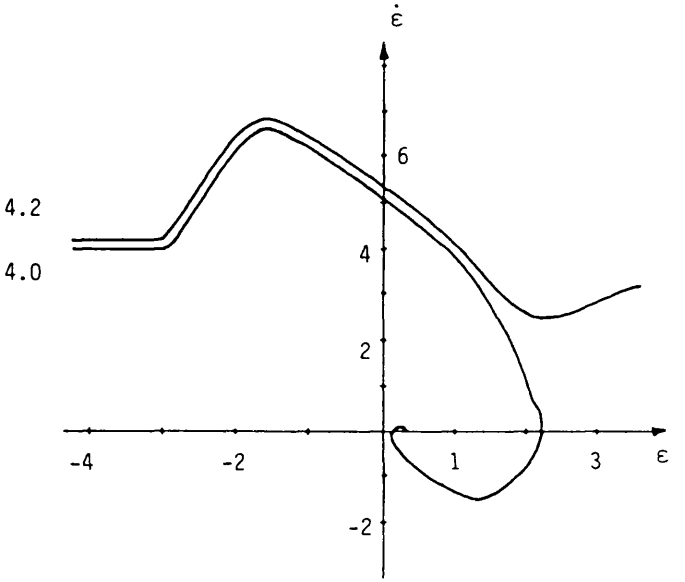
Figure 4.13 (Continued).



a) No W.G. Noise



b) SNR = -27 dB



c) SNR = -30 dB

Figure 4.14. Experimental acquisition trajectories of the simple 4-Δ delay lock loop.

Note. No AGC is used in the receiver.

noise ratio of -30.0dB which permit lock-on at slip rate equal to $4x\omega_o$. These power spectral densities of the signal and noise were shown in Figure 4.13 (c,d) respectively. Of course this delay lock loop permits displacement of $\pm 2\Delta$ between the received signal and the locally generated sequence.

For the 4-Δ delay lock loop, it is also possible to share the complexity between the transmitter and the receiver. Figure 4.15 shows an alternative 4-Δ system. The output transmitted signal in this case is:

$S_i + \frac{1}{2}S_{i-1} + S_{i-2}$ or it could be written as:

$S_{i+1} + \frac{1}{2}S_i - S_{i-2}$

This is a six level signal whose autocorrelation function is shown in Figure 4.16(a).

In the receiver, this six level signal can now be correlated with $(S_{r-1} - S_{r+1})$ instead of S_i to produce the 4-Δ wide N-shape error curve, as follows:

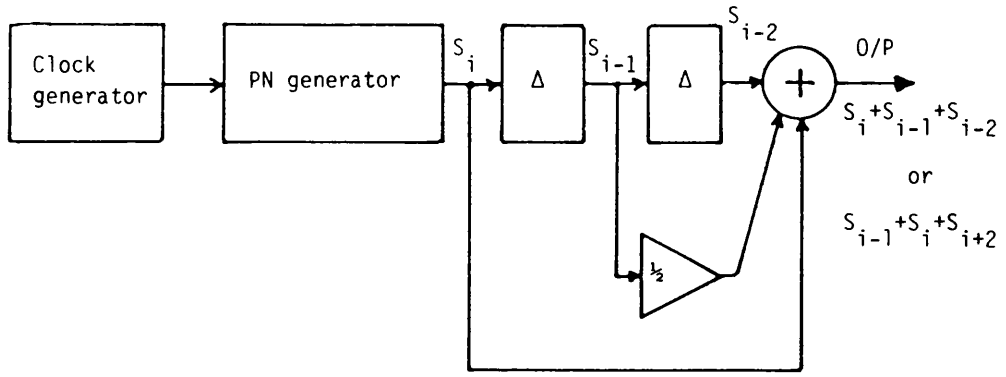
Let the correlation between two sequences S_i and S_r be denoted by $S_i * S_r$.

$$\text{error curve} = \sum(S_{i-1} + \tfrac{1}{2}S_i + S_{i+1}) * (S_{r-1} - S_{r+1})$$

$$= \sum(S_{i-1} * S_{r-1} + \tfrac{1}{2}S_i * S_{r-1} + S_{i+1} * S_{r-1} - S_{i-1} * S_{r+1} - \tfrac{1}{2}S_i * S_{r+1} - S_{i+1} * S_{r+1})$$

The correlation of the first term $S_{i-1} * S_{r-1}$ is identical to the correlation function of the last term $S_{i+1} * S_{r+1}$. So these terms cancel each other. Hence:

$$\text{error curve} = \sum(S_{i+1} * S_{r-1} + \tfrac{1}{2}S_i * S_{r-1} - \tfrac{1}{2}S_i * S_{r+1} - S_{i-1} * S_{r+1}) \qquad 4.7$$



a) Transmitter (six lvels sequence generator).

b) Receiver (4-Δ delay lock loop)

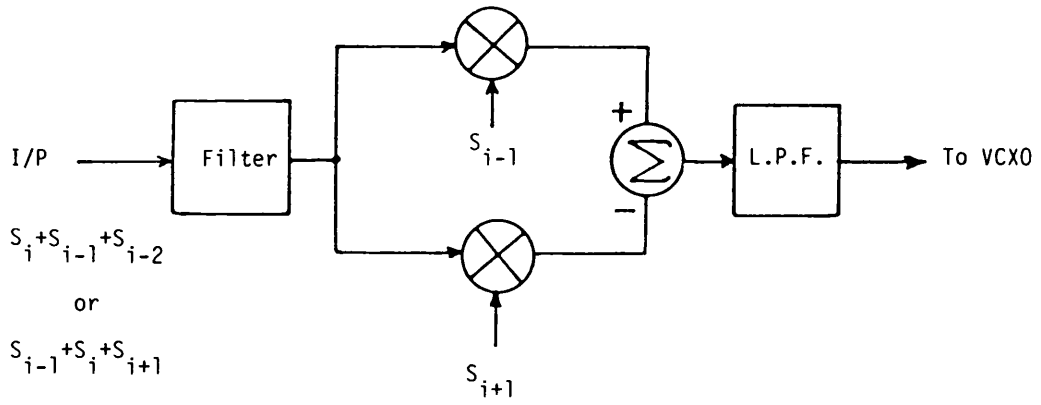


Figure 4.15. Alternative 4-Δ system.

The error curve produced here is exactly the same as the one produced earlier for the 4-Δ delay lock loop. Therefore the acquisition trajectories should also be exactly the same. The main advantage obtained by this modification is that without any changes to the original standard 2-Δ delay lock loop discussed earlier in Chapter Three, which employs only two locally generated sequences S_{i+1} and S_{i-1}, this loop can now generate a 4-Δ wide N-shape error curve if it is used to receive this new six level transmitted signal. Of course, as a result, the new maximum initial search rate could now be increased to $4.0\omega_n$ instead of $2.0\omega_n$.

The power spectral density of the new six level transmitted signal can be calculated from the auto-correlation function of the signal (shown in Figure 4.16(a)) as follows:

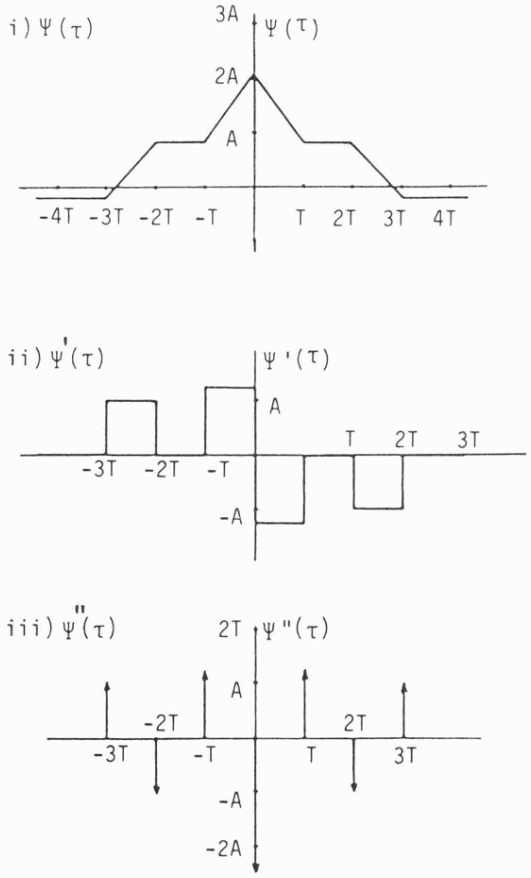
$$S(\omega)=\frac{A}{j^2\omega^2T}\left[2\left(\frac{e^{j3\omega T}+e^{-j3\omega T}}{2}\right)-2\left(\frac{e^{j2\omega T}+e^{-j2\omega T}}{2}\right)+2.5\left(\frac{e^{j\omega T}+e^{-j\omega T}}{2}\right)-2.5\right]$$

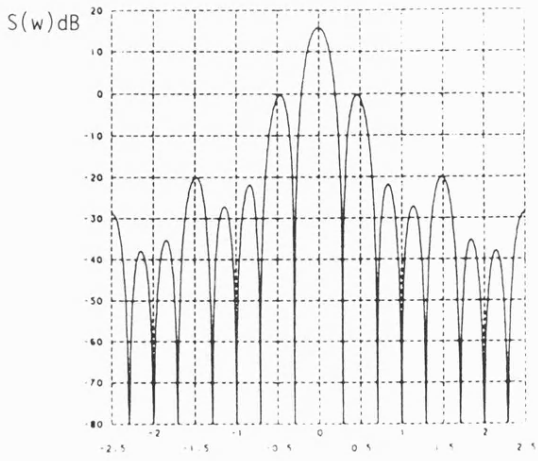
$$=\frac{A}{j^2\omega^2T}\left[2\ \mathrm{Cos}\ 3\omega T-2\ \mathrm{Cos}\ 2\omega T+2.5\ \mathrm{Cos}\ \omega T-2.5\right]$$

$$=AT\left[9\left(\frac{\mathrm{Sin}\ 3\omega T/2}{3\omega T/2}\right)^2+4\left(\frac{\mathrm{Sin}\ \omega T}{\omega T}\right)+1.25\left(\frac{\mathrm{Sin}\ \omega T/2}{\omega T/2}\right)\right]$$

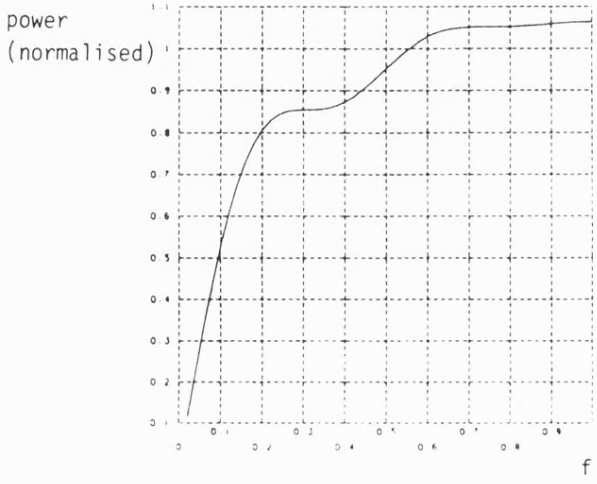
The calculated power spectral density of this signal is shown in Figure 4.19. The total power in the main bandwidth i.e. 2 x f_c is shown to be equal to 2.35 times the total power in the same bandwidth of the original standard spread spectrum spectral density. This is shown in figure 4.16(c).

a) Auto-correlation function of six levels sequence





b) Power spectral density of the six level sequences



c) Distribution of power in the main bandwidth

Figure 4.16. Six levels sequence auto-correlation function and power spectral density

4.2 HIGH PERFORMANCE NEW SPREAD SPECTRUM SYSTEM

4.2.1 Introduction

As seen earlier, the spread spectrum system has the ability to reject large levels of interference and also jamming signals, due to its high process gain, which has been defined as:

$$G_p \text{ (dB)} = 10 \log_{10} \frac{BW_t}{BW_d} \qquad 4.8$$

When the sequence is a maximal length sequence the main lobe bandwidth of the power spectral density has the form $(\sin x/x)^2$ is twice the clock rate of the code sequence. Each of the sidelobes has a bandwidth from null-to-null which is equal to the clock rate. The $(\sin x/x)^2$ distribution results in relatively high power in the sidebands. Therefore the power in these sideband lobes could cause interference in adjacent spread spectrum channels [4,5]. In addition to that this also decreases the process gain by a small amount because not all the power is confined to the main lobe.

$$SNR_{out} = \frac{P}{P_i} \left(\frac{BW_t}{BW_d}\right)$$

or

$$SNR_{out} = SNR_{in} \cdot G_p \qquad 4.9$$

where G_p is the process gain, P is the desired signal power, P_i is the interference power. The effective reduction of interference is due to: $\left(\frac{BW_d}{BW_t}\right)$

It is therefore important that the total power in the main bandwidth should be large and the power in the sidelobes negligible

for maximum process gain and for interference rejection. In order to prevent excess spectrum pollution only the main lobe of power spectrum distribution is allowed to be transmitted, and the sidelobes are filtered out. About 10 percent of the overall baseband signal power is contained in the sidelobes as shown in Figure 4.17, for a conventional direct sequence spread spectrum system using maximal length sequence. And this represents a potential loss in the transmitted signal power.

Usually the bandwidth of every receiver must be commensurate with the input signal bandwidth. However, this bandwidth in spread spectrum systems is very wide. Therefore the spread spectrum receiver has to accept more noise in exactly the same ratio as the increase in bandwidth.

The bandwidth of the receiver is usually taken to be equal to the main lobe of the $(\sin x/x)^2$ power spectral density which is equal to 2 times the clock frequency of the spreading code. However, Dixon [6] suggested that by judicious choice of the receiver bandwidth, more of the potential noise than signal itself could be rejected, and produce some gain. This is illustrated in Figure 4.18, which shows the percentage of the power distributed in the main lobe and the power of a white noise considered to be flat.

If the receiver bandwidth is kept to be equal to the main lobe bandwidth i.e. 2 times the clock rate, the receiver would accept all the noise and the input signal. However, if the receiver bandwidth is reduced to 60 percent of the main lobe bandwidth, the noise power would be reduced by 40 percent, while the input signal power would be reduced by only 10 percent of its original power, and that is

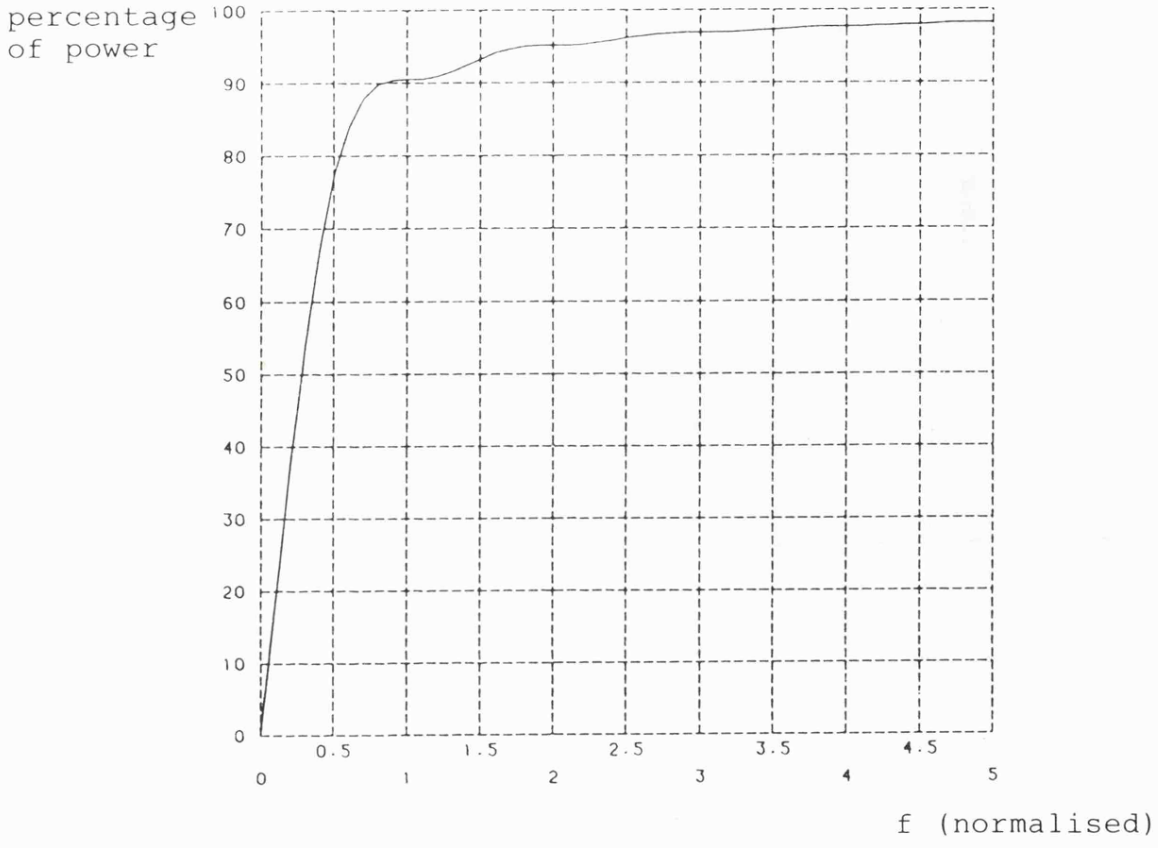


Figure 4.17. Percentage of power versus frequency of a standard two levels sequence.

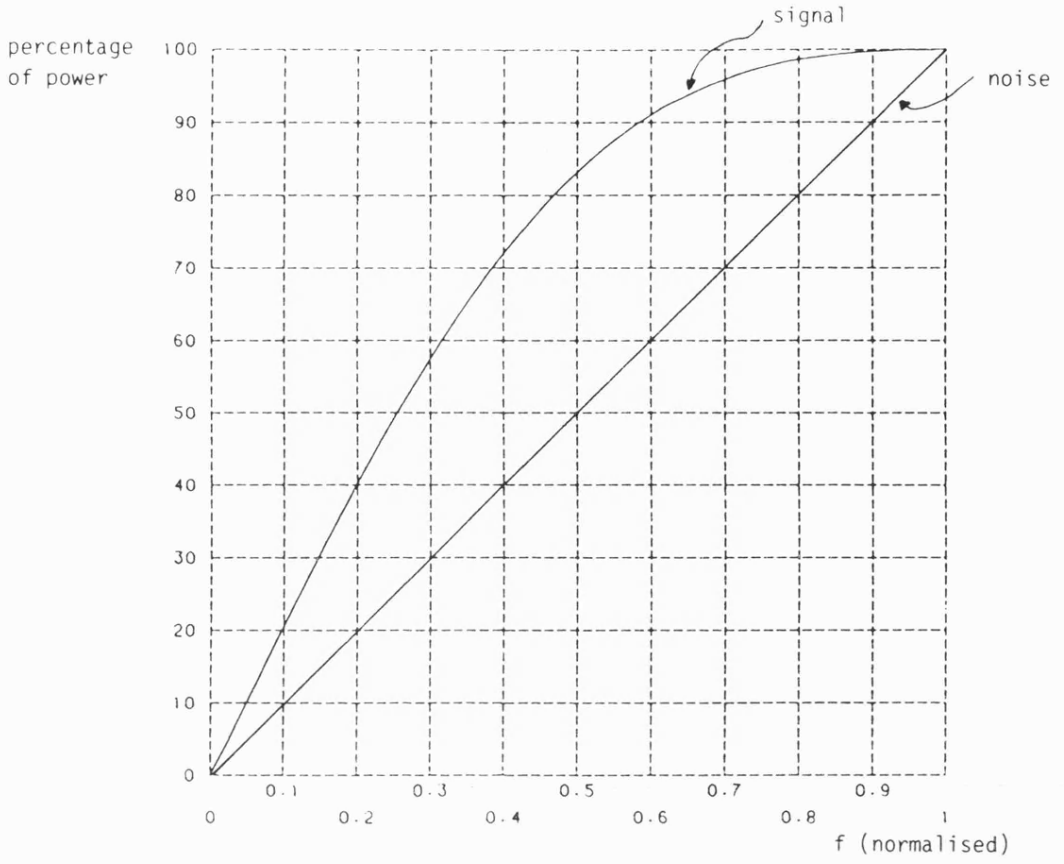


Figure 4.18 Percentage of power in the main lobe bandwidth.

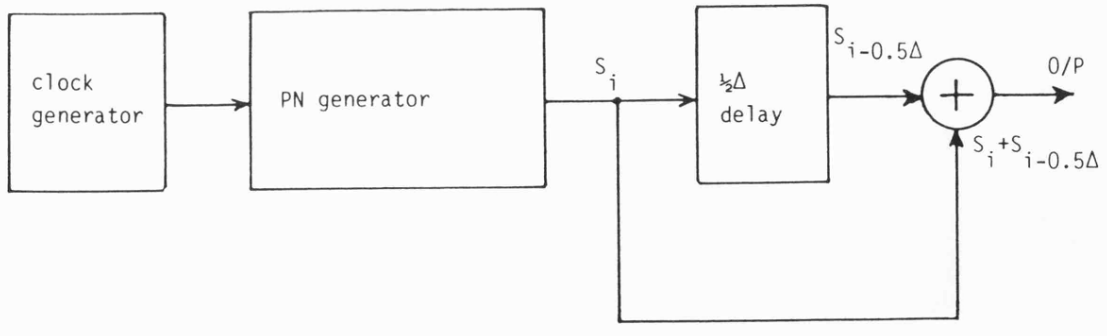


Figure 4.19. Block diagram of generating the modified spreading pseudonoise sequence.

considered to be the optimum reduction in the receiver bandwidth for optimum signal to noise ratio improvement.

In the following sections, the design and performance of a **new** spread spectrum system (both the transmitter and the receiver) is described. In particular, the advantage of increasing the transmitter power spectral density for better process gain, and decreasing the bandwidth of the receiver for a better signal to noise ratio are discussed. Some structures of the receiver indicate high performance from the synchronisation point of view, by decreasing the acquisition time of the delay lock loop and increasing the tracking limits as well as the Doppler-shift limit which keep the system in synchronisation and tracking mode. Some new delay lock loops appear to have a rather simple structure compared to their corresponding standard ones.

4.2.2 Transmitter Modification to Improve Spectrum Utilisation

Some advantages can be gained by modifying the power spectral density of the transmitted spread spectrum signal. By considering the following two relationships:

$$\Psi(\tau) = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} f(t) f(t+\tau) dt \qquad 4.10$$

$$S(\omega) = \int_{-\infty}^{\infty} \Psi(\tau)\, e^{-j\omega\tau}\, d\tau \qquad 4.11$$

it is seen, that the power spectrum density can be modified by modifying the auto-correlation function of the transmitted sequence.

Therefore, in this section, work is described on the modification of the transmitted signal so that it will give a better distribution of the power spectral density.

Figure 4.19 shows a block diagram of a method for generating the modified spreading pseudonoise sequence. Here the maximal length pseudonoise-sequence is first generated by the usual way via a feedback shift register. Then it was delayed by half bit, and added to the original sequence to form the modified three level signal required for the new system. The auto-correlation function of this signal has a wider base than the original standard one which is equal to 3T instead of 2T, and its amplitude is three times higher as shown in Figure 4.20(a).

The data could be modulated on the pseudonoise sequence by the same way as was described previously, except that a modulo-2 adder, has to be replaced by a true analogue multipler because of the three level sequence now involved in the process.

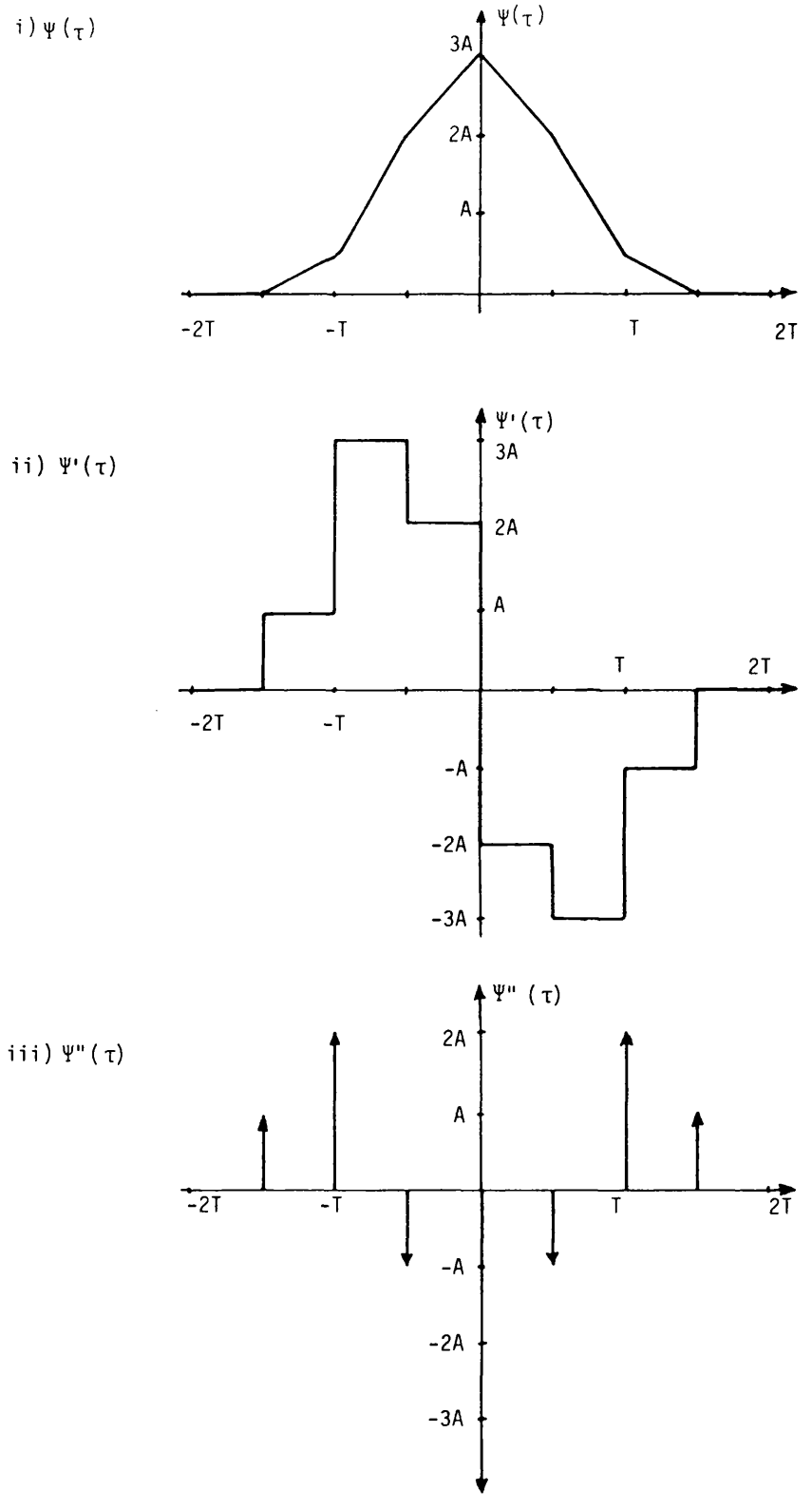
The new power spectral density of the modified transmitted signal from the auto-correlation function, shown in Figure 4.22 (b), is:

$$S(\omega) = \frac{2A}{j^2\omega^2T}\left[\left(\frac{e^{j1.5\omega T}+e^{-j1.5\omega T}}{2}\right)+2\left(\frac{e^{j\omega T}+e^{-j\omega T}}{2}\right)-\left(\frac{e^{j0.5\omega T}+e^{-j0.5\omega T}}{2}\right)-2\right]$$

$$= \frac{2A}{j^2\omega^2T}\left[\text{Cos } 1.5\omega T + 2 \text{ Cos } \omega T - \text{Cos } 0.5\omega T - 2\right]$$

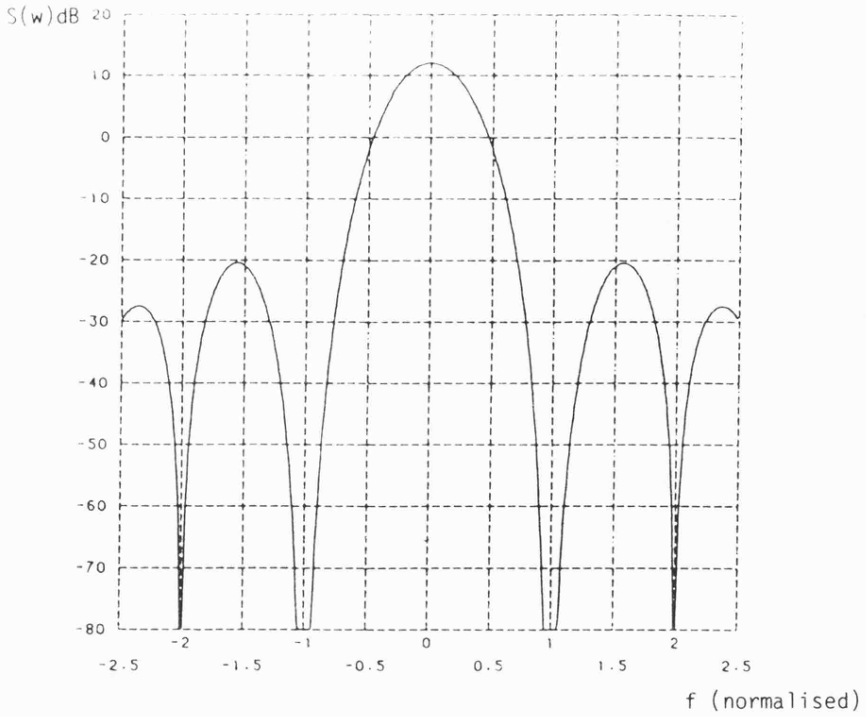
$$S(\omega) = 2AT\left[1.125\left(\frac{\text{Sin } 0.75\omega T}{0.75\omega T}\right)^2 + \left(\frac{\text{Sin } 0.5\ \omega T}{0.5\omega T}\right)^2 - 0.125\left(\frac{\text{Sin } 0.25\omega T}{0.25\omega T}\right)^2\right] \qquad 4.12$$

The power spectral density is calculated and shown in Figure 4.20(b). The null to null bandwidth or the main lobe bandwidth is also two times the clock frequency of the feedback shift register which generates the pseudonoise code sequence which is to be expected

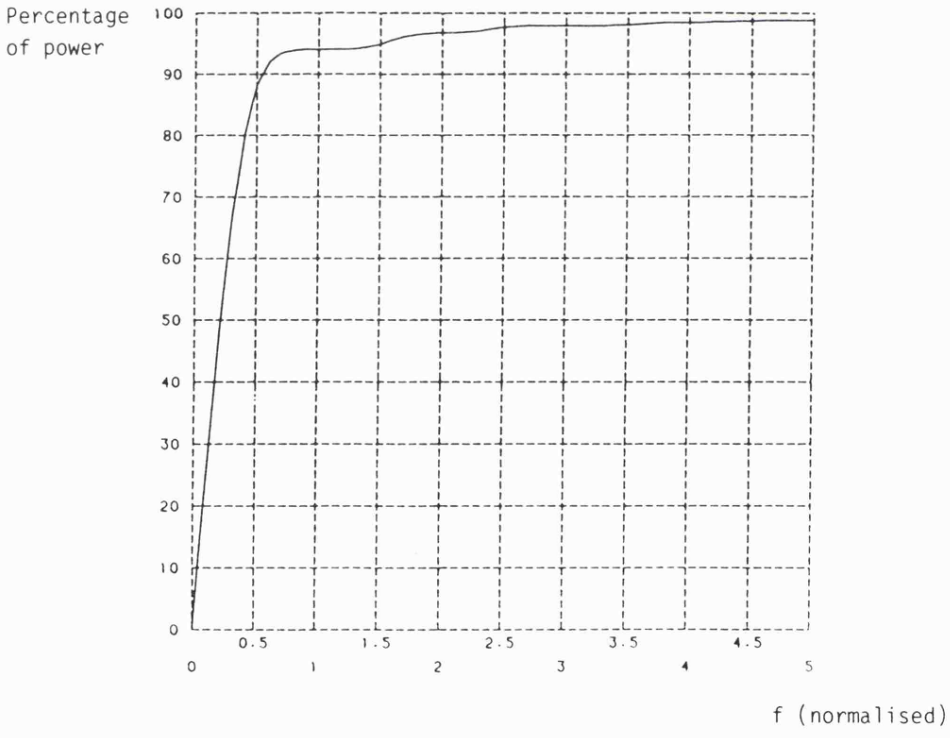


a) Auto-correlation function of the modified 0.5-Δ shift sequence.

Figure 4.20. Modified 0.5-Δ shift three level sequence's auto-correlation function and its power.

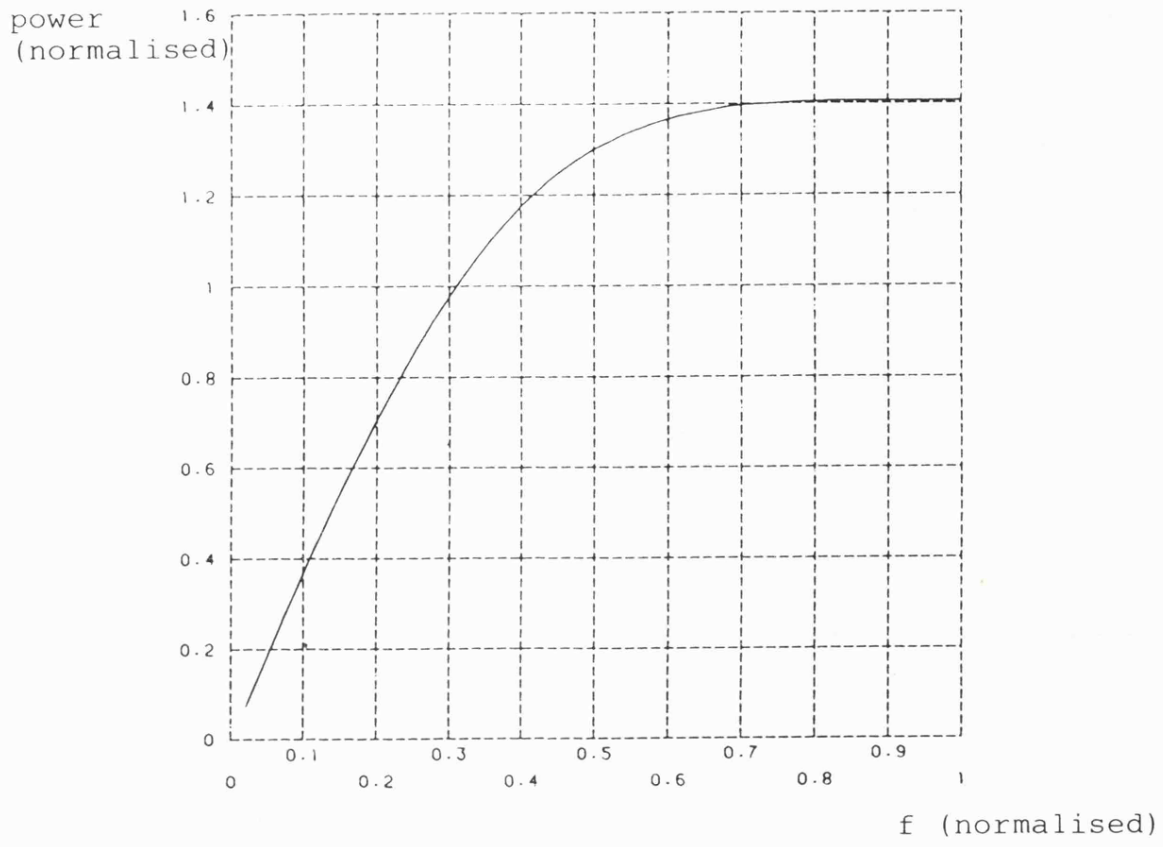


b) Power spectral density



c) Percentage of power versus frequency

Figure 4.20 (Continued).



d) Distribution of power in the main lobe bandwidth.

Figure 4.20 (Continued).

because the three level sequence is effectively clocked at twice the rate of the normal sequence. But here the distribution of the power spectral density is different from the standard one described earlier, more power being transferred from the side lobes to the main lobe. It is clear from Figure 4.20(c), that now only about 6 percent of the power is distributed in the side lobes instead of 10 percent for the standard one.

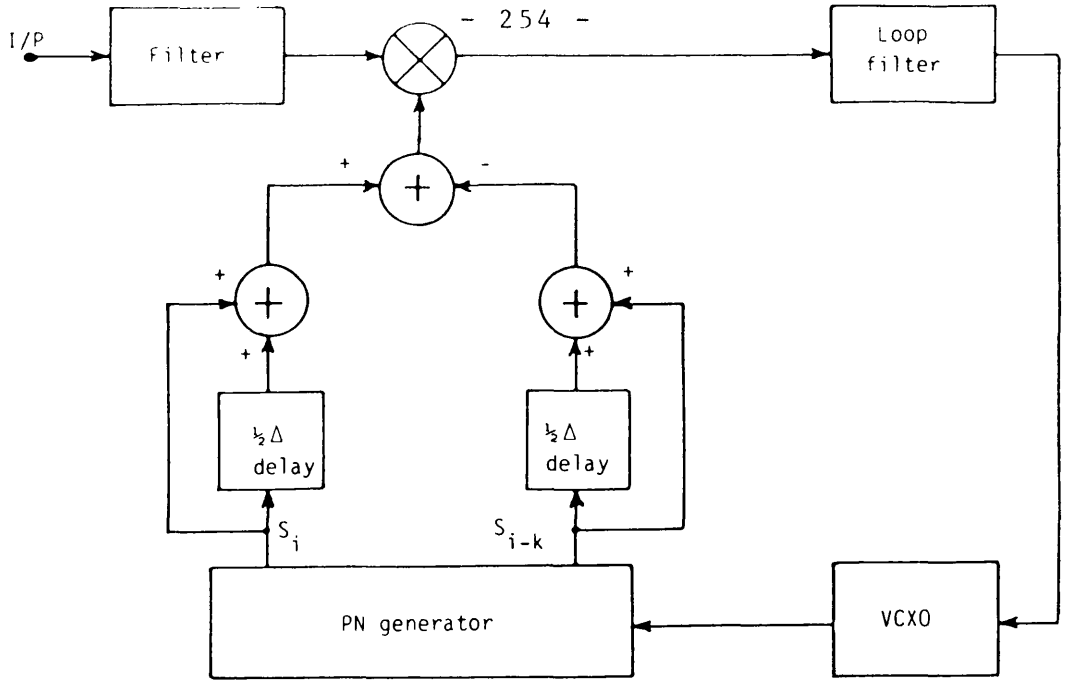
This indicates that 4 percent more power is contained in the main lobe. This can be used to improve the signal to noise ratio of the spread spectrum system. Another advantage is that the interference to the adjacent channel is also reduced.

Other advantages concerning the delay lock loop in the receiver using this type of multi-level sequence, such as, its N-shaped error curve, acquisition time or maximum search rate for the new signal will be discussed in the next section.

4.2.3 Delay Lock Loop Using Modified Sequence

In order to receive the modified transmitted signal described in the previous section, a modification to the existing delay lock loop is necessary. Figure 4.21 shows block diagrams of possible two modified versions of the delay lock loops used to synchronise the new incoming signal. Only the correlation circuit is slightly different from the standard one. The structure of Figure 4.21 (b) has less hardware than that of (a) but the functions of both loops are the same.

Although the general structure of this delay lock loop is the same as the previous one, its tracking range, the N-shape error curve, the search rate, and more importantly, the signal to noise



a) modified delay lock loop

b) Simple modified delay lock loop

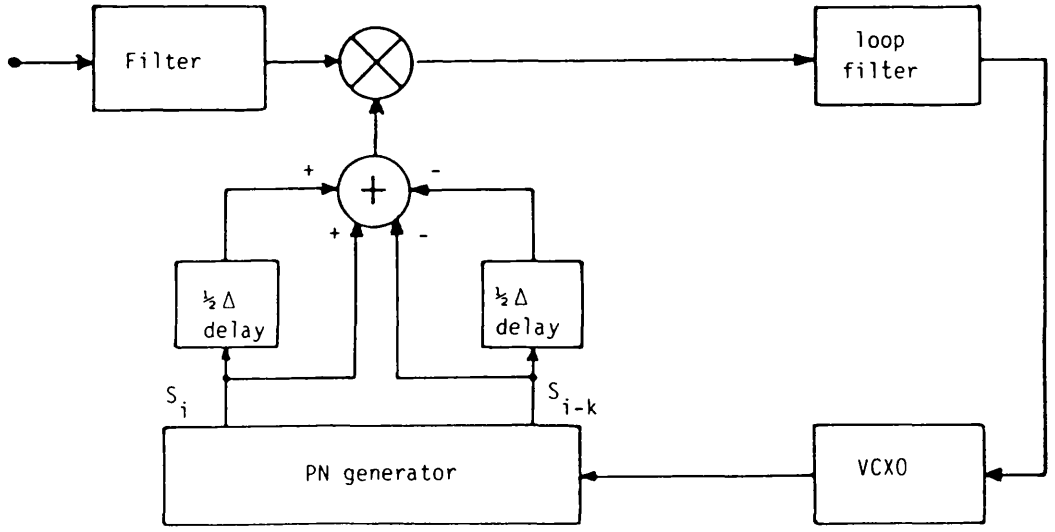


Figure 4.21. Block diagram of the modified delay lock loop.

i) k = 3 for 2-Δ delay lock loop.

ii) k = 2.5 for 2-Δ delay lock loop.

iii) k = 2 for 2-Δ delay lock loop.

ratio capability are different. From the structure shown in Figure 4.21, three different widths of delay lock loops could be established for different time displacement K of the locally generated sequences (S_i and S_{i-K}). From (S_i and S_{i-3}),(S_i-$S_{i-2.5}$), (S_i and S_{i-2}), for example, 3-Δ, 2.5-Δ, and 2-Δ delay lock loops, respectively, could be designed.

The N-shaped error curves of these loops, are shown in Figure 4.22. In each of these cases the locally generated sequence is added to a 1/2 bit delayed version of itself to form the correlation necessary to develop the error curve which is required in a particular delay lock loop.

The acquisition trajectories of the 3-Δ, 2.5-Δ, and 2-Δ delay lock loop were computed and shown in Figure 4.23. The maximum slipping rate of the 3-Δ loop was found to be equal to 5.5 times the natural frequency of the loop. Clearly this is much higher than the maximum slipping rate of the standard 4-Δ delay lock loop described earlier which has a maximum slipping rate of 4.0 times the natural frequency of the loop. However, for 2.5-Δ delay lock loop the maximum slipping rate is less, and it is equal to 3.0 times the natural frequency of the loop. But, there is no advantage, from the maximum slipping rate point of view for the modified 2-Δ delay lock loop, as it is reduced from 2.0 for the standard 2-Δ loop to 1.7 for the 2-Δ modified loop using the modified sequence. However, there is another important advantage concerning the signal to noise ratio which will be discussed shortly.

It is important to say here that all these acquisition trajectories are computed according to the condition that the slope

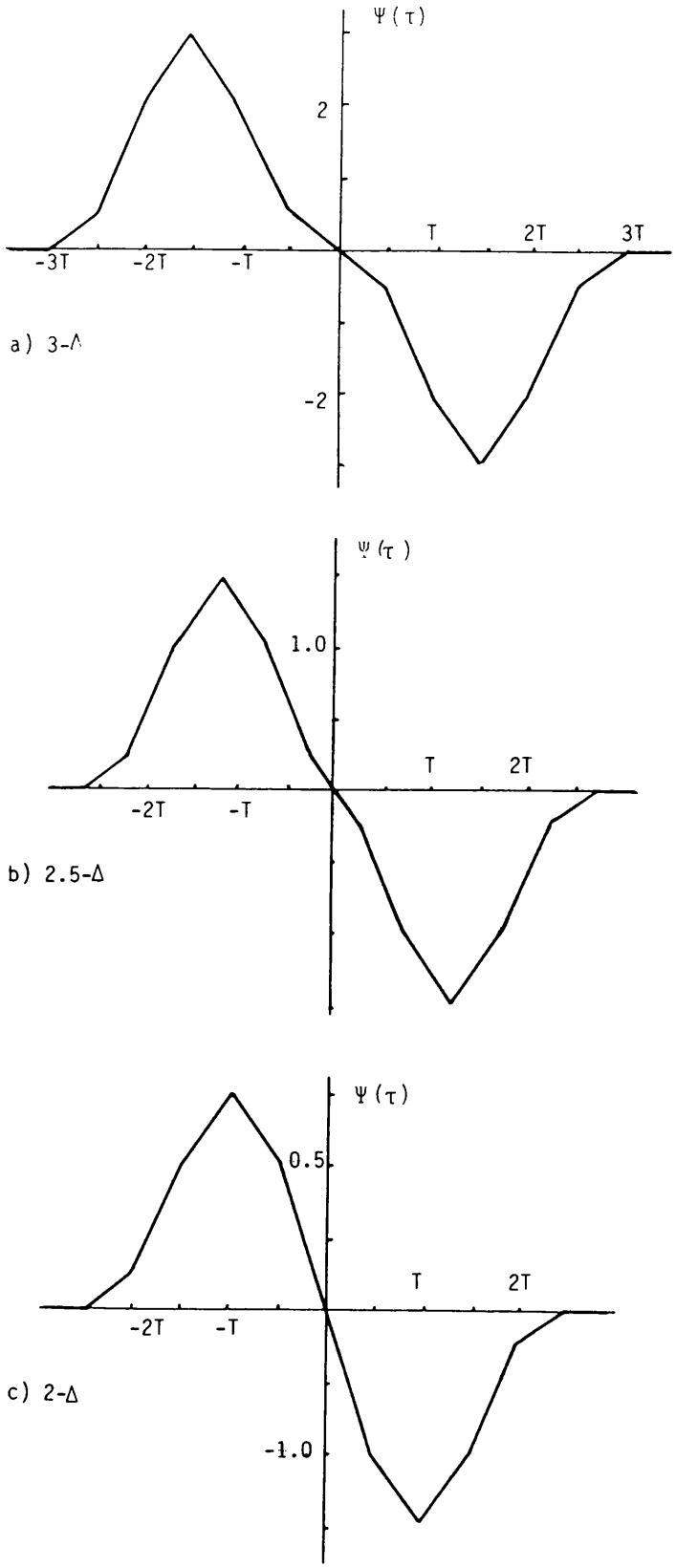
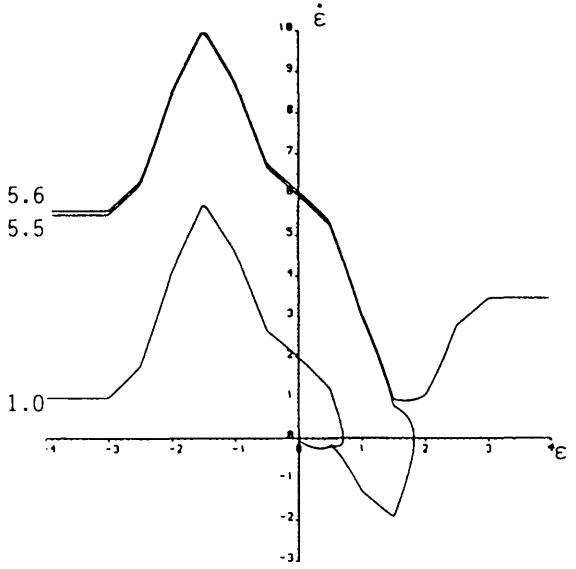
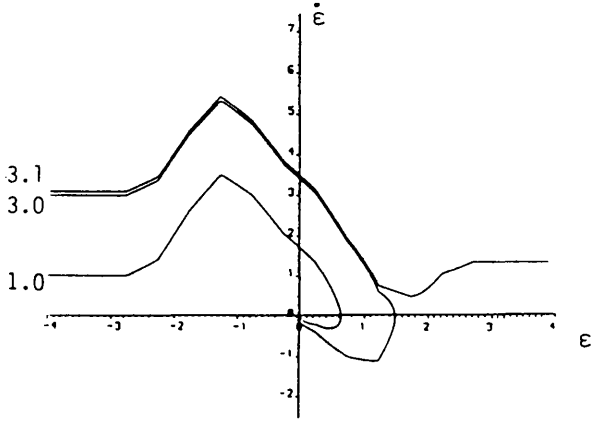


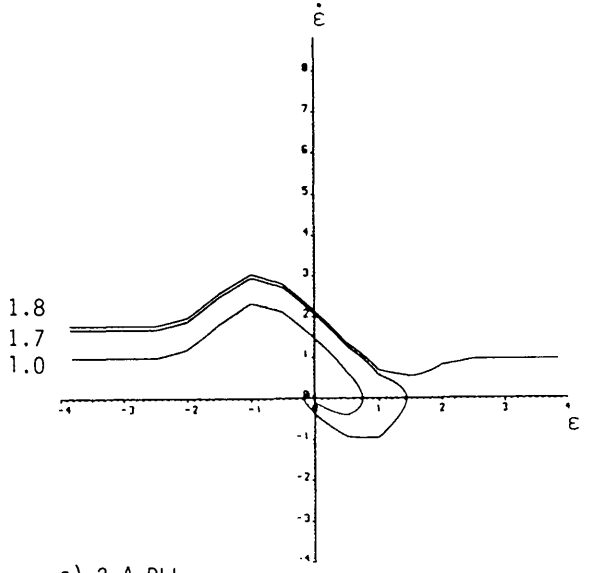
Figure 4.22 Modified N-shape error curve.



a) 3-Δ DLL



b) 2.5-Δ DLL



c) 2-Δ DLL

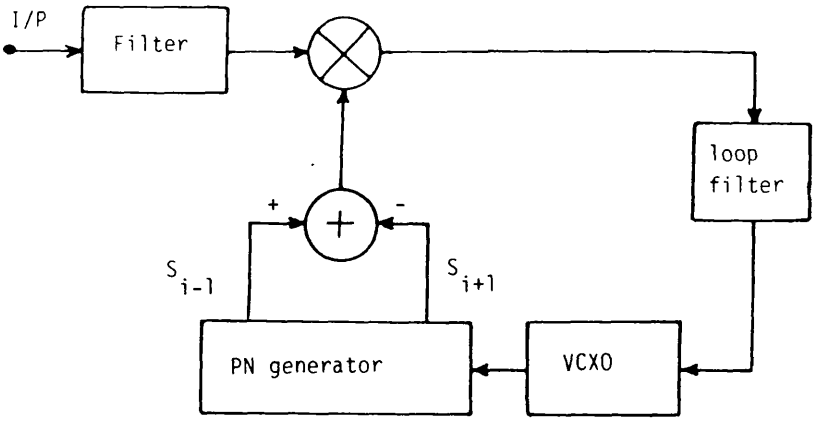
Figure 4.23. Theoretical acquisition trajectories of the modified delay lock loop

of the error curves is xl near the origin (i.e. when the time displacement ε is small) [2], and to ensure that the same gain at $\varepsilon = 0$ is used for all the various discriminator characteristics during computation. This explains why the maximum slipping rate of the last delay lock loop has dropped to 1.7.

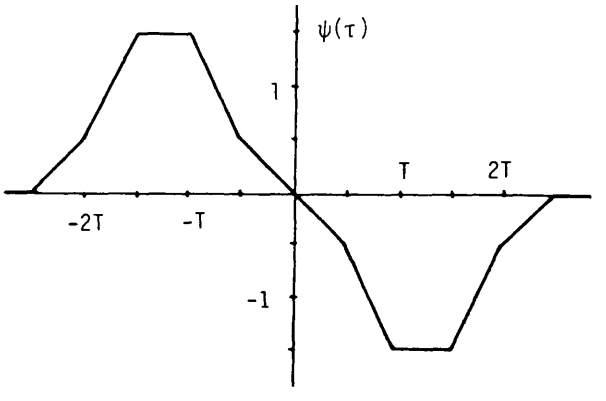
It is also possible to receive the new transmitted signal without any modification to the standard 2 DLL. This is shown in figure 4.24. It was found that a higher maximum slipping rate could be achieved with the new multi-level transmitted signal. This was found to have a maximum search rate of 3.3 times the natural frequency of the loop instead of only 2.0, as shown in Figure 4.24(c).

It is worth noting that the N-shape error curve for this 2-Δ delay lock loop has a flat top and bottom peaks of width $1/2\Delta$ each, and the actual tracking range is beween $\pm\Delta$ as shown in Figure 4.24(b).

To construct a 1-Δ delay lock loop working with the new transmitted signal, only one locally generated reference is taken from the pseudo-noise generator and then subtracted from a 1/2 bit delayed version of itself. The resultant signal is then multiplied by the received signal to develop the error curve needed, as shown in Figure 4.25(b). This time, exactly the same error curve is developed which is similar to a standard 1-Δ loop working with a standard binary maximal sequence. The same acquisiton trajectory is thus to be expected wih a maximum slipping rate of 1.0 times the natural frequency of the loop, and configuration of this is shown in Figure 4.25(c).



a) Block diagram



b) 2-Δ N-shape error curve.

c) Acquisition trajectories

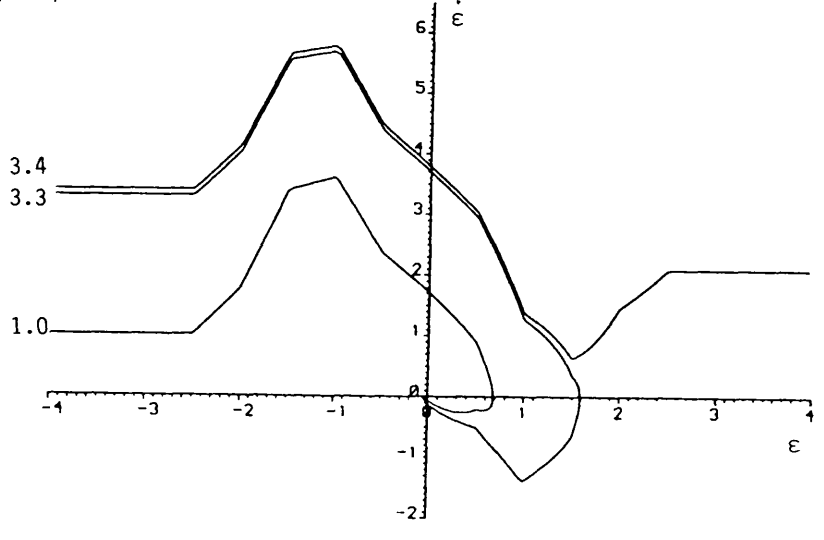
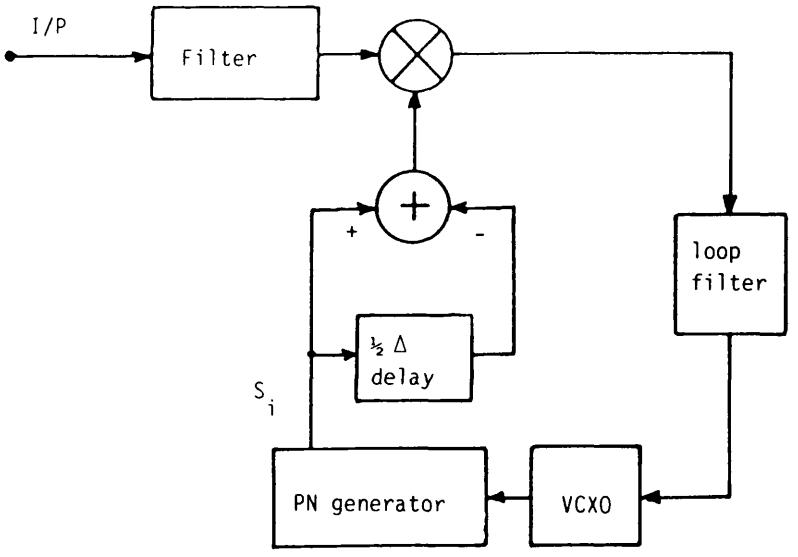
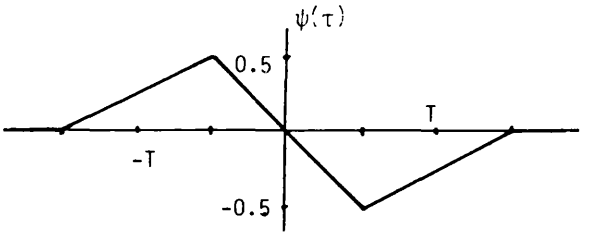


Figure 4.24. Alternative 2-Δ modified delay lock loop.



a) Block diagram



b) 1- N-shape error curve

c) Acquisition trajectories

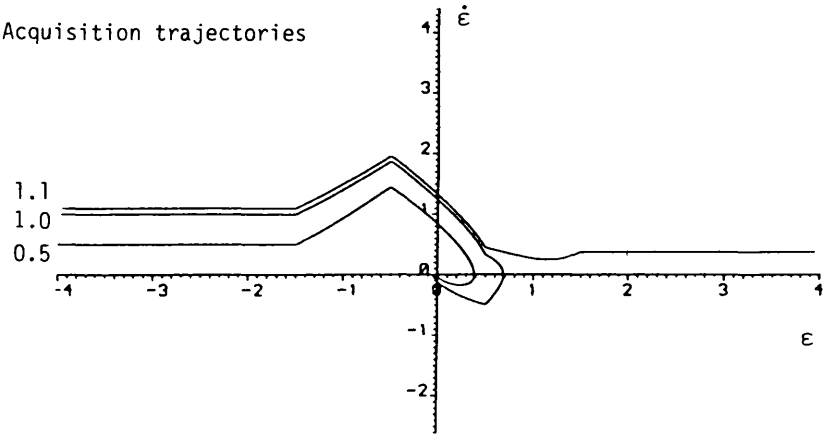
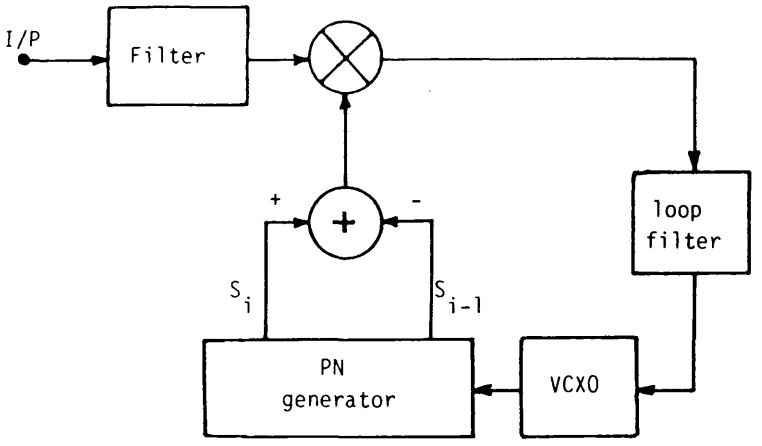


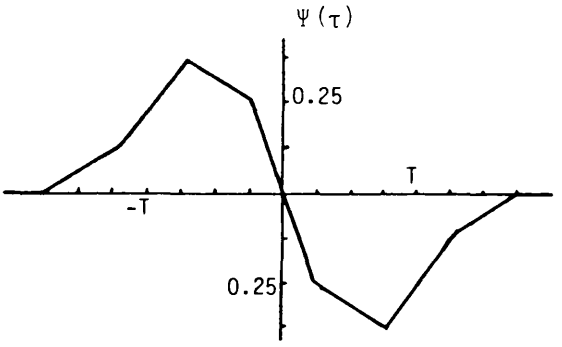
Figure 4.25. Alternative 1-Δ modified delay lock loop.

The final delay lock loop, to be considered in this section is the original standard 1-Δ delay lock loop, but this time it is to be used to receive the new multi-level transmitted signal. In fact it is found that this loop forms a 1.5-Δ delay lock loop having an error curve tracking range of 1.5 Δ, as shown in Figure 4.26. Although this loop shows a reduction of the maximum slipping rate by 0.1 i.e. its maximum limit is 0.9 instead of 1.0 for the standard 1-Δ loop. But certainly this loop has a wider tracking range and a better noise rejection capability which would make it useful in applications where there is very high Doppler shift, or where the noise level is high which will cause the normal loops to lose lock prematurely because of the limited range of delay error where lock may be achieved.

Finally we come to a very important advantage concerning the receiver which used any of the delay lock loops discussed in this section, and that is the signal to noise ratio improvement. As it is described previously, the bandwidth of the receiver is usually taken to be equal to the main lobe of the $(\sin x/x)^2$ power spectral density which is equal to 2 times the clock frequency of the pseudonoise code sequence. But this is not necessarily to be the best condition as Dixon [6] has found. If the bandwidth of the receiver was reduced to 60 percent of the main lobe bandwidth, the noise power would be reduced by 40 percent, while the input signal power would be reduced only by 3 percent instead of the 10 percent for the original input power of a standard signal. A further reduction in the bandwidth of the receiver to 50 percent, causes a drop in the input signal power only by 7.5 percent which is still better than the 10 percent reduction of input signal power corresponding to reduction of 60



a) Block diagram



b) 1.5- N-shape error curve

c) Acquisition trajectories

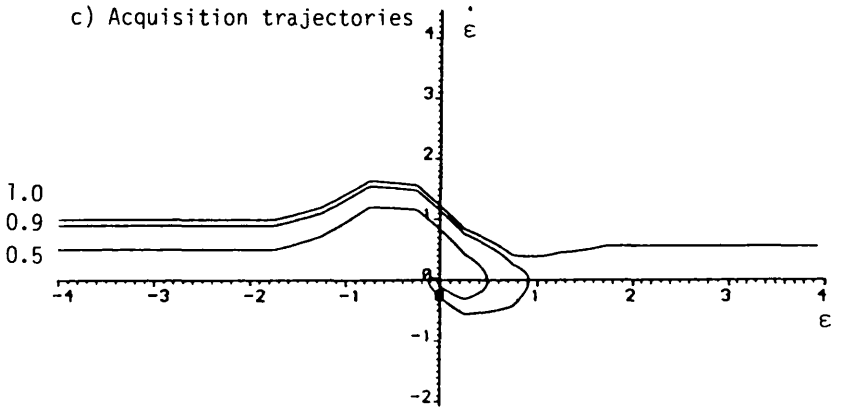


Figure 4.26. 1.5-Δ modified delay lock loop.

percent in bandwidth for the original standard system. This is shown in Figure 4.27.

Other multi-level sequence structures have been considered. For example, the possibility of **subtracting** the half bit delayed version of the sequence from itself rather than adding them together. The resulting signal $(S_i - S_{i-0.5})$ has also three levels +5, 0, -5 volts. Unlike previously discussed multilevel sequences it has no advantages from either the receiver or the transmitter point of view. The important results under investigation here are shown in Figure 4.28. The total power in the main bandwidth $(2 \times f_c)$ is less than that of the standard spread spectrum signal. It also appears to have considerable amount of power, about 20 percent, distributed in the side lobes, and as a consequence there will be no advantage in reducing the bandwidth of the receiver to improve the signal to noise ratio, as above. The only delay lock loop found to receive this type of signal is the 0.5-Δ delay lock loop which generates a single local code sequence S_i and correlates it with the received signal $(S_i - S_{i-0.5})$. Its N-shape error curve is shown in Figure 4.28(e).

4.3 OTHER POSSIBLE SYSTEMS

In this section some ideas of constructing an alternative 4-Δ, 2-Δ, and 1-Δ delay lock loops are given. Some advantages as well as disadvantages were obtained as a result of these structures.

i) Another structure of 4-Δ delay lock loop could be obtained by transmitting the signal $(S_i + S_{i+1})$. Its autocorrelation function and the power spectral density are shown in figure 4.29. The total power in the main bandwidth i.e. $2 \times f_c$ is about twice that of the standard one. But the power has zeros at multiples of $\pi/2\Delta$ instead

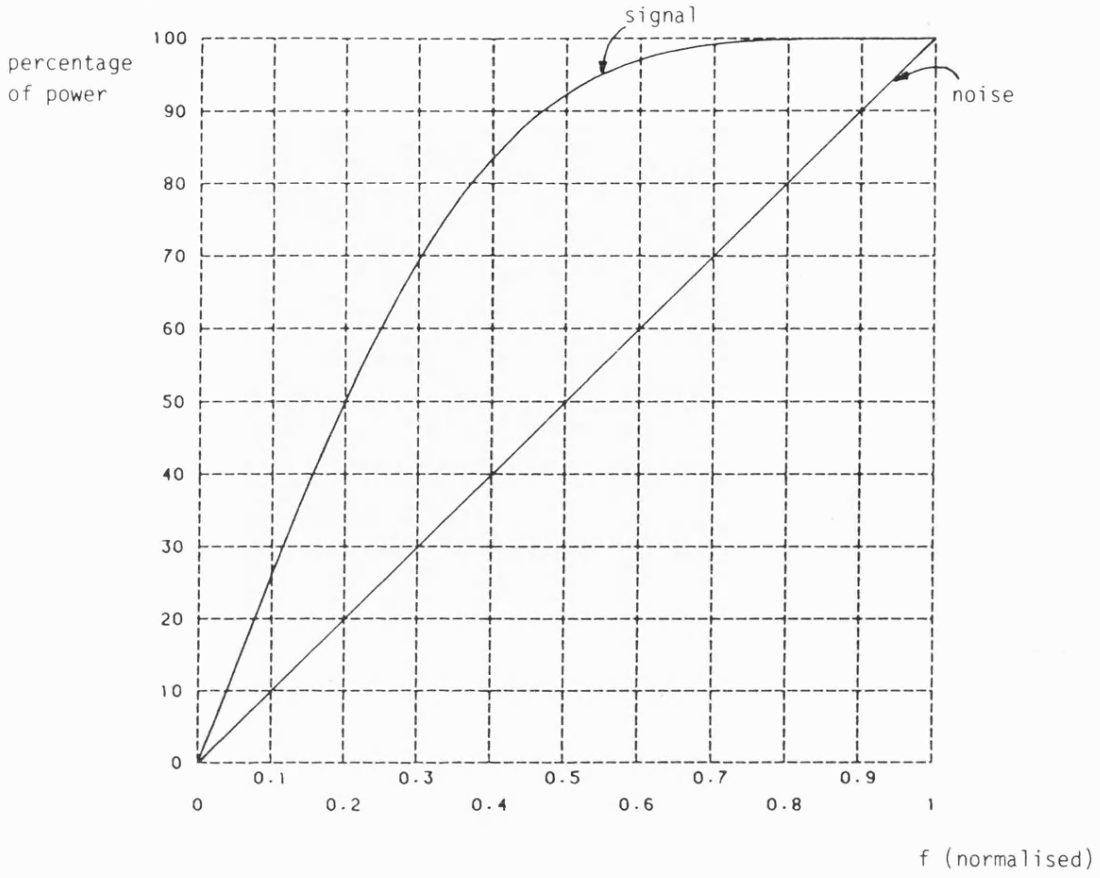
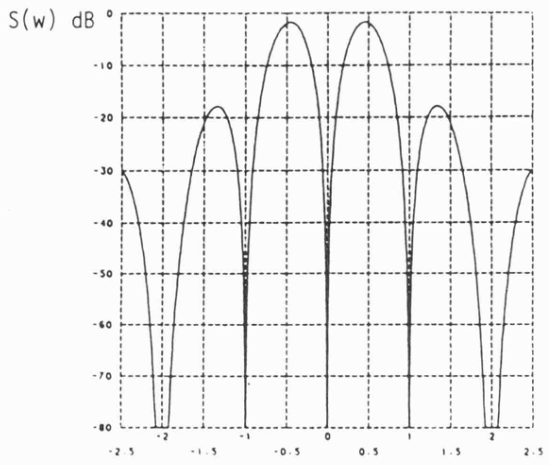
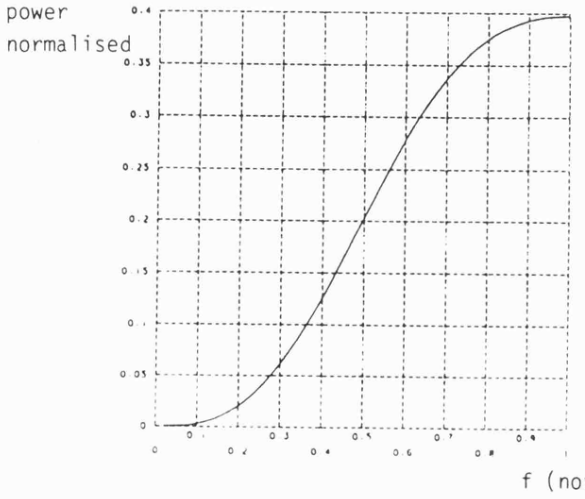


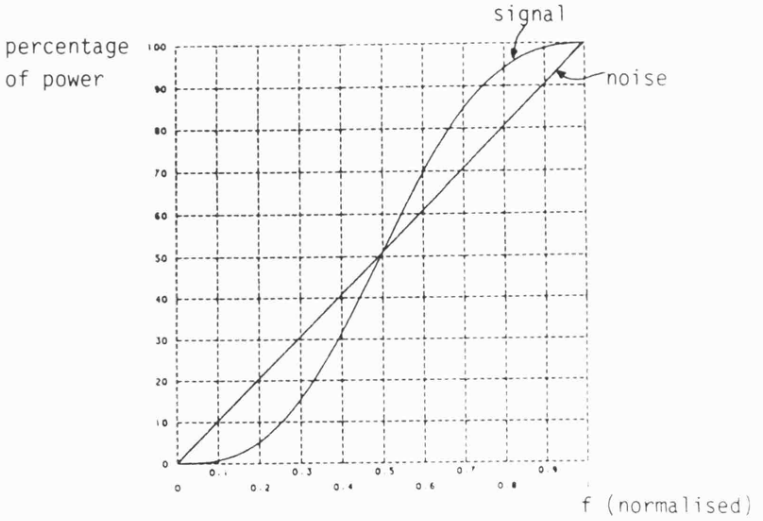
Figure 4.27. Percentage of power versus bandwidth in the main lobe bandwidth



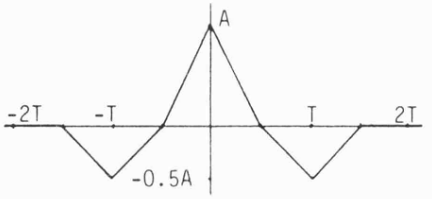
a) Power spectral density



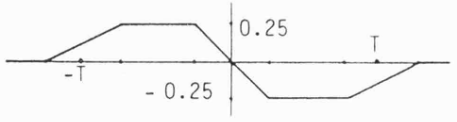
b) Distribution of power on the main bandwidth



c) Percentage of power versus frequency

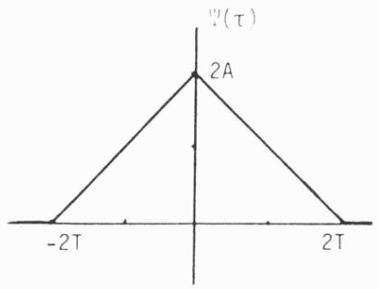


d) Auto-correlation function

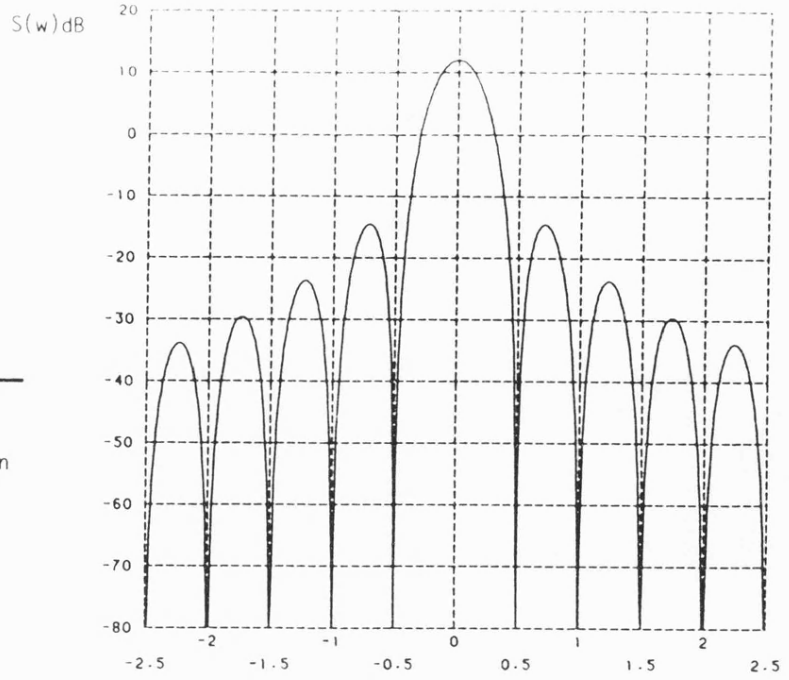


e) 0.5-Δ N-shape error curve

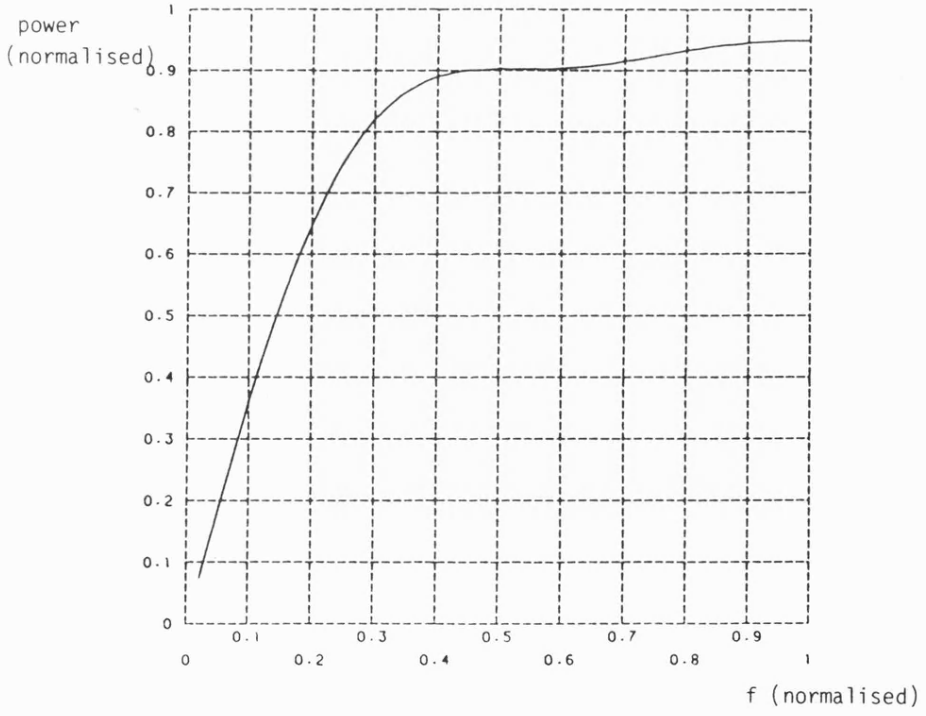
Figure 4.28. $(S_i - S_{i-0.5})$ related waveforms



a) Auto-correlation function



b) power spectral density



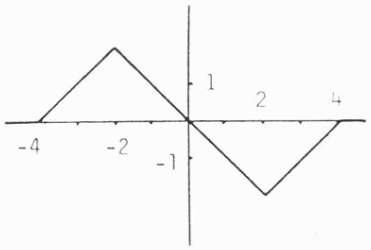
c) Distribution of power in the main bandwidth.

Figure 4.29 Transmitting $S_i + S_{i+1}$ for alternative 4-Δ system.

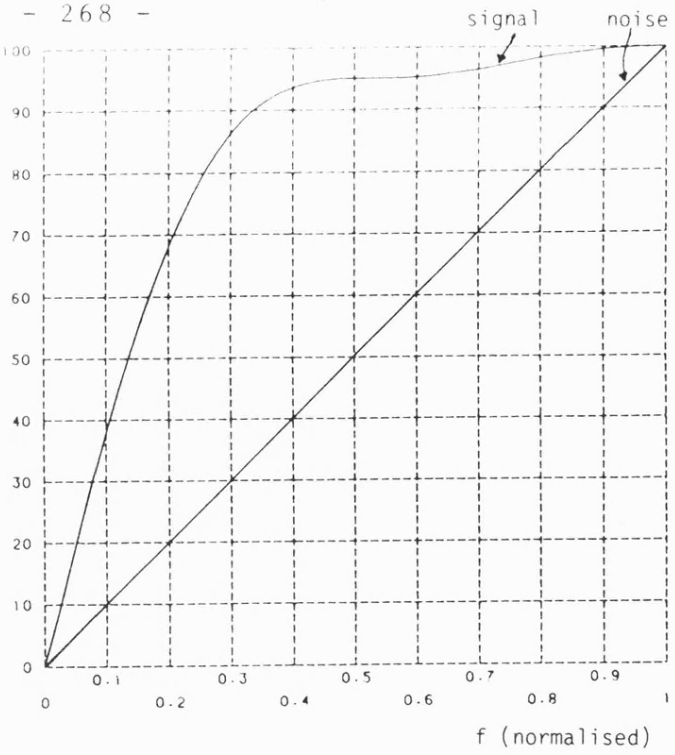
of π/Δ. In the receiver, the received signal (S_i+S_{i+1}) is correlated with $(S_{i-2}+S_{i-1} - S_{i+2} - S_{i+3})$ to develop the N-shape error curve needed as shown in Figure 4.29. Clearly the structure of this 4-Δ delay lock loop is slightly simpler than the standard 4-Δ loop since the two locally generated sequences S_{i-1} and S_{i+2} are not multiplied by the scale factor 1/2. Also the N-shape error curve is slightly different from the traditional one, where the slope is ± 1 at all positions. It is because of this difference the acquisition trajectories are also slightly different, as shown in Figure 4.30. A slight increase in the maximum slipping rate and Doppler-shift displacement were obtained. The last important point here is that by narrowing the receiver bandwidth to 60 percent of the main bandwidth, would reduce the noise to 40 percent of its original value, while only 5 percent of the desired signal power would be lost.

It is also possible to establish a 2-Δ delay lock loop by using the same transmitted signal i.e. $(S_i + S_{i+1})$ and correlate this signal in the receiver by the local code sequence (S_i-S_{i-1}). The error curve and the acquisition trajectories are the same as the standard 2-Δ delay lock loop, but the signal to noise ratio improvement can be gained as mentioned above.

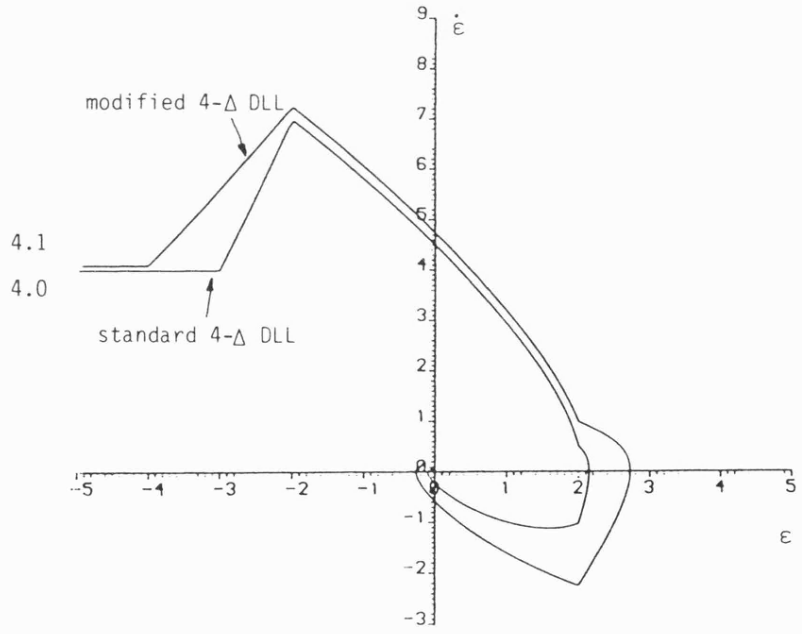
ii) Another 4-Δ delay lock loop could be constructed by transmitting the signal $(S_{i-1} + S_{i+1})$ whose related waveform and signal power are shown in Figure 4.31. In the receiver, this signal is correlated with $(S_i + 2\ S_{i+1} - 2\ S_{i+3} - S_{i+4})$. The N-shape error curve is identical to that in (i) above, and hence the acquisition trajectories. It was found that this system has no great advantage compared with other systems discussed earlier.



a) 4-Δ N-shape error curve

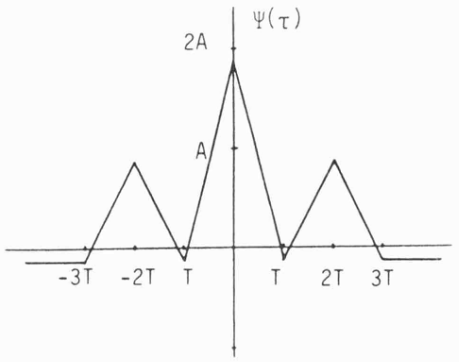


b) percentage of poewr in the main bandwidth

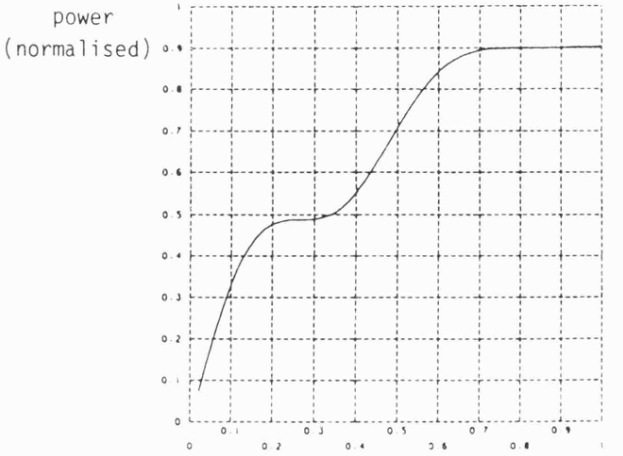


c) Acquisition trajectories

Figure 4.30. An alternative 4-Δ delay lock loop.

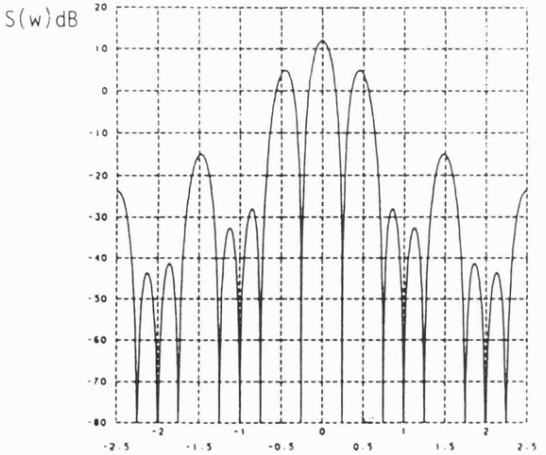


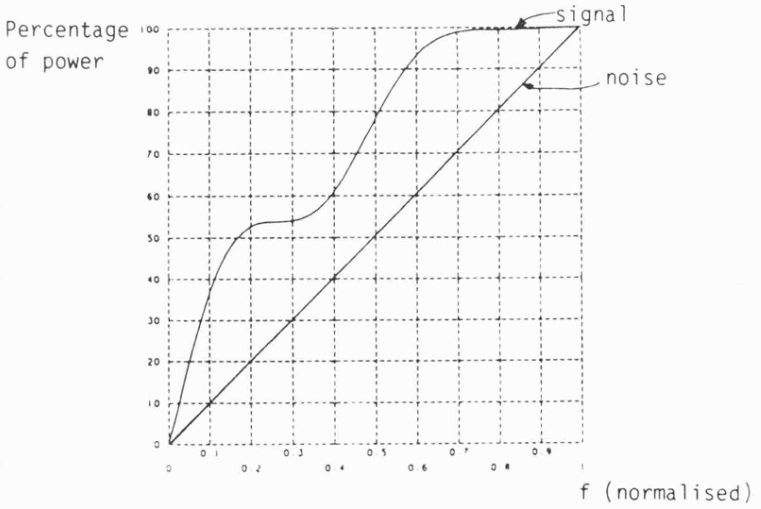
a) Auto-correlation function



c) Distribution of power in the main bandwidth

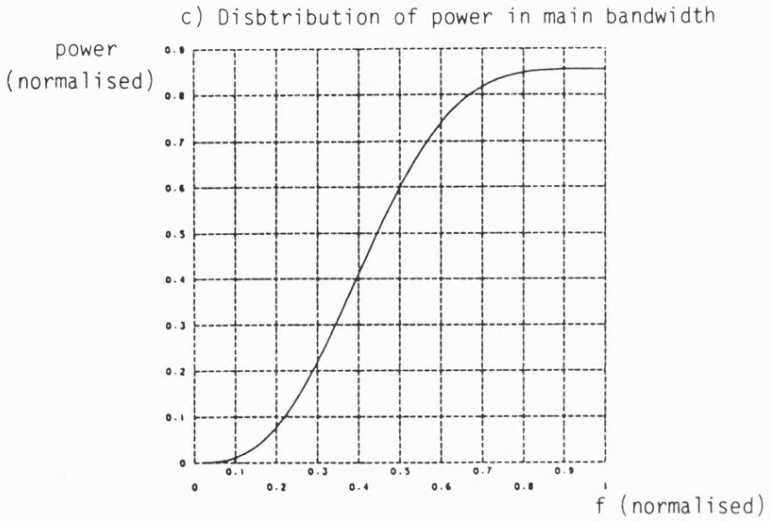
b) Power spectral density

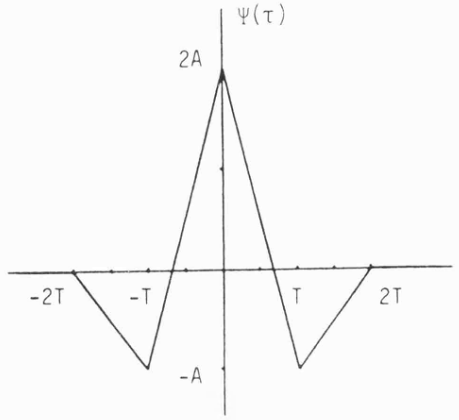


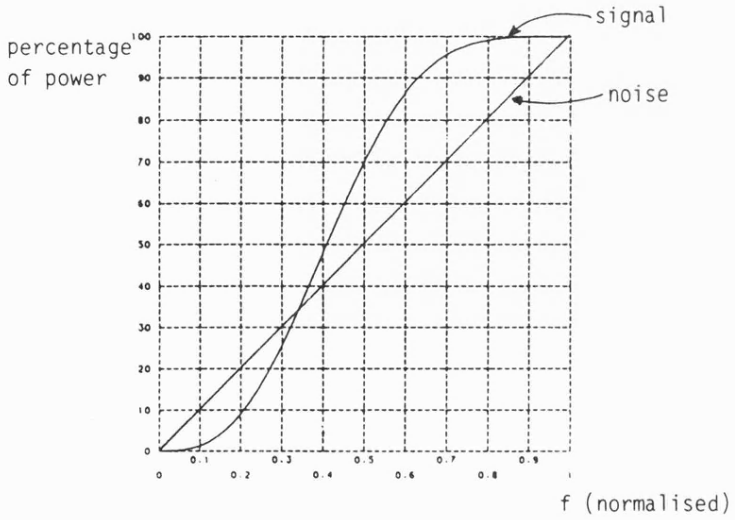


d) Percentage of power in the main bandwidth

Figure 4.31. $(S_{i-1}+S_{i+1})$ transmitted signal for 4-Δ delay lock loop.







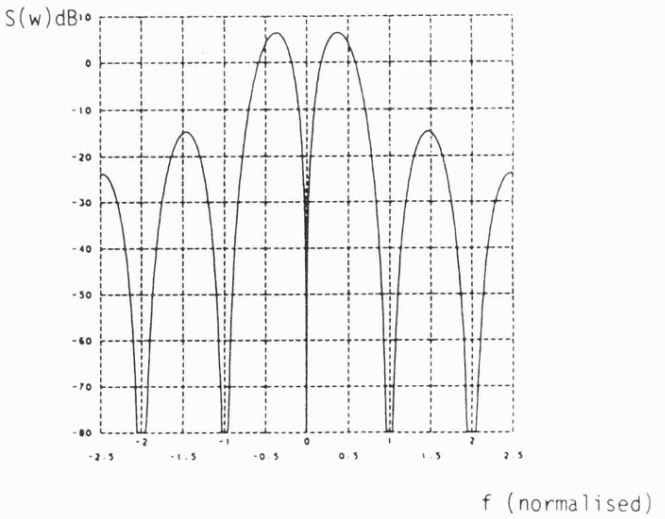


Figure 4.32 $(S_i - S_{i-1})$ transmitted signal for 1-Δ and 2-Δ DLL.

TRANSMITTED SEQUENCE			DELAY LOCK LOOP	
Structure	Levels	Type	Local generated sequence	M.Search rate
$S_{i-1} - S_{i+1}$	3	2-Δ	S_i	2.0
$S_{i-2} - \frac{1}{2}S_{i-1} - \frac{1}{2}S_{i+1} - S_{i+2}$	7	4-Δ	S_i	4.0
$S_{i+1} + \frac{1}{2}S_i - S_{i-2}$	6	4-Δ	$S_{i-1} - S_{i+1}$	4.0
$S_i + S_{i+0.5}$	3	3-Δ	$S_i + S_{i+0.5} - S_{i-3} - S_{i-3.5}$	5.5
$S_i + S_{i+0.5}$	3	2.5-Δ	$S_i + S_{i+0.5} - S_{i-2.5} - S_{i-3}$	3.0
$S_i + S_{i+0.5}$	3	2-Δ	$S_i + S_{i+0.5} - S_{i-2} - S_{i-2.5}$	1.7
$S_i + S_{i+0.5}$	3	2-Δ	$S_{i-1} + S_{i+1}$	3.3
$S_i + S_{i+0.5}$	3	1-Δ	$S_i - S_{i-0.5}$	1.0
$S_i + S_{i+0.5}$	3	1.5Δ	$S_i - S_{i-1}$	0.9
$S_i - S_{i-0.5}$	3	1-Δ	S_i	1.0
$S_i + S_{i+1}$	3	4-Δ	$S_i + S_{i+1} - S_{i+4} - S_{1+5}$	4.1
$S_{i-1} + S_{i+1}$	3	4-Δ	$S_i + 2S_{i+1} - 2S_{i+3} - S_{i+4}$	4.1
$S_i - S_{i-1}$	3	1-Δ	S_i	1.0
$S_i - S_{i-1}$	3	2-Δ	$S_i + S_{i+1}$	2.0

Table 4.1. Summarised Results

iii) The final transmitted signal under consideration in this chapter is one which consists of $(S_i - S_{i-1})$. Its power spectral density, and other related waveforms are shown in Figure 4.32. Two possible delay lock loops could be constructed to receive this signal. The first one is a 1-Δ delay lock loop which correlates the received signal $(S_i - S_{i-1})$ with a single local code sequence S_i. The error curve and the acquisition trajectories are the same as for the standard 1-Δ loop. The second configuration is a 2-Δ delay lock loop. This correlates the received signal with $(S_i + S_{i+1})$. This loop is also identical to the standard 2-Δ delay lock loop. Obviously no advantages are gained from the 2-Δ loop, but clearly the structure of the 1-Δ delay lock loop is simpler than the standard one since single local code sequence is involved in the correlation process, and this could be used when a simple receiver is required.

Table 4.1 summarises the results of various delay lock loops discussed earlier in this chapter.

4.4 CONCLUSIONS

This chapter has presented several novel spread spectrum configurations, in which a delay lock loop is used to achieve synchronisation and maintain tracking between the received signal and the locally generated sequence. These modifications have not previously been considered by other workers. The modifications given in this chapter affect both the transmitter and also the receiver.

First, a method was given to simplify the structure of the standard 2-Δ and 4-Δ delay lock loop, which consequently reduces the complexity and cost of the receiver. This method was achieved by

transferring part of the delay lock loop's correlator from the receiver to the transmitter. This involved transmitting a multi-level sequence. This type of technique could be applied particularly where there are many receivers connected to a single transmitter in a certain communications network. Experimental results were obtained, which showed no degradation, in the search rate as well as white noise rejection performance, as a result of these modifications.

Secondly, by transmitting three level sequences generated in the transmitter by adding 1/2 bit shift version of the transmitted sequence to itself, other structures of various delay lock loops are presented which not only show higher search rates than the standard loop but also show relative improvement in the signal to noise performances when the bandwidth of the receiver is reduced to 60% of the original mainlobe bandwidth because of their improved utilisation of the main lobe. Some of these structures are also relatively simple, and a few have no significant advantages.

The only disadvantage that can be seen as a result of transmitting the multi-level sequence in the transmitter is the necessity of having linear amplifiers in both the transmitter and the receiver ends rather than non-linear transmitter amplifiers used to amplify the two level standard sequence.

CHAPTER FOUR - REFERENCES

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CHAPTER FIVE

THE APPLICATION OF COMPOSITE SEQUENCES TO MULTIPLE ACCESS SPREAD-SPECTRUM SYSTEMS

5.1 INTRODUCTION

The direct-sequence spread-spectrum receiver can be considered as a simple averaging signal processor. If the maximal length pseudo-noise sequence has a length L bits and the period of each data bit is the same as the sequence-repeat period, the value of each data bit is effectively repeated L times. Thus, in the presence of white noise interference the improvement of the SNR at the output is approximately:

$$\frac{SNR_o}{SNR_{in}} = 10 \log_{10} L$$

relative to the input SNR. Where maximum interference rejection is required, at the expense of the data bit rate, very long maximal length pseudo-noise codes are used. Long codes may also be used to ensure improved security because detection of long codes is more difficult than short codes. These two main aims can be fulfilled by trying to make the spreading codes as close as possible to a purely random binary sequence, however it is necessary for these codes to be generated easily and synchronised, and as the length of the sequence increases the epoch search process takes proportionately longer. The acquisition of pseudo-noise codes has been considered in the previous two chapters.

Other techniques for acquiring phase synchronisation of codes include surface acoustic wave (SAW) correlators and convolvers [1-4], and active (sliding) correlators with a variety of "search-lock"

strategies such as rapid acquisition by sequential estimation (RASE) or rapid acquisition by recursion aided sequential estimation (RARASE) [5,6], and delay lock loop (DLL) [7,10]. The advantage of the RASE and RARASE techniques is their rapid acquisition of coarse phase synchronisation in moderate signal to noise ratios. Although the DLL can work with very poor signal to noise ratios, its acquisition time is relatively long, and in general, however, the longer the maximal length sequence the longer the acquisition.

In order to improve the acquisition time of long sequences, many different forms of combination or composite sequence have been proposed [11,14]. In generating these sequences the aim is to break the sequence into a series of shorter sequences which may each be correlated against a replica of that short sequence, thus allowing a relatively rapid estimation of code phase, comparable to the acquisition time of the short code. However, it is necessary not to compromise the correlation performance of the combination sequences, if they are to be useful in ranging or multi-access spread-spectrum systems. Although there will be large partial correlations when correlating the combination sequence with one of the sub-sequences used in most system applications, it is the correlation properties between the entire sequence and its replica, or against other sequences generated in the set which are important.

Some combination sequences used in spread spectrum systems have been discussed in Chapter One. The construction of these sequences is slightly different from one family to another. Generally they are constructed from short sequences, but clocked from the same source of frequency, and combined by modulo-2 summation. The individual sequences may either have the same lengths or different lengths.

In general, however, these codes do not have as good cross correlation properties as the corresponding maximal length sequences [15].

A popular class of combination sequence has been proposed by Gold [11]. This does not provide significantly improved acquisition times but is useful in generating L+1 different sequences, each of length L bits, and having predictable auto-correlation and cross-correlation properties. Clearly, a large number of codes are required in a large capacity code division multiple access spread-spectrum system, where each code acts as a user address or key to the system. In such a system not all users are expected to operate simultaneously, nevertheless user capacity is limited by the number of sequences available. For the case of maximal sequences, unless L>1023 bit the number of different sequences is fairly limited (<60). An advantage of the class of Gold sequences is that the cross-correlation performance of the sequences is no worse than the cross-correlation performance of the two maximal length sequences used to generate the Gold sequences [11]. In general the correlation properties of Gold sequences are determinable. However, the index of discrimination in the auto-correlation function is not as high as for maximal length sequences.

An alternative class of combination sequences has been suggested primarily to provide both a large number of sequences and fast acquisition by Beale and Tozer [13]. These sequences have been proposed as being ideal for multi-access spread spectrum systems. Sorwate and Stark [14] have also proposed a similar class of composite sequences called Kronecker sequences. They have shown that

if the signal to noise ratio is relatively good the time required to synchronise Kronecker in passive matched filter correlators is significantly less than the time required to synchronise maximal length sequences of comparable length.

Composite or Kronecker sequences appear to have an important contribution in ranging and multi-access systems. In this chapter composite sequences are considered further, from two main viewpoints. The first considers the correlation properties of the sequences and from this the power spectral density of the transmitted signal, and the ability of the sequences to reject the interference of other users. The second viewpoint considers the acquisition properties of this class of sequences using a sliding correlator. A delay lock loop with a RASE search-lock strategy are used. And the acquisition times using these techniques are compared with those for a conventional maximal length sequence of similar length, L.

5.2 GENERATION OF THE COMPOSITE SEQUENCE

In order to construct the composite sequence, we first define the two component sequences as follows: Let U be a sequence of binary digit of amplitude +1 and -1 of period n_u. This sequence could be represented in the ith digit domain as:

$$u(i) = U(i+kn_u) \qquad 5.1$$

where k is an integer, i is 0, 1, 2, 3 .... n_u-1, and u(i) is a repetitive binary sequence.

In the same way we define the other binary sequence, V, having amplitudes +1 and -1 of period n_v such that:

$$V(j) = V(j+k\ n_v) \qquad 5.2$$

where j is 0, 1, 2, 3 .... n_v-1 and V(j) is a second repetitive binary sequence.

From these two component sequences, U and V, the resulting binary sequence, Z, also has amplitudes, +1 and -1, and is constructed by a multiplication process equivalent to sequence inversion keying modulation, SIK. The sequence, U, is the 'high speed' inner code modulated by the slower outer code, V. Figure 5.1 shows the construction of this composite sequence and it is summarised as follows:

By multiplying the first digit of the outer sequence V(0) by each digit of the inner sequence U(0), U(1), U(2) ... U(n_u-1), the first n_u digits of the composite sequence Z(0 ... n_u-1) are constructed. The second n_u digits of the composite sequence Z(n_u ... $2n_u$-1) are constructed by multiplying the second digit of the outer component sequence V(1) by each digit of the inner component sequence U(0), U(1), U(2) ... U(n_u-1), and so on until the last digit of the outer component sequence V(n_v-1) is to be multiplied by each digit of the inner component sequence U(0), ... U(n_u-1) to form the last n_u digits of the composite sequence Z[$n_v n_u$-n_u) ...($n_v n_u$-1)]. Then the whole process is to be repeated and so on.

From the illustration above, it is clear that:

(i) The chip-rate of the composite sequence Z is the same as the chip rate of the inner composite sequence U.

(ii) The chip-rate of the outer component sequence V should be made n_u times lower than the chip-rate of the inner component

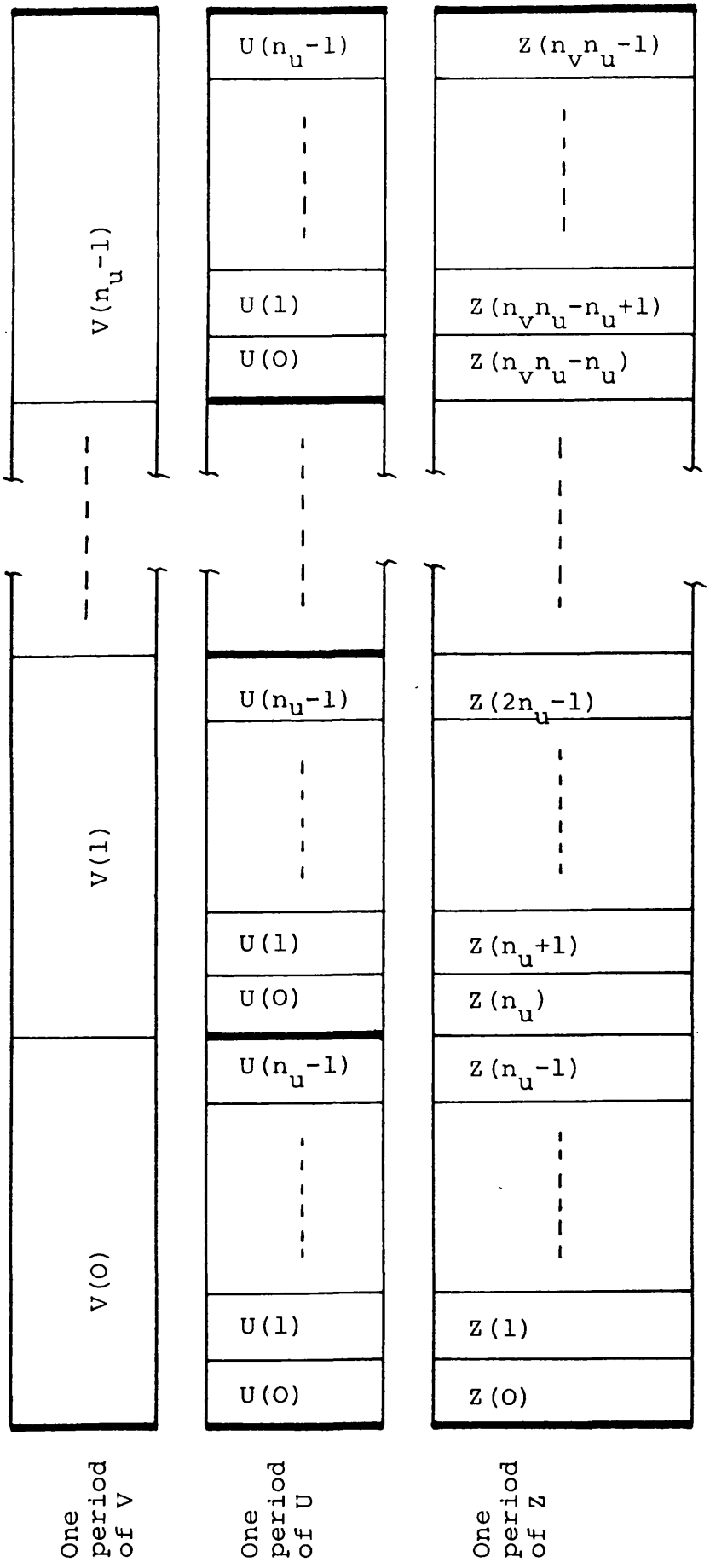


Figure 5.1. Construction of the composite sequence of Z from two composite sequences V and U, [13].

sequence U, i.e., the duration of every digit of V is equal to the whole period of U.

(iii) Each period of n_z of the composite sequence Z has the same duration as the outer component sequence period and it consists of $n_z = n_u n_v$ digits.

It is more convenient to explain the construction of the composite sequence by a small example as follows: let the digit +1 be represented by + and the digit -1 be represented by -. Let the component sequence U be a maximal length sequence of length 7 generated from 3 stages feedback shift register (2^3-1):

U= + + + - - + -

similarly let the other component sequence V be a maximal length sequence of length 3:

V = + + -

Although the lengths of the two sequences chosen in this example are different, but in practice they could be the same. So if we choose the later sequence V to be the outer component sequence and the first one U as the inner component sequence,

V = + + -

U = + + + - - + - + + + - - + - + + + - - + -

Z = + + + - - + - + + + - - + - - - - + + - +

one period of V is needed with n_v period of U to form one period of the resulting sequence Z. The period of the resulting sequence is $n_r = n_u \times n_v = 7 \times 3 = 21$. Longer composite sequences can be generated by

multiplying or by sequence inversion keying modulating the resulting sequence Z by a third outer component sequence, W, with period n_w. The chip-rate of this new outer sequence must be n_r (or $n_u n_v$) times slower than that of the sequence Z, and so on. So by this way long composite sequences can be generated from much shorter component sequences. In this chapter we concentrate on a composite sequence generated from two component sequences only.

The two component sequences need not be a maximal sequence. One example is the use of a maximal sequence for the inner component and a Barker code for the outer component [14]. Maximal sequences are used in this chapter because it is a very common sequence in multiple access spread spectrum systems, easy to generate and it has good correlation properties.

The composite sequence Z could be expressed mathematically from the two component sequences U and V, from which it can be constructed as follows:

$$Z(i) = U(i)\ V(0) \qquad \text{for } 0 \leqslant i \leqslant n_u-1$$

$$Z(i) = U(i-n_u)\ V(1) \quad \text{for } n_u \leqslant i \leqslant 2n_u-1$$

$$\vdots$$

etc

The general expression could be either of the form:

$$Z(i) = U(i-kn_u)\ M(k) \text{ for } kn_u \leqslant i \leqslant (k+1)n_u-1$$

$$\text{and } k \text{ is } 0, 1, 2 \ldots (n_v-1) \qquad 5.3$$

or of the form

$$Z(i) = U(j)\ V(k) \text{ for } 0 \leqslant j \leqslant n_u-1,\ 0 \leqslant k \leqslant n_v-1$$

$$\text{with } i = kn_u + j \qquad 5.4$$

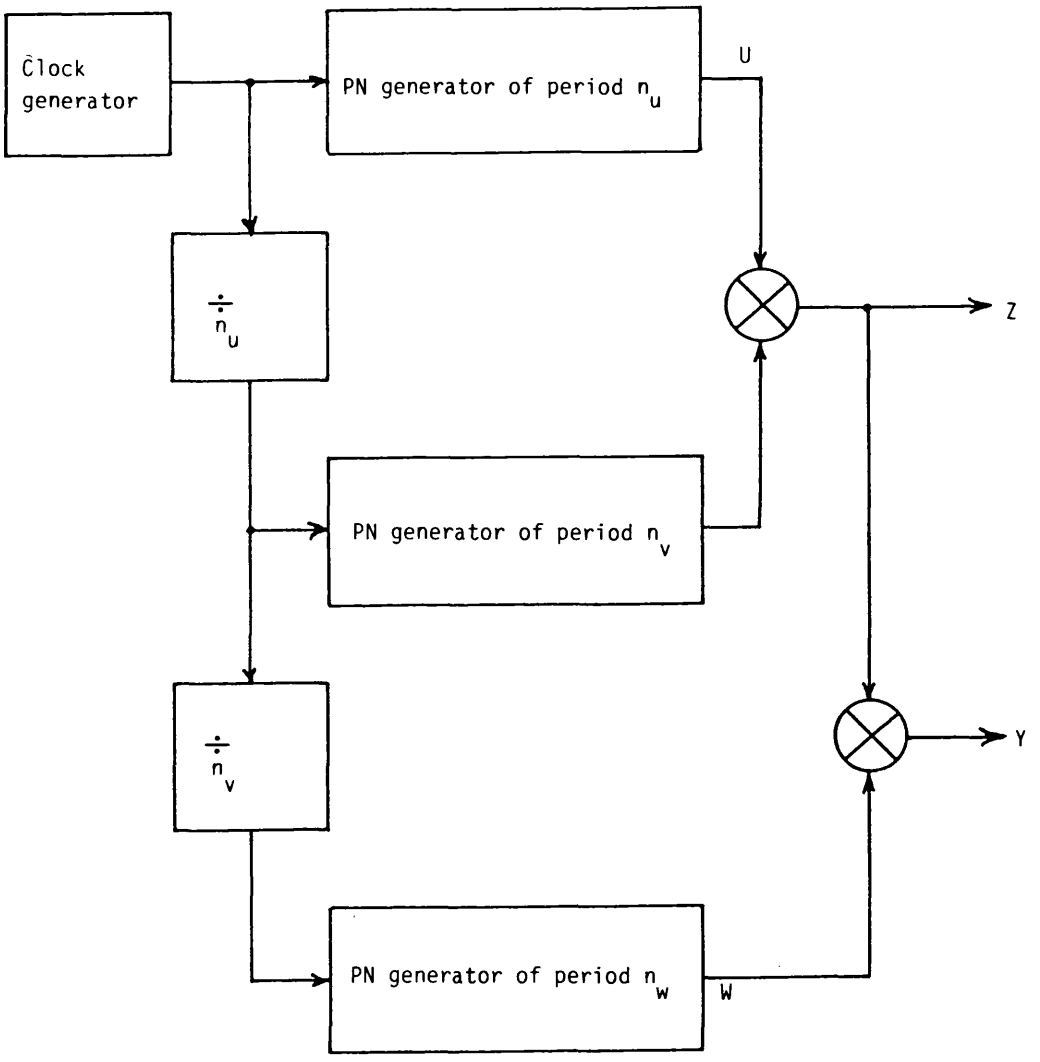


Figure 5.2 Block diagram of generating composite sequence.

(i) Z, from two component sequences U, V.

(ii) Y, from three component sequences U, V, W.

Figure 5.2 shows a block diagram of how to generate two composite sequences Y and Z.

i) generates a composite sequence Z from two component sequences; U as an inner sequence, and V as an outer sequence where the clock of the later is n_u times slower than the first one.

ii) generates a longer composite sequence Y from three short component sequences. The outer component sequence in this case is sequence W which has chip rate n_v times slower than the outer sequence V. The pseudo-noise generator could be an n-stages feedback shift register with a selected feedback taps to produce a maximal sequence of period 2^n-1. The multiplier could be replaced by a modulo-2 adder if a unipolar sequence is used.

This is the form of sequence generator proposed by Sarwate and Stark [14] to produce the Kronecker sequence.

5.3 CORRELATION PROPERTIES OF THE COMPOSITE SEQUENCE

One of the most important properties of any spread spectrum signal is the correlation function property of the sequences used. Both the cross-correlation and the auto-correlation function are equally important because in code division multiple access systems, the receiver must not respond to any signal other than the proper addressing sequence and the codes require a two valued auto-correlation function and a very low value of cross-correlation function.

Similarly, systems designed to suppress jamming signals require a good autocorrelation function with a high index of discrimination.

The cross-correlation properties of composite sequences will be presented first.

5.3.1 Cross-Correlation Function of the Composite Sequence

The unnormalised cross-correlation function between any two sequences Z_1 and Z_2 could be expressed as:

$$\Psi_{Z_i,Z_j}(\tau) = \sum_{k=0}^{L-1} Z_1(k)Z_2(k+\tau) \qquad 5.5$$

where L is the sequence length and τ is equal to 0, 1, 2, ... (L-1). Now consider the two sequences Z_1 and Z_2 are composite sequences constructed as shown in Figure 5.2. Suppose that their corresponding component sequences have equal periods; i.e. $n_{u_i} = n_{u_j} = n_u$, and $n_{v_i} = n_{v_j} = n_v$. Referring to Figure 5.2 Beale and Tozer have shown that the cross-correlation function of these two composite sequences is:

$$\Psi_{Z_1,Z_2}(\tau) = \sum_{k=0}^{n_v-1} \sum_{i=kn_u}^{(k+1)n_u-1} Z_i(i)Z_2(i+\tau)$$

$$= \sum_{k=0}^{n_v-1} \sum_{i=kn_u}^{(k+1)n_u-1} U_1(i-kn_u)V_1(k)U_2(i-kn_u)V_2(k+\tau_v)$$

where $\tau=\tau_v n_u$, i.e. τ is some integer multiple τ_m of the period n_u of the component sequence U_1 and U_2.

$$= \sum_{k=0}^{n_v-1} V_1(k)V_2(k+\tau_m) \sum_{j=0}^{n_u-1} U_1(j)U_2(j) \qquad 5.6$$

The first sum in the equation 5.6 above represents the periodic cross-correlation function for the two component sequences V_1 and V_2,

while the second sum represents the periodic cross-correlation function between the two component sequences U_1 and U_2, for a relative phase-shift of zero, so, the cross-correlation function now becomes:

$$\Psi_{Z_1,Z_2}(\tau) = \Psi_{U_1U_2}(0)\ \Psi_{V_1V_2}(\tau_v) \qquad 5.7$$

where $\tau = \tau_v\ n_c$

This result shows that the cross-correlation function of two composite sequences is depended on the cross-correlation function of the component sequences from which they are generated.

However, for relative phase shifts such that, $\tau \neq \tau_v n_u$ the cross-correlation function can also be found. Beale and Tozer [13] have considered this for values of τ in this range:

$\tau_v n_u + 1 \leq \tau \leq (\tau_v+1)\ n_u - 1$

where $\tau_v = 0, 1, 2 \ldots (n_v-1)$

Referring to figure 5.3, the two composite sequences $Z_1(i)$ and $Z_2(i+\tau)$ over the shaded area A, and for $\tau_v=1$ are:

$$\left.\begin{aligned} Z_1(i) &= U_1(i-kn_u)V_1(k) \\ Z_2(i+\tau) &= U_2[i+\tau-(k+1)n_u]V_2(k+1) \end{aligned}\right\} \quad kn_u \leq i \leq (k+2)n_u-1-\tau \qquad 5.8$$

For the unshaded area B

$$\left.\begin{aligned} Z_1(i) &= U_1(i-kn_u)V_1(k) \\ Z_2(i+\tau) &= U_2[i+\tau-(k+2)n_u]v_2(k+2) \end{aligned}\right\} \quad (k+2)n_u-\tau \leq i \leq (k+1)n_u-1 \qquad 5.9$$

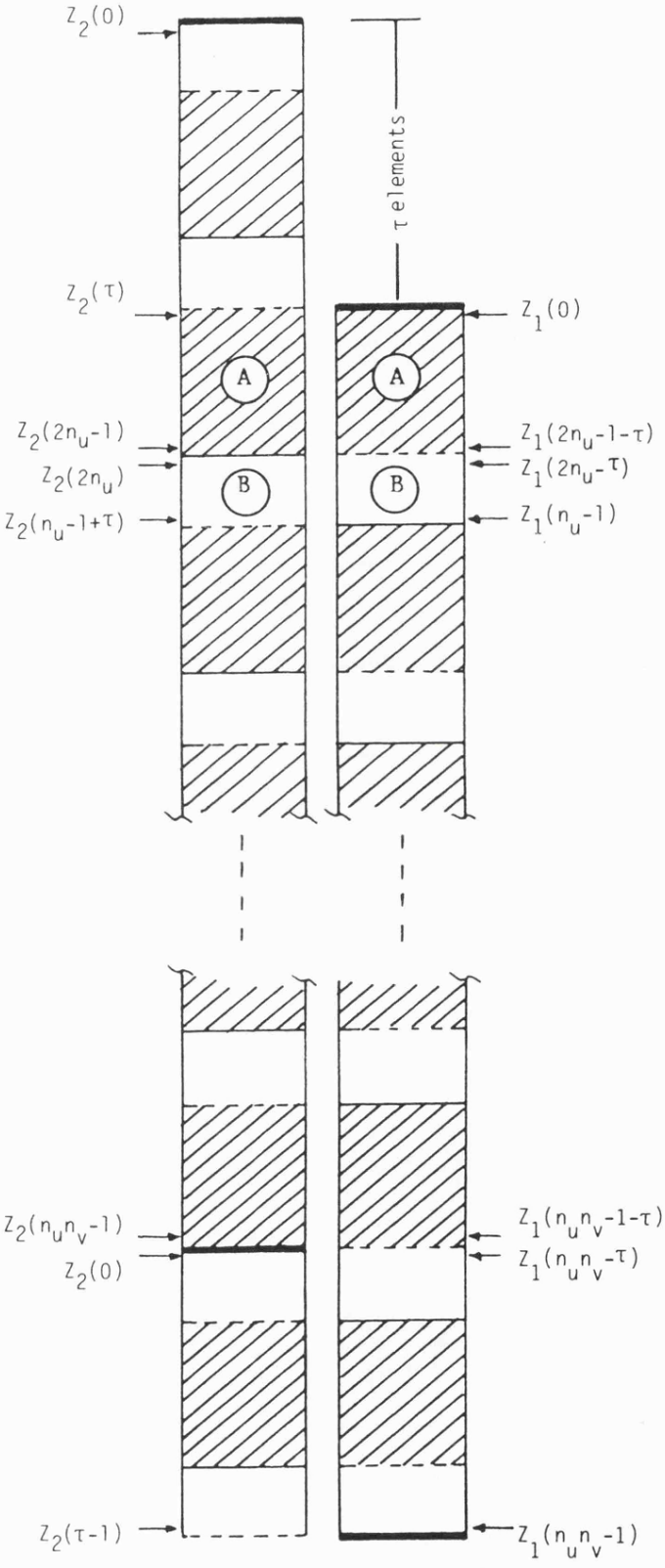


Figure 5.3. Periodic cross-correlation function for (n_u+1) τ $(2n_u-1)$ [13]

Similarly for the other values of τ_v

$$Z_1(i)=U_1(i-kn_u)V_1(k) \text{ for } kn_u \leq i \leq (k+1)n_u-1$$

$$Z_2(i+\tau) = \begin{cases} U_2[i+\tau-(k+\tau_v)n_u]V_2(k+\tau_v) \text{ for } kn_u \leq i \leq (k+\tau_v+1)n_u-1-\tau \\ U_2[i+\tau-(k+\tau_v+1)n_u]V_2(k+\tau_v+1), \text{ for } (k+\tau_v+1)n_u-\tau \leq i \leq (k+1)n_u-1 \end{cases}$$

5.10

The equation of $Z_1(i)$ is applied to both shaded and unshaded area as it is the same in equations 5.8 and 5.9 for both shaded and unshaded case where $\tau_v=1$. But there are two equations for $Z_2(i+\tau)$, the upper one in 5.10 applied to the shaded area while the lower one applied to the unshaded area, for the limit

$$\tau_v n_u+1 \leq \tau \leq (\tau_v+1)n_u-1 \ , \ (\tau_v=0, 1, 2, \ldots n_v-1)$$

So the cross-correlation function of the two composite sequences $Z_1(i)$ and $Z_2(i+\tau)$ can be now written as:

$$\psi_{Z_1,Z_2}(\tau) = \sum_{k=0}^{n_v-1} \left\{ \sum_{i=kn_u}^{(k+\tau_v+1)n_u-1-\tau} U_1(i-kn_u)V_1(k)U_2[i+\tau-(k+\tau_v)n_u] \right.$$

$$\left. V_2(k+\tau_v)+\sum_{i=(k+\tau_v+1)n_u-\tau}^{(k+1)n_u-1} U_1(i-kn_u)V_1(k)U_2[i+\tau-(k+\tau_v)n_u]V_2(k+\tau_v+1) \right\}$$

5.11

This equation could now be simplified to

$$\psi_{Z_1,Z_2}(\tau) = \phi_{u_1,u_2}(\tau_u)\psi_{V_1,V_2}(\tau_v) + \phi_{u_1,u_2}(\tau_u - n_u)\psi_{V_1,V_2}(\tau_v+1) \qquad 5.12$$

where $0 \leq \tau_v \leq n_v-1$, $0 \leq \tau_u \leq n_u-1$, and $\tau = \tau_v\tau_u+\tau_u$ (from which the value of τ changes between $0 \leq \tau \leq n_u n_v-1$) and

$$\phi_{U_1,U_2}(\tau_u) = \sum_{j=1}^{(\tau_v+1)n_u-1-\tau} U_1(j)U_2(j+\tau-\tau_v n_u)$$

$$\phi_{U_1,U_2}(\tau_u-n_u) = \sum_{j=(\tau_v+1)n_u-\tau}^{n_u-1} U_1(j)U_2[j+\tau-(\tau_v+1)n_u]$$

so the periodic cross-correlation function for a pair of composite sequences is given in equation 5.12, for all relative phase-shift τ, in terms of the cross parameters of their component sequences.

The results obtained by Beale and Tozer [13] is identical to that obtained by Sarwate and Stark [14]. However, the later authors considered the correlation properties further. They obtained the aperiodic and odd cross-correlation function of two composite sequences. This is particularly important in asynchronous data modulated systems. Using similar arguments to the above, the odd cross correlation function obtained by [14] is:

$$\hat{\psi}_{Z_1,Z_2}(\tau) = \phi_{U_1,U_2}(\tau_u)\hat{\psi}_{V_1,V_2}(\tau_v) + \phi_{U_1,U_2}(\tau_u-n_u)\hat{\psi}(\tau_v+1) \qquad 5.13$$

the same limits are applied, that is

$$0 \leq \tau_u \leq n_v-1,\ 0 \leq \tau_u \leq n_u-1,\ \tau = \tau_v n_u + \tau_u$$

Equation 5.13 is the same as that of 5.12 except that the presence of $\hat{\Psi}_{v_1,v_2}$ instead of Ψ_{v_1,v_2}, and this represents the odd cross-correlation function of the outer component from which the odd cross-correlation function of a pair of composite sequences could be obtained.

The aperiodic cross-correlation function can be shown to be:

$$\phi_{Z,Z_2}(\tau) = \begin{cases} \frac{1}{2}[\psi_{Z_1,Z_2}(\tau)+\hat{\Psi}_{Z_1,Z_2}(\tau)] \text{ for } 0 \leq \tau \leq n_u n_v \\ \frac{1}{2}[\psi_{Z_1,Z_2}(\tau+ n_u n_v)-\hat{\psi}_{Z_1,Z_2}(\tau+n_u n_v)] \text{for } 1-n_u n_v \leq \tau \leq -1 \end{cases}$$

5.14

or it could be expressed by using equations 5.12 and 5.13.

$$\phi_{Z_1,Z_2}(\tau) = \phi_{U_1,U_2}(\tau_u)\ \phi_{V_1V_2}(\tau_v)+\phi_{U_1,U_2}(\tau_u-n_u)\phi_{V_1,V_1}(\tau_v+1) \qquad 5.15$$

this shows that the aperiodic cross-correlation function of two composite sequences depends on the aperiodic cross-correlation function of their component sequences.

An alternative, and rather simpler but longer way to determine the cross-correlation function of any two digital sequences including composite sequences is from the following relationship:

$$\Psi_{Z_1,Z_2}(\tau) = \text{number of bit agreements - number of bit disagreements}$$

5.16

The normalised cross-correlation function is

$$\psi'_{Z_1,Z_2}(\tau) = \frac{\psi_{Z_1,Z_2}(\tau)}{\text{total number of sequence bits}} \qquad 5.17$$

where $\tau = 0, 1, 2, \ldots n-1$

This is calculated over all integral bit shift, with the two sequences being compared bit by bit.

In the following, some examples of the cross-correlation performance of several sequences will be given. To find out the behaviour of some composite sequences and compare them with that of their component sequences from which they are constructed or with maximal length sequences, several maximal length sequences and composite sequences have been chosen and constructed as shown in tables 5.1 and 5.2 respectively. All the maximal length sequences are generated from an n-stages feedback shift register with selected feedback taps as shown in the table, while the composite sequences are constructed as explained in Section 5.2.

First the normalised cross-correlation function of some maximal length sequences, which are calculated and shown in Figure 5.4, are examined. From this figure, we can see that the normalised cross-correlation function varies from one pair of sequences to another. It is mainly dependent on the type of sequences under consideration, the bit by bit structure, and the length of the sequences. For the pair of sequence {D15, E15} (see table 5.1) and the pair {B7, C7}, the normalised cross-correlation function is relatively high. Their peak to peak value reaches about 1.1. A slightly lower peak to peak value of about 0.7 is found for the pair {F31, C7} and also for {F31, E15}. A similar result (not shown) was found for {F31, D15} and

Sequence Symbol	No. of stages	Feedback taps	Sequence length	Sequence +1 = + 0 or -1 = -
A3	2	2,1	3	+ + - .
B7	3	3,1	7	+ + + - + - - .
C7	3	3,2	7	+ + + - - + - .
D15	4	4,1	15	+ + + + - + - + + - - + - - - .
E15	4	4,3	15	+ + + + - - - + - - + + - + - .
F31	5	5,2	31	+ + + + + - - + + - + + - .... + - - - .
G63	6	6,1	63	+ + + + + + - + - + - + + ... - - - - - .

Table 5.1. Generation of some maximal length sequences.

(a)

	Inner Component	Outer Component	
C. Sequence Symbol	Inner Component	Outer Component	C. Sequence length
B7A3	B7	A3	21
C7A3	C7	A3	21
B7C7	B7	C7	49
C7B7	C7	B7	49
D15A3	D15	A3	45
E15A3	E15	A3	45
D15B7	D15	B7	105
D15C7	D15	C7	105
E15C7	E15	C7	105
E15B7	E15	B7	105
F31A3	F31	A3	93
F31C7	F31	C7	217
F31B7	F31	B7	217
F31D15	F31	D15	465
F31E15	F31	E15	465
G63C7	G63	C7	441
G63B7	G63	B7	441
2B15B7	2B15+1	B7	217

Table 5.2. Generation of some composite sequences

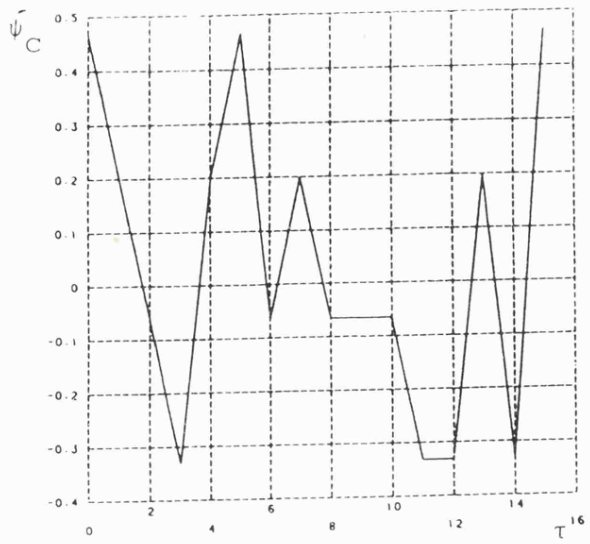
a) Inner component outer component

Table 5.2 Continued

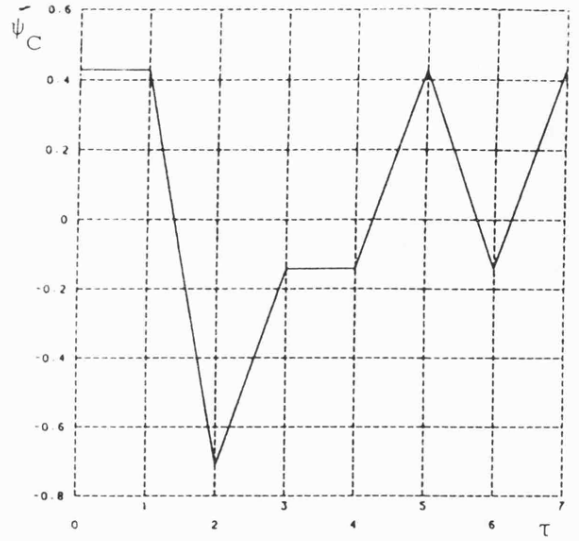
(b)

Inner Component	Outer Component		
C. Sequence Symbol	Inner Component	Outer Component	C. Sequence length
A3C7	A3	C7	21
A3B7	A3	B7	21
A3D15	A3	D15	45
A3E15	A3	E15	45
A3F31	A3	F31	93
C7D15	C7	D15	105
B7E15	B7	E15	105
C7E15	C7	E15	105
B7D15	B7	D15	105
C7F31	C7	F31	217
B7F31	B7	F31	217
E15D15	E15	D15	225
D15E15	D15	E15	225
D15F31	D15	F31	465
E15F31	E15	F31	465
C7G63	C7	G63	441
B7G63	B7	G63	441
B72B15	B7	2B15+1	217

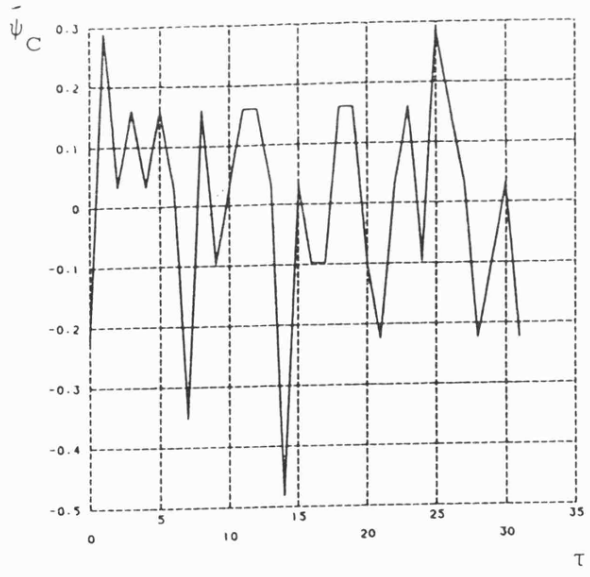
b) Inner component outer component



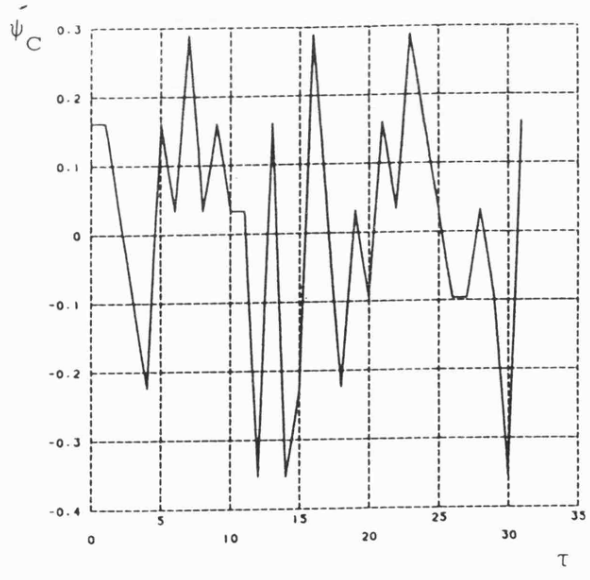
a) D15, E15



b) B7, C7

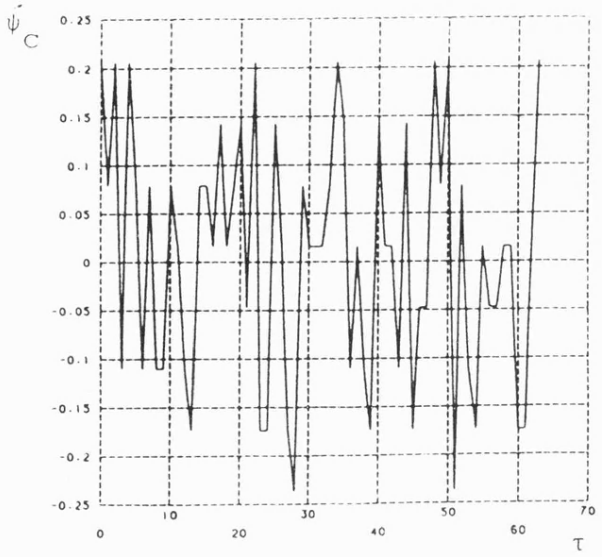


c) F31, C7

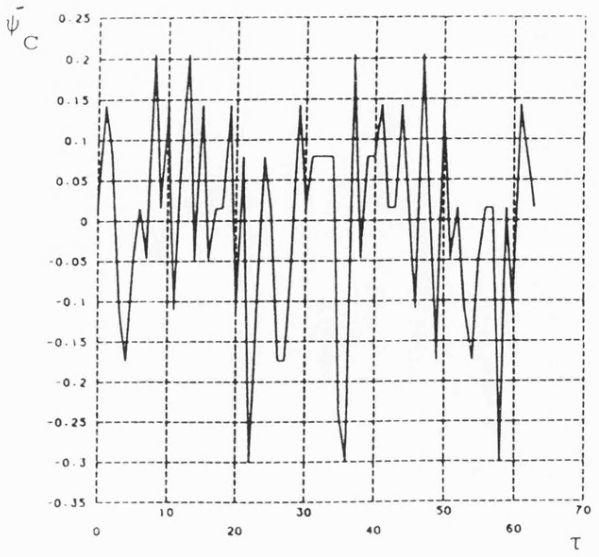


d) F31, E15

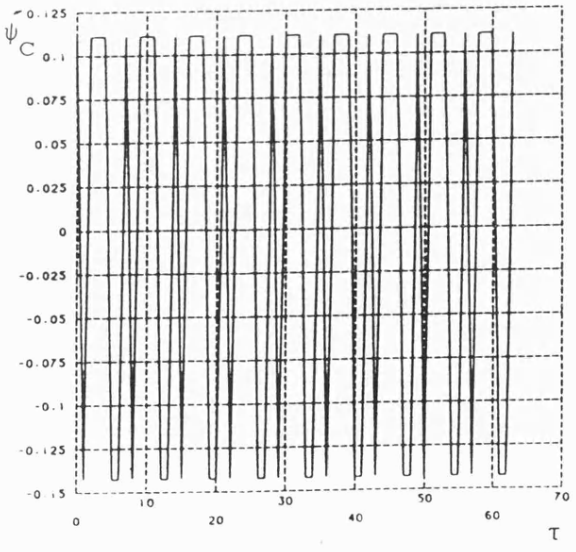
Figure 5.4. Some normalised cross-correlation functions of different maximal length sequences.



e) G63, E15



f) G63, F31



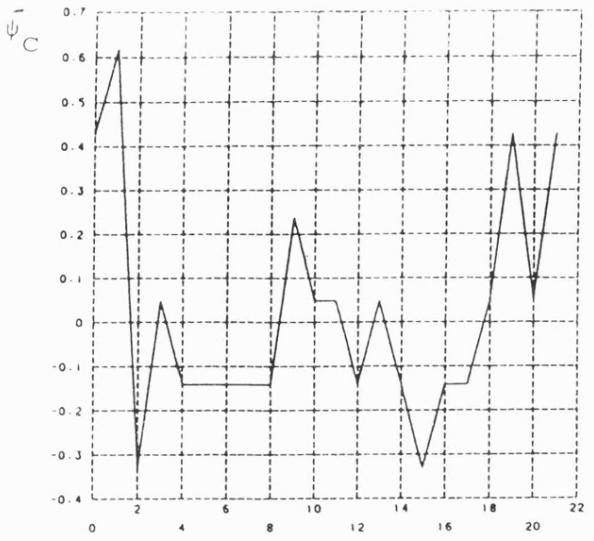
g) G63, C7

Figure 5.4. (Continued).

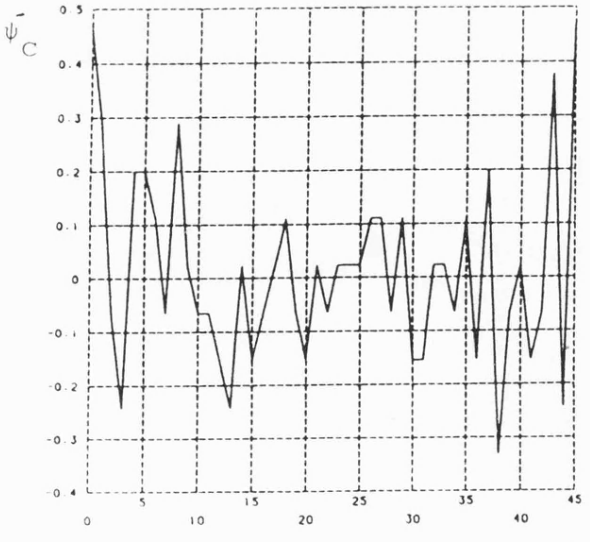
{F31, B7}. The next, smaller, peak to peak value which is equal to 0.45 is found for {G63, E15} and {G63, F31}. A similar result (not shown) was found for {G63, D15}. However for the pair {G63, C7} the peak to peak value is only 0.25 which is not only a very small value but also has uniform distribution.

Referring to table 5.2 (a), which shows some composite sequences and their components (note that the inner component is longer or equal to the outer component), the normalised cross-correlation function is calculated and plotted in Figure 5.5. Three main types of cross-correlation function are noticed here. The first one has relatively high value with respect to the others such as the two pairs {C7A3, B7A3} and {D15A3, E15A3}. Their peak to peak value reaches 0.9. The second type has a lower peak to peak value, equal to 0.5, such as the two pairs {E15B7, D15C7} and {F31C7, 2B15B7}. However, for the two pairs {F31E15, F31D15} and {G63C7, G63B7}, the cross-correlation function is very small, about 0.2, except for some "spikes" where they reach ± 0.5 as shown in the Figure. The Figure also shows that for some periods of delay the cross-correlation value is not only constant but of a very small value, nearly zero. Similar results were found for the pair {F31C7, F31B7}, (not shown in Figure 5.5).

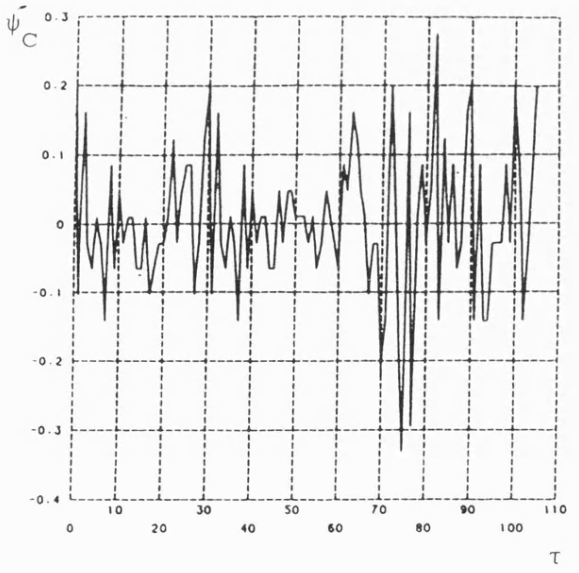
Further examination has been carried out with respect to the relationship between the inner and outer component of the composite sequence and their effect on the cross-correlation function. It was found that if the inner component is shorter than the outer component, such as those in Table 5.2 (b), some composite sequences show very low level cross-correlation functions, and some have no



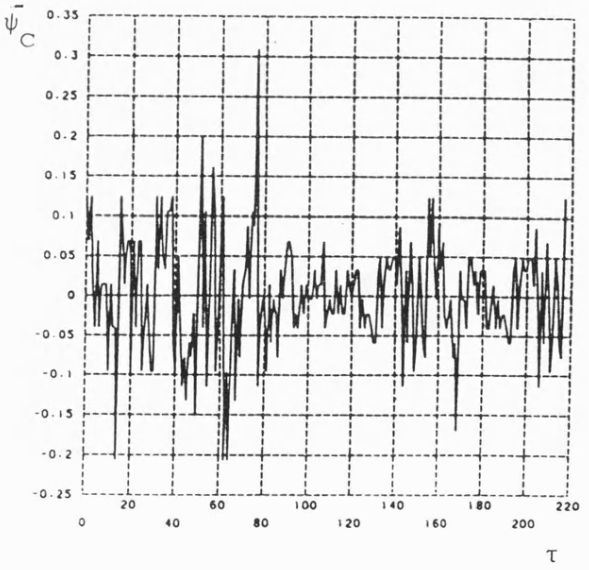
a) C7A3, B7A3



b) D15A3, E15A3

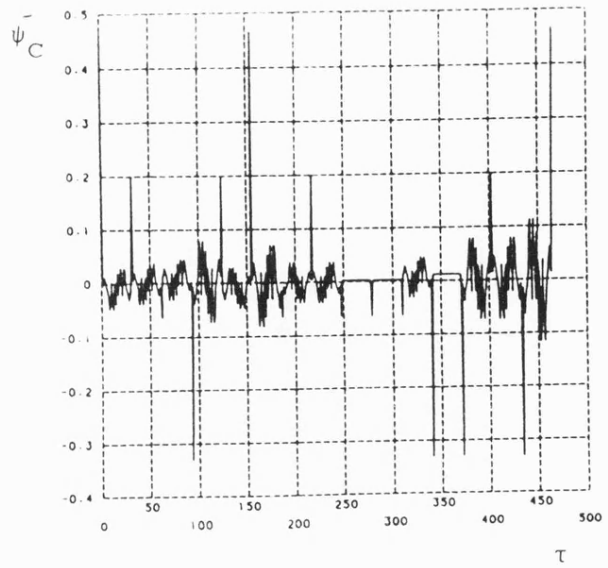


c) E15B7, D15C7

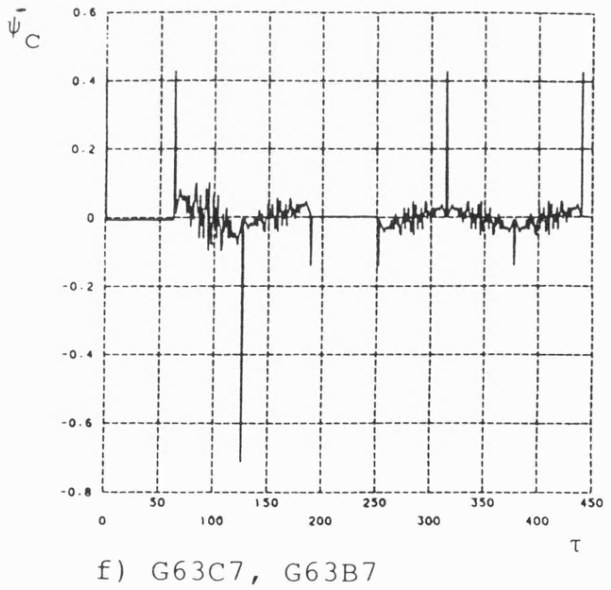


d) F31C7, 2B15B7

Figure 5.5. Some normalised cross-correlation functions of different composite sequences.



e) F31E15, F31D15



f) G63C7, G63B7

Figure 5.5 (Continued)

effect. The composite sequences {A3D15, A3E15}, (A3C7, A3B7}, and {B7E15, C7D15} are the codes having no effect. The cross-correlation function of the latter is shown in Figure 5.6. However, the pairs {D15F31, E15F31}, {C7F31, B7F31}, and {C7G63, B7G63} show a remarkably low and uniform cross-correlation function for most of the period (less than 0.04) except for a very short period, where the values reaches ± 0.5 as shown in Figure 5.6.

So it is clear now that:

1) The cross-correlation function of a pair of composite sequences is mainly dependent on the type of its component sequences.

2) If the outer component is longer than the inner component some composite sequences show extremely low cross-correlation function.

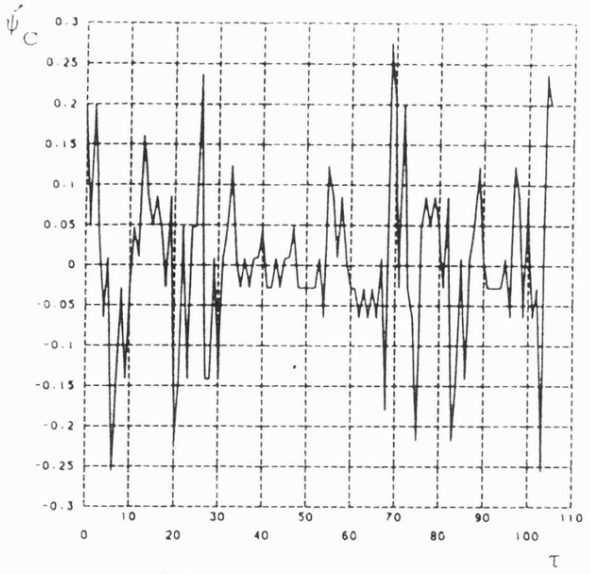
5.3.2 Auto-Correlation Function

The auto-correlation function refers to the degree of correspondence between a signal or a sequence and a phase-shifted replica of itself, or another identical one. Thus, equation 5.5 can be rewritten as:

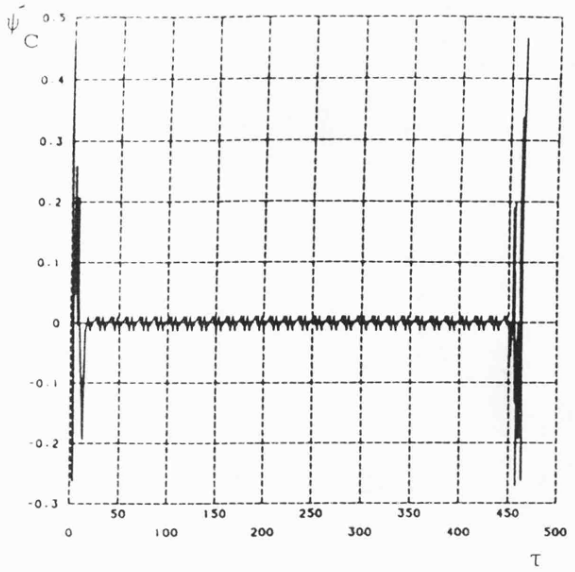
$$\Psi_z(\tau) = \sum_{k=0}^{L-1} Z(k)\, Z(k+\tau) \qquad 5.18$$

where $\Psi_z(\tau)$ is the auto-correlation function of the sequence Z.

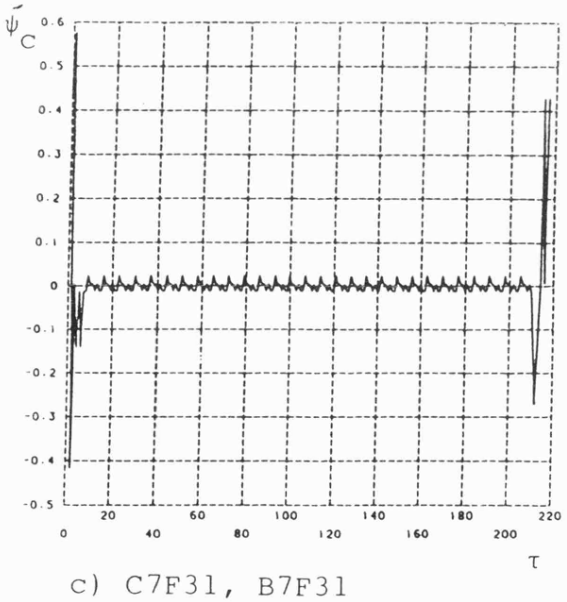
By making the inner component $U_1=U_2=U$ and the outer component $V_1=V_2=V$, the two composite sequences Z_1 and Z_2 will be the identical sequence, Z. The auto-correlation function of this composite sequence Z could be expressed in terms of the auto-correlation



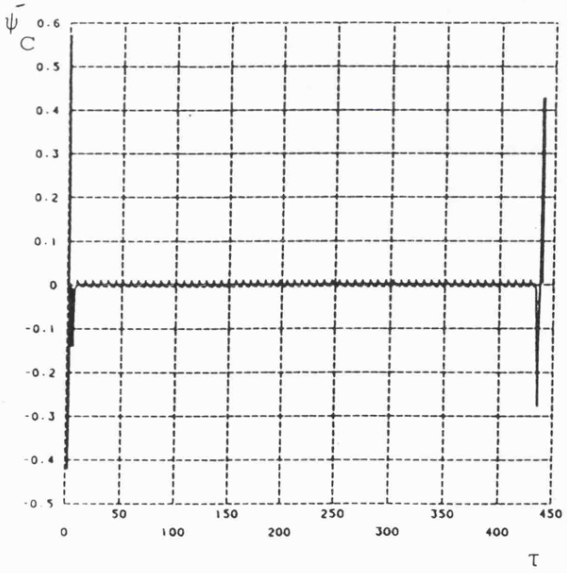
a) B7E15, C7D15



b) D15F31, E15F31



c) C7F31, B7F31



d) C7G63, B7G63

Figure 5.6. Some normalised cross-correlation functions of different composite sequences

function of its inner component U and outer component V for $\tau = \tau_v n_u$, $\tau_v = 0,1,2 \ldots (n_v-1)$, as

$$\Psi_Z(\tau) = \Psi_u(o)\ \Psi_v(\tau_v) \qquad 5.19$$

Similarly equation 5.12 becomes

$$\Psi_Z(\tau) = \phi_u(\tau_u)\Psi_v(\tau_v)+\phi_u(\tau_u-n_u)\Psi_v(\tau_v+1) \qquad 5.20$$

for $0 \leqslant \tau_v \leqslant n_v-1$, $0 \leqslant \tau_u \leqslant n_{u-1}$, and $\tau=\tau_v\tau_u+\tau_u$

i.e. for $0 \leqslant \tau \leqslant n_u n_v-1$

And for the same range the aperiodic and odd auto-correlation function is

$$\hat{\Psi}_Z(\tau) = \phi_u(\tau_u)\ \hat{\psi}_v(\tau_v)+\phi_u(\tau_u-n_u)\ \hat{\Psi}_v(\tau_v+1) \qquad 5.21$$

Alternatively, it is also possible to express the auto-correlation function from equation 5.17.

$\Psi_z(\tau)$ = number of bit agreements - number of bit disagreement

5.22

where $\tau = 0, 1, 2, .. n-1$ and the sequence is compared bit by bit with itself.

The normalised auto-correlation function is:

$$\Psi_Z(\tau)=\frac{\Psi_Z(\tau)}{\text{total number of sequence bits}} \qquad 5.23$$

Again here a comparison is made between the auto-correlation of some composite sequences and their component sequences, i.e. with a standard maximal length sequence. It is well known by now that the auto-correlation function of a maximal length sequence has two levels, L and -1 (or 1 and -1/L respectively for the normalised auto-

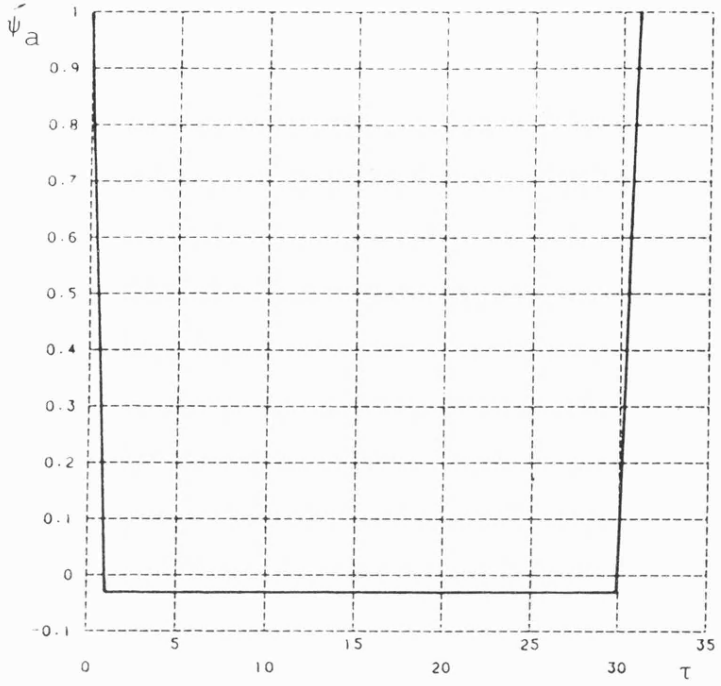


Figure 5.7. Normalised auto-correlation function of maximal length sequence of 31 bits.

correlation function, as shown in Figure 5.7 for a sequence of length 31 bits).

However, the auto-correlation function of the composite sequence is different from that of the maximal length sequence. The same composite sequences constructed from table 5.1, which are tabulated in Figure 5.2(a) and (b), were chosen to find out their auto-correlation function and their properties. First, we take the case where the inner component is longer than the outer component as those in Table 5.2(a). Figure 5.8 shows the auto-correlation function of four different composite sequences, C7A3, E15C7, F31D15, and G63B7.

For those of table 5.2(b) where the inner component is shorter than the outer component such as, A3C7, C7D15, D15F31, and B7G63 are shown in Figure 5.9. And for those where the inner and outer component are equal such as B7C7, C7B7, D15E15, and E15D15 are shown in Figure 5.10.

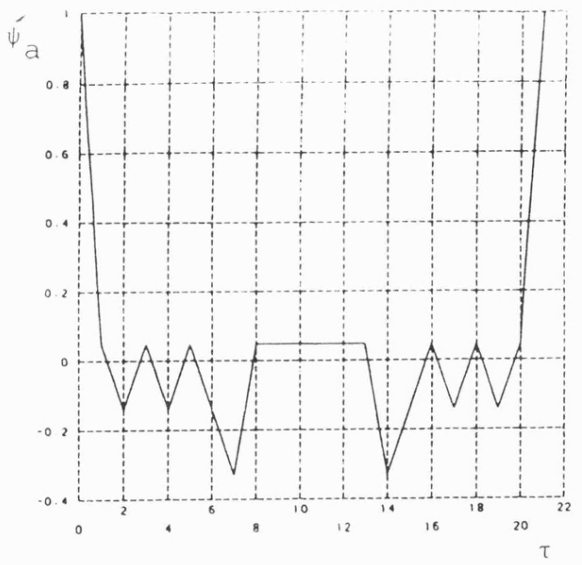
By careful examination of the above results in Figures 5.8 to 5.10, several important points are noticed:

a) For every inner component sequence period n_u there is one negative peak triangle of amplitude $-n_u$.

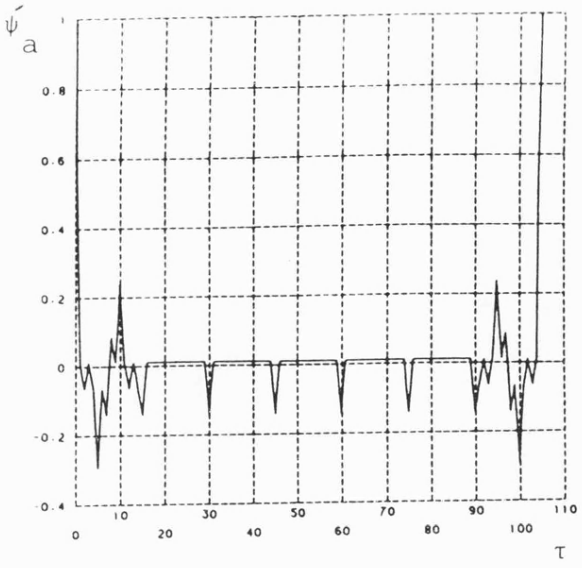
b) The number of the negative triangles is equal to the period of the outer component sequence minus one i.e. n_v-1. All these negative peaks are of equal amplitude.

c) For every $n_u n_v$ there is a maximal positive peak triangle of amplitude $n_u n_v$.

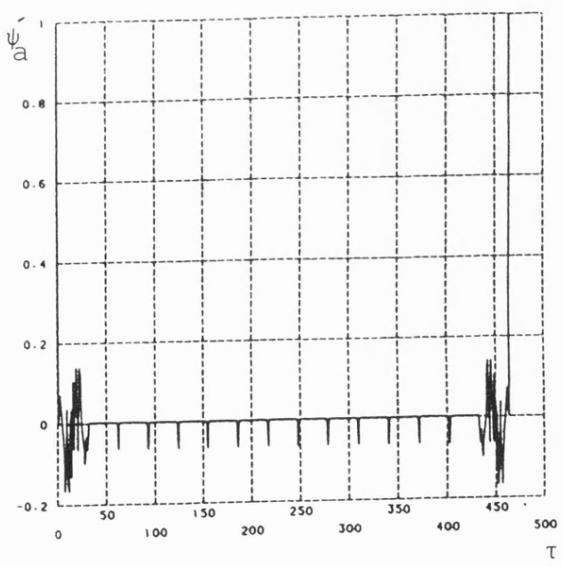
d) From zero the first $\pm n_u$, the auto-correlation functions distribution depends on the inner component sequence only, and



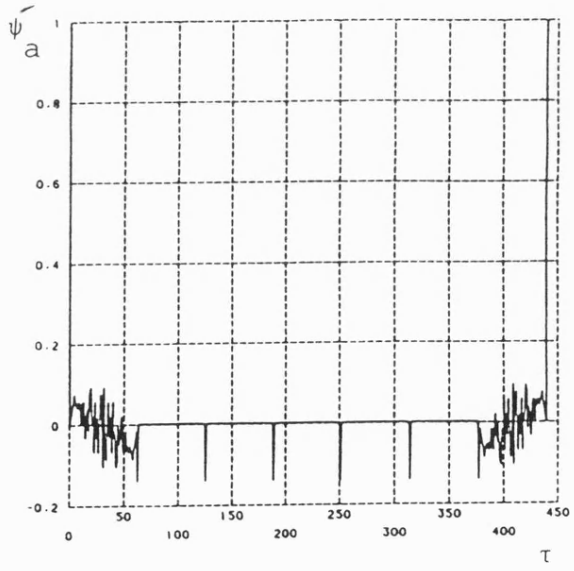
a) C7A3



b) E15C7

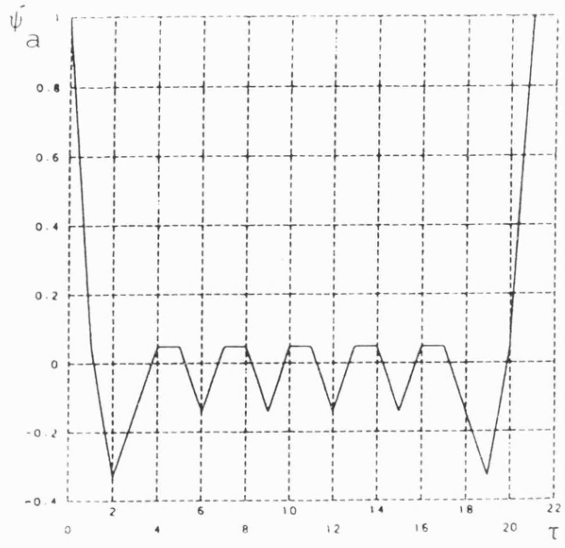


c) F31D15

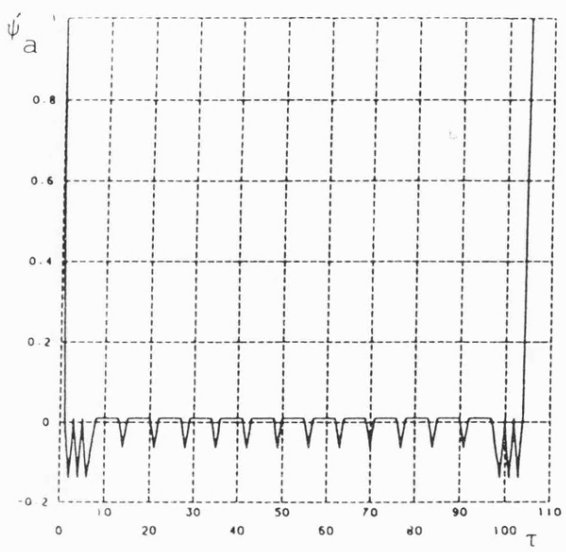


d) G63B7

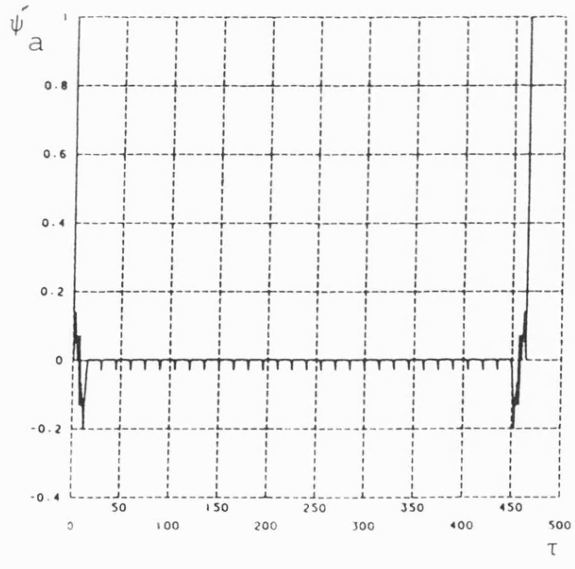
Figure 5.8. Some normalised auto-correlation function of different composite sequences (U>V).



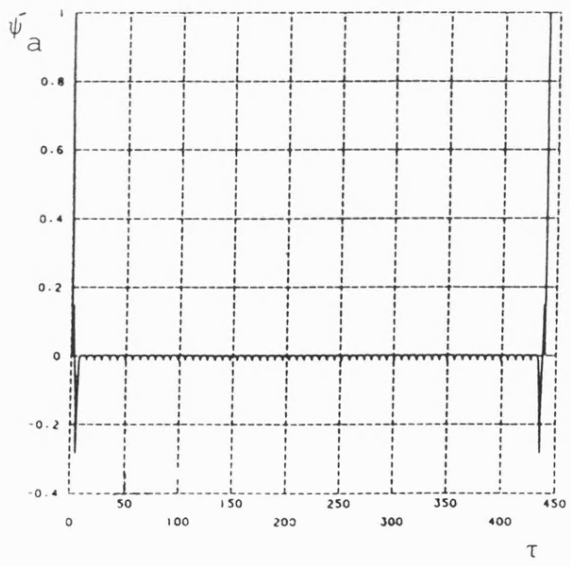
a) A3C7



b) C7D15

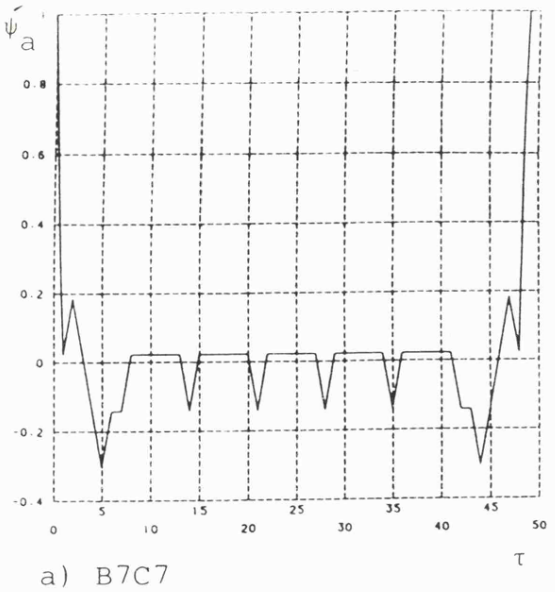


c) D15F31

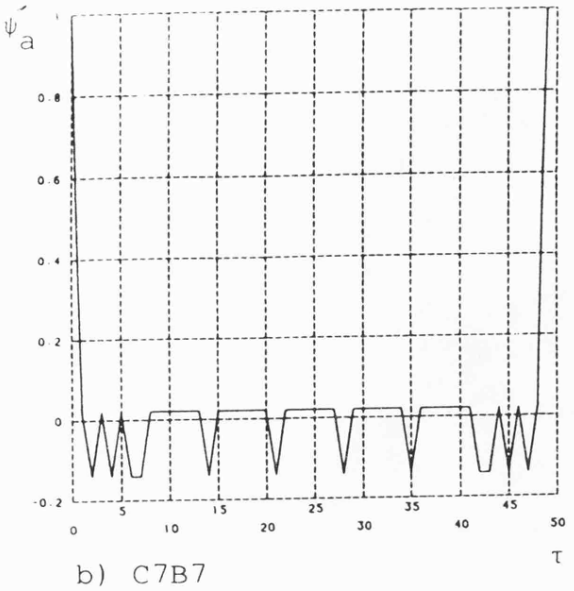


d) B7B63

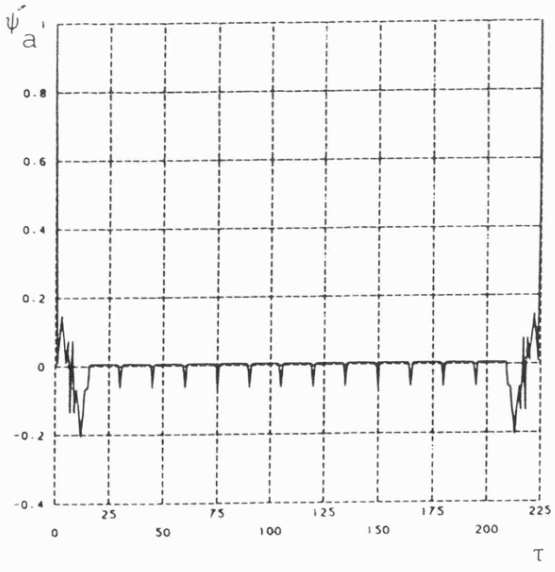
Figure 5.9. Some normalised auto-correlation functions of different composite sequences (U<V).



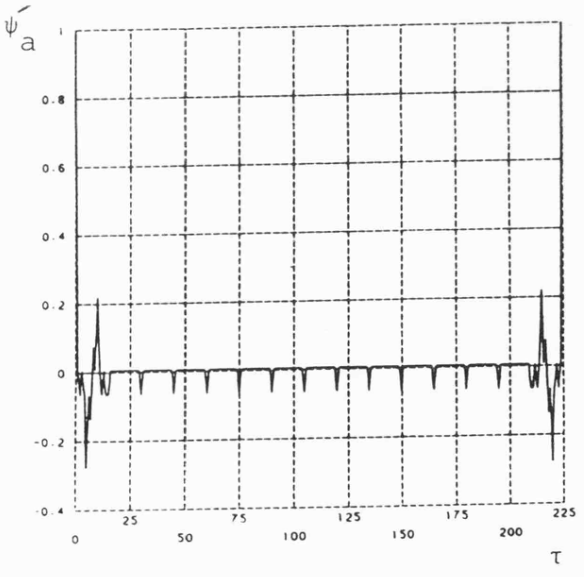
a) B7C7



b) C7B7



c) D15E15



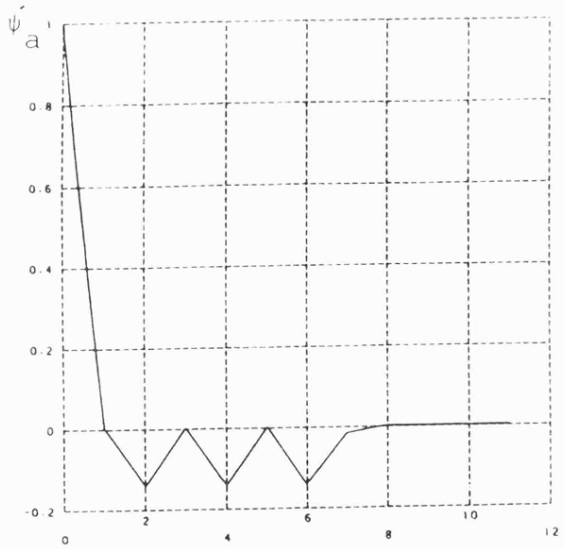
d) E15D15

Figure 5.10. Some normalised auto-correlation functions of different composite sequences (U=V).

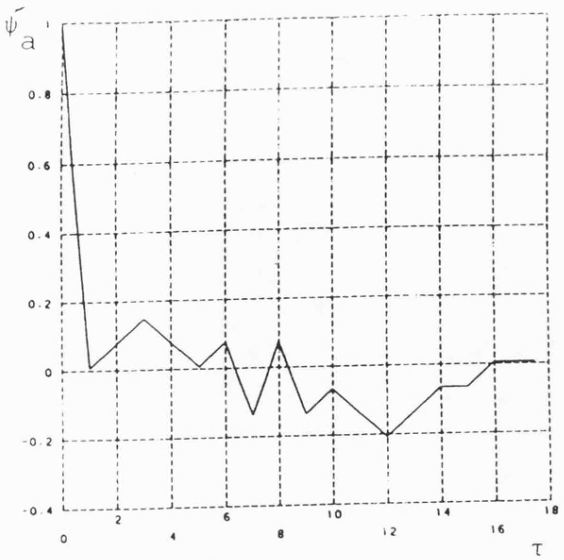
not on the outer component sequence. Figure 5.11 illustrates this point very clearly. From 0 to $+n_u$ a portion of the auto-correlation function of the composite sequence C7G63 is plotted in Figure 5.11(a). A similar function would be found for C7F31, C7D15, C7E15, C7B7 and so on as long as the inner component is the same for all these composite sequences. The same applies to D15E15, F31D15, and G63C7 shown in Figure 5.11(b) (See Figure 5.10(c)), 5.11(c) (See Figure 5.8(c)), and 5.11(d) respectively. So a careful choice of this component sequence may be advantageous especially in the synchronisation process at the receiver end, where the index of discriminator should be as large as possible. It is noticed that the shorter the inner sequence the lesser the number of "zigzags" in this region. It is also noticed that if the inner component is shifted by one or more bits for a particular composite sequence a different zigzag form is produced from 0 to $\pm n_u$ as shown in Figure 5.12 (a to g) for all shifts of a composite sequence B7C7 shown earlier in Figure 5.10(a).

e) Between every two successive n_u, with the exception of the first and the last n_u, there is a flat auto-correlation function which is equal to $1/n_u n_v$, which could be considered in general to be out of phase auto-correlation function similar to -1/L for maximal length sequences.

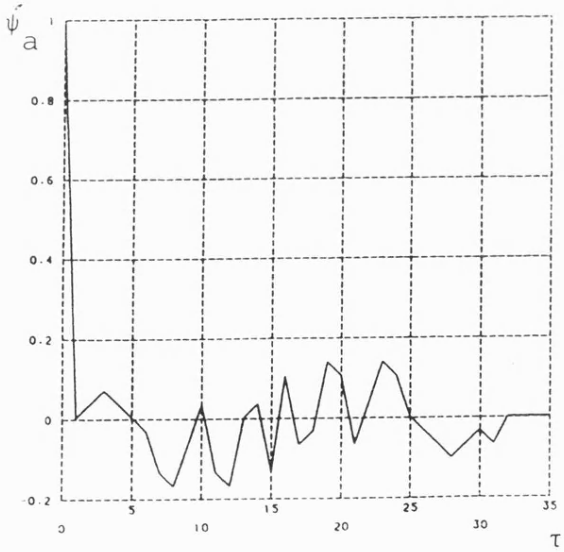
f) The maximum positive peak which is equal to $n_u n_v$ always starts and ends at a value of $1/n_u n_v$ at ± 1 bit shift (which is the same value in e) above).



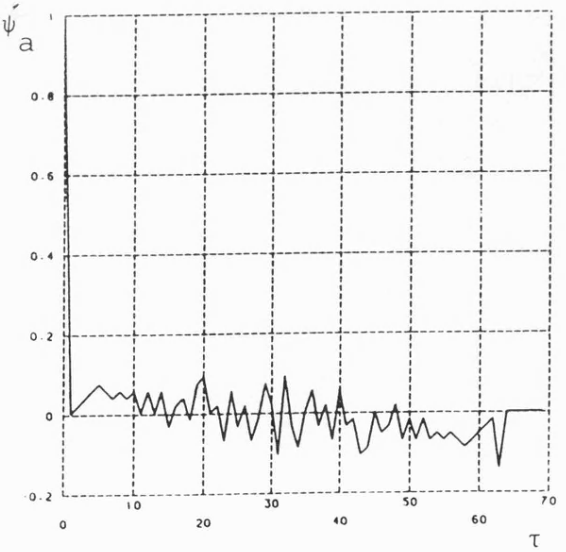
a) C7G63



b) D15E15



c) F31D15



d) G63C7

Figure 5.11 More detailed normalised auto-correlation function for selected composite sequences (from 0 to n_u).

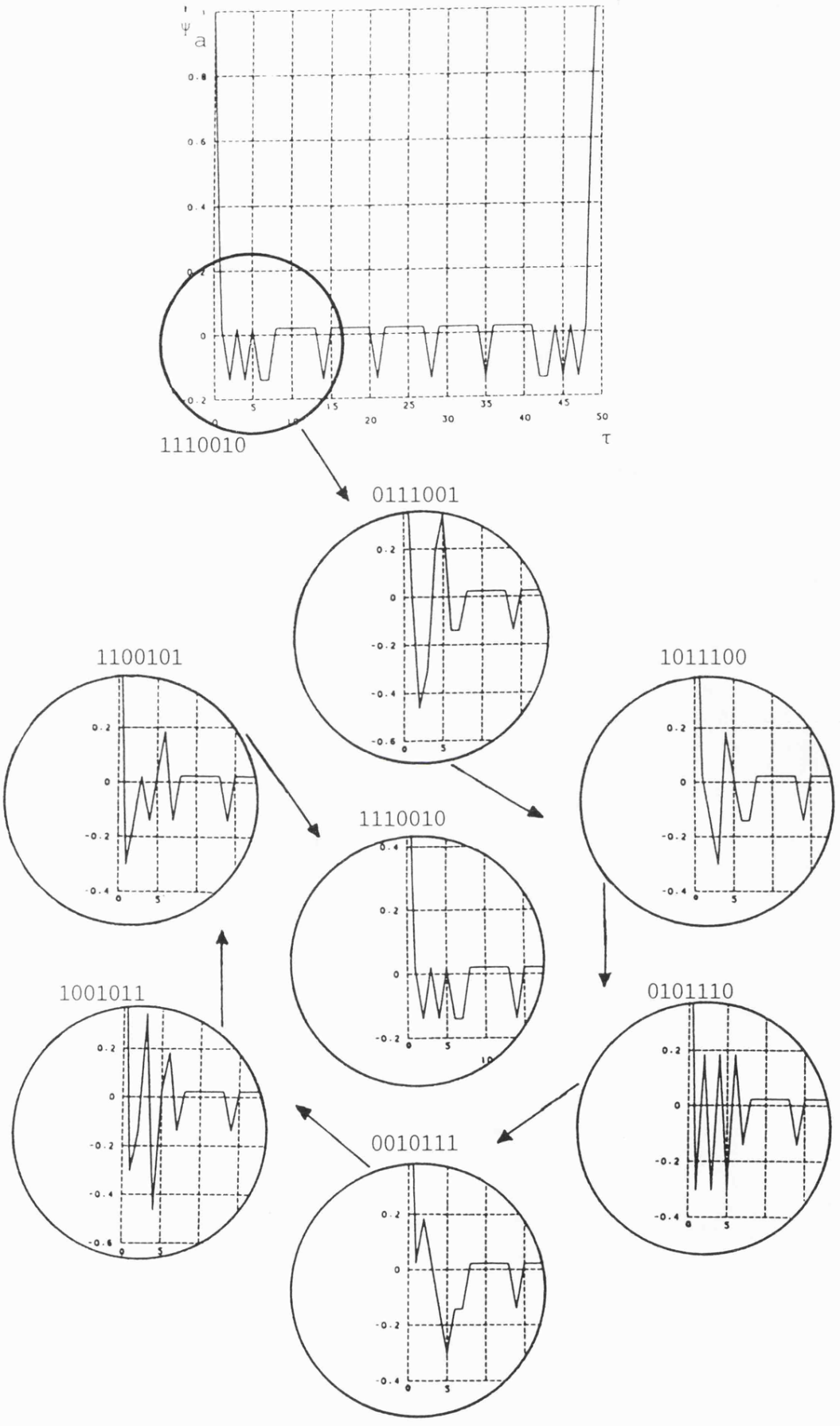


Figure 5.12. Bit by bit normalised auto-correlation function variation due to shift of inner component, composite sequence is C7B7.

g) Since the period of the composite sequence is equal to $n_u n_v$, so to get higher amplitude inner auto-correlation triangle function, one can increase n_u and decrease n_v (or vice versa) keeping $n_u n_v$ unchanged. Also the interval between them could be increased or decreased by decreasing or increasing n_v respectively.

h) If the composite sequence is auto-correlated with an inverse version of itself, a negative auto-correlation function is produced. The inverse version of the composite sequence could be generated simply by inversing the outer component sequence only.

As has been mentioned earlier, there is no restriction to use only maximal sequences as component sequences to generate composite sequences. Other sequences such as Barker and Gold sequences may be used as well, but the earlier stated properties, or part of them are no longer applicable since they were obtained for composite sequences generated from maximal length sequences. Figure 5.13 shows the auto-correlation functions of some composite sequences generated from Barker code as an inner and outer component. Very few Barker codes are known [16], as listed in Table 5.3, and some possible related composite sequences are tabulated in Table 5.4. From Figure 5.13 and close examination of many other auto-correlation functions of composite sequences constructed from Barker code component, the following points were noticed:

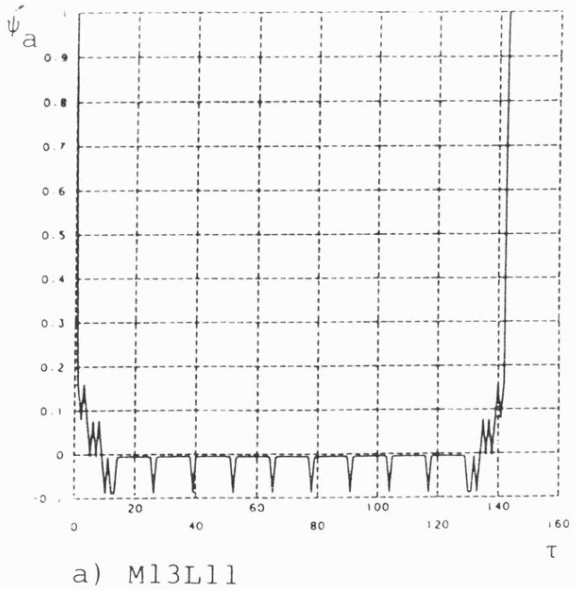
a) The earlier properties are still applicable to some Barker composite sequences such as L11K7, K7L11, J5L7, and M13L11 (the later is shown in Figure 5.13a), or in general any composite sequence whose outer component is a Barker code which has an

Sequence Symbol	Sequence length	Sequence +1 = + 0 or -1 = -
H3	3	+ + - .
I4	4	+ + + - .
J5	5	+ + + - + - - .
K7	7	+ + + - - + - .
L11	11	+ + + - - - + - - + - .
M13	13	+ + + + + + - - + + - + - .

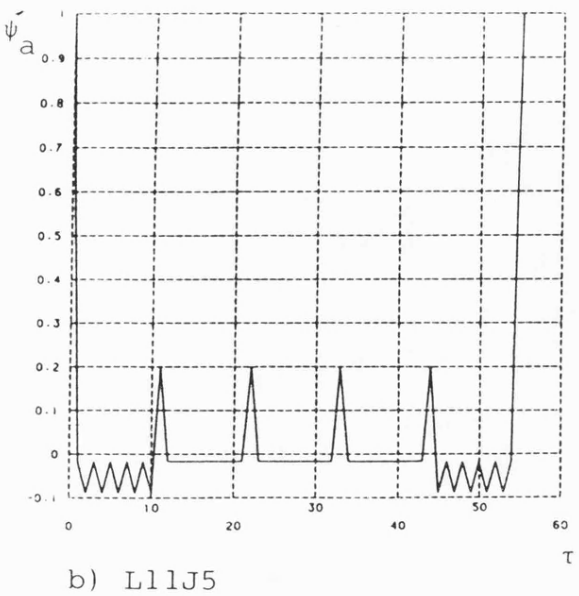
Table 5.3 Barker codes [18].

C. Sequence Symbol	Inner Component	Outer Component	C. Sequence length
H3I4	H3	I4	12
I4H3	I4	H3	12
I4J5	I4	J5	20
J5I4	J5	I4	20
I4L11	I4	L11	44
L11I4	L11	I4	44
J5L11	J5	L11	55
L11J5	L11	J5	55
J5M13	J5	M13	65
M13J5	M13	J5	65
K7LH	K7	L11	77
L11K7	L11	K7	77
L11M13	L11	M13	143
M13L11	M13	L11	143

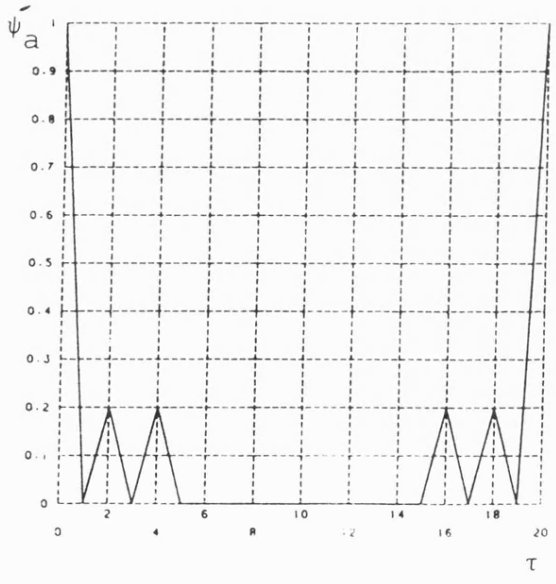
Table 5.4. Some possible composite sequences generated from Barker codes



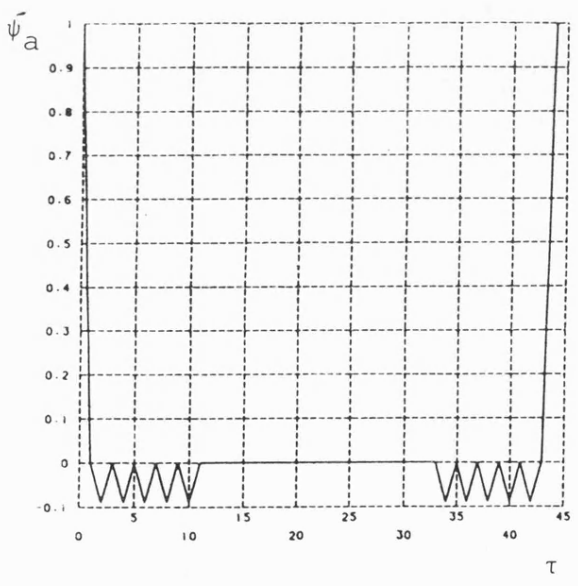
a) M13L11



b) L11J5



c) J5I4



d) L11I4

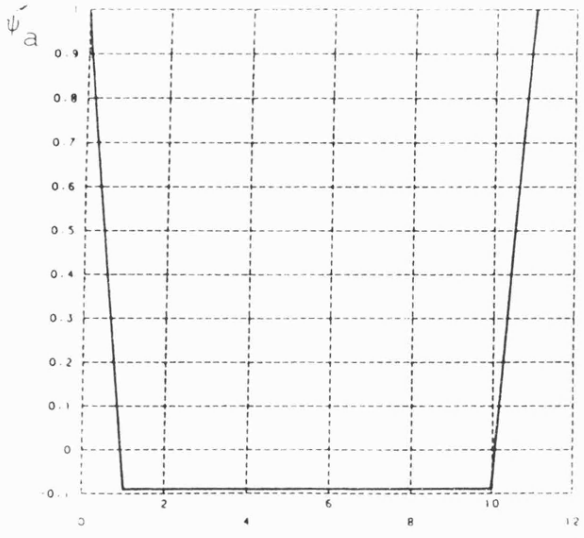
Figure 5.13. Some normalised auto-correlation functions of composite sequences generated from Barker codes.

auto-correlation function similar to that familiar one shown in Figure 5.14(a) for a H3, K7, and L11. These codes are very similar to the maximal length codes.

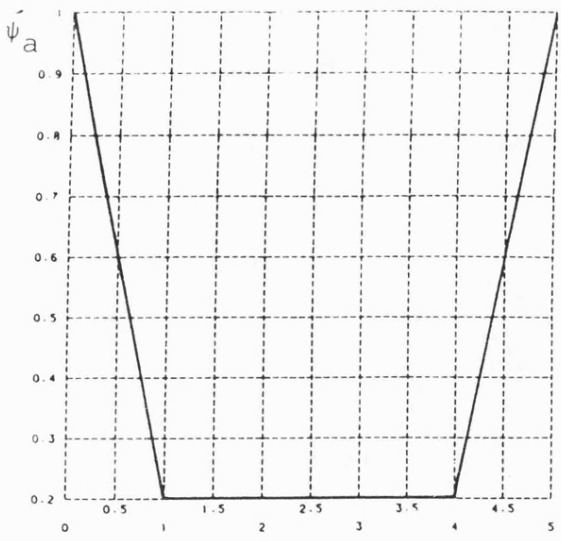
b) If the outer component sequence has an auto-correlation function such as that shown in Figure 5.14(b) for a J5 and M13, where the out-of-phase auto-correlation function is +1/L instead of -1/L, the inner triangle auto-correlation function inverted to positive instead of negative as shown in Figure 5.13(b) for a L11J5 composite sequence. Most other properties remain applicable.

c) For those outer component codes whose out-of-phase auto-correlation function is zero, such as I4, which is shown in Figure 5,14(c), the auto-correlation function of their composite sequence shows no inner triangle correlation functions, as shown in Figure 5.13 (c,d) for J5I4 and L11I4 composite sequences respectively.

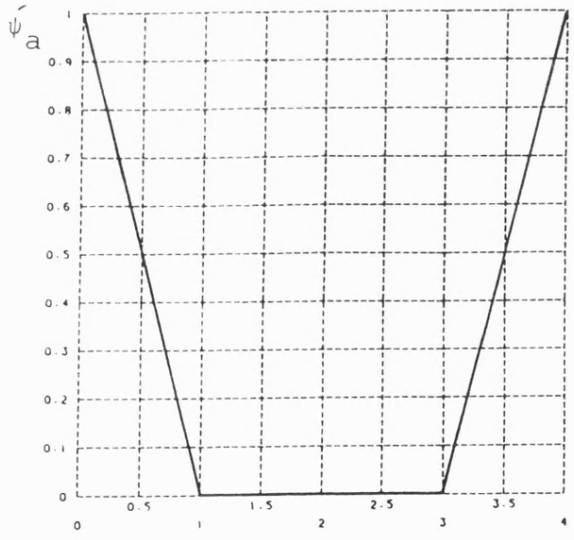
The reason for these differences is very obvious. It is related to the type of Barker code used as an outer component of the composite sequence, and more precisely on its out-of-phase auto-correlation function, because this value is to be multiplied by the in-phase auto-correlation function of the inner component sequence to form the final auto-correlation function. As far as the cross-correlation function of Barker component sequence is concerned, no particular differences were found compared with the earlier maximal composite sequences.



a) L11



b) J5



c) I4

Figure 5.14. Normalised auto-correlation functions of different Barker codes.

5.3.3 Power Spectral Density

The most straightforward method of calculating the power spectral density of a particular signal is from its auto-correlation function as seen earlier. The auto-correlation function and the power spectral density are related by:

$$\Psi(\tau) = \int_{-\infty}^{\infty} S(\omega)\ e^{J\omega\tau}\ df$$

and

$$S(\omega) = \int_{-\infty}^{\infty} \Psi(\tau)\ e^{-j\omega\tau}\ d\tau$$

where $\Psi(\tau)$ is the auto-correlation function and S(f) is the power spectral density of the signal in watts/Hz. This relationship is known as the Wiener-Khintchine theorem [25].

The process of generating the composite sequence is similar to the process of modulating a high speed binary spreading code by a known low rate binary data using sequence inversion keying modulation SIK. The transmission bandwidth is a direct function of the code bit rate. Code repetition rate is also a function of bit rate, that is code repetition rate,

$$R_c = \frac{\text{Clock rate in bits per second}}{\text{Code length in bits}}$$

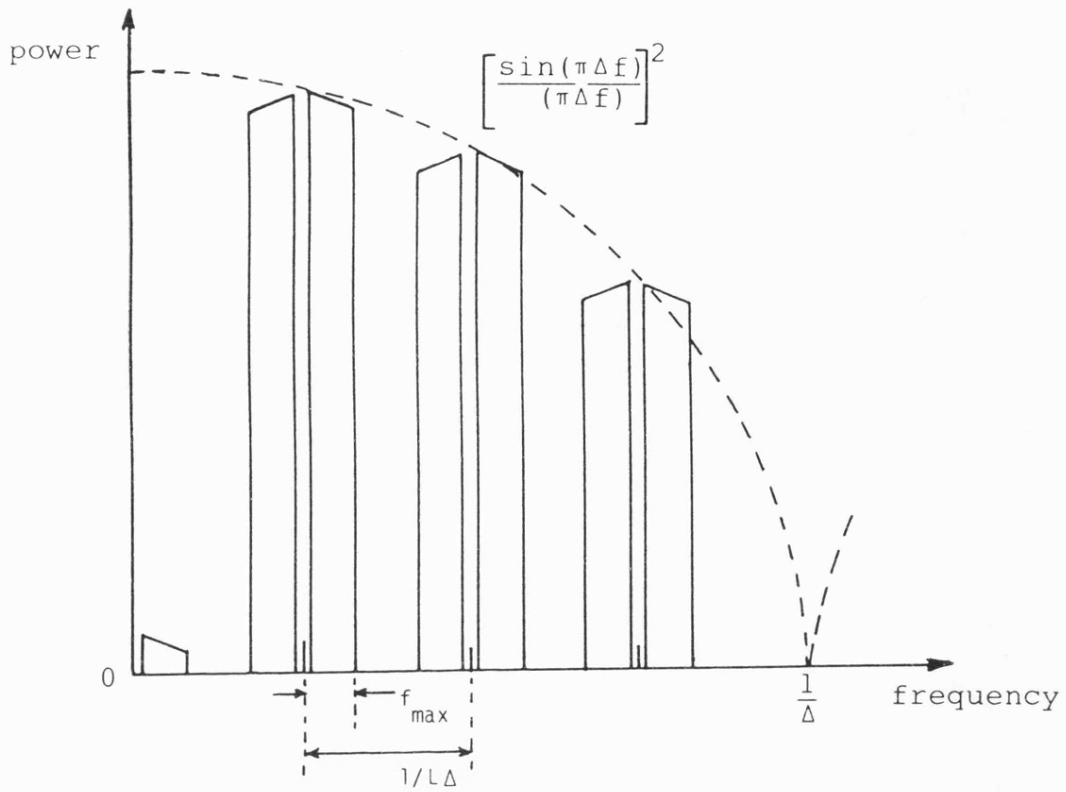
This repetition rate determines the line spacing in the radio frequency output spectrum and is an important consideration in a system design. Dixon [15) stated that it is advisable that a direct

sequence system's code repetition rate be adjusted by choosing a satisfactory code length so that it will not lie in the information band. Otherwise, unnecessary noise will be passed into the information demodulators, especially under jammed conditions. The space between the lines is narrow when the repetition rate of the code is low and vice-versa.

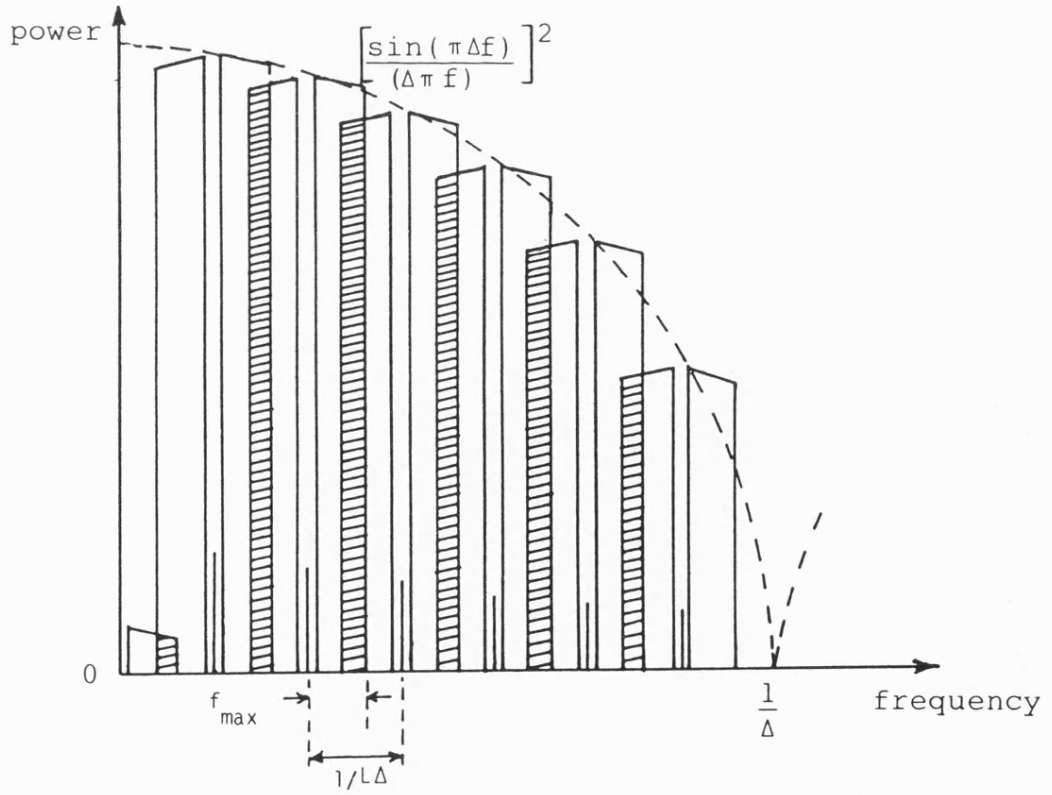
For a composite sequence, the inner component could be considered or treated as a binary spreading code in a direct spread spectrum system, and the outer component as a binary information or data. Its repetition rate clearly depends on the length and rate of the inner component sequence length as well as its own length. Perhaps nothing can be done with respect to the rate of the component code because this determines the bandwidth of the overall transmitted spread spectrum system and perhaps the transmitted channel. Therefore and according to the first point raised above, one needs to have a careful selection of the inner and outer component sequence lengths. Ormondroyd and Shipton [19] have shown that if a conventional non-spread spectrum receiver has sufficient selectivity and dynamic range, it can be used to receive the spread spectrum information in a direct sequence system by scanning the receiver across the main lobe bandwidth if the following relationship is held for the spread spectrum system:

$$2\ f_{max} \leqslant 1/L\Delta \qquad 5.24(a)$$

where f_{max} is the maximum frequence component of the information. This is shown clearly in Figure 5.15(a). So without any knowledge of the spreading code one can detect the data if operated in the common



a) Direct-sequence with contiguous sidebands



b) Direct-sequence with non-contiguous sidebands.

Figure 5.15. Power spectral density of direct-sequence [19].

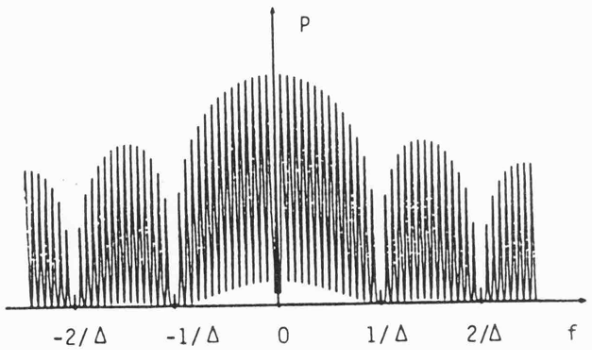
bandwidth. Therefore this type of transmission is not secure. However, Figure 5.15(b) shows a spectrum where:

$$2 f_{max} > 1/L\Delta \qquad 5.24(b)$$

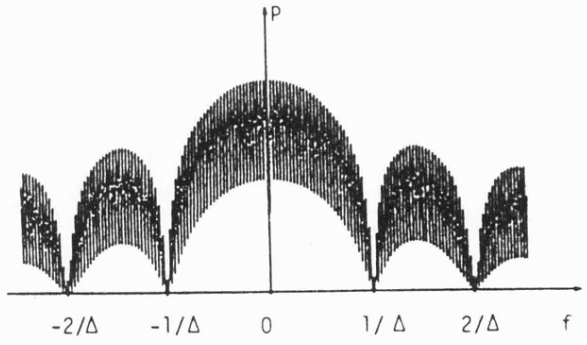
in which the sidebands now overlap considerably, which make it very difficult to a conventional receiver to receive the information without knowledge of the spreading code. This is mainly because of the aliasing noise due to the sidebands overlapping, which leaves the transmission to be secure. Al-Rawas [20] has shown several experimental power spectral densities for different maximal sequence lengths unmodulated and modulated with data, some of his results are shown in Figure 5.16. The rate of the spreading code is 10 kbps and the data rate is 110 bps. Figure 5.16(a,b) satisfies the relationship 5.24(a) for sequence lengths of 15 and 31 respectively, the sidebands of the data are clearly not seen overlapping as those of Figure 5.16(c,d) for sequence lengths of 63 and 511 respectively, where the relationship 5.24(b) is maintained. The other noticeable point of Figure 5.16, is that as the code length increases, the power spectral density becomes closer to a white noise power spectral density.

It is therefore also important to take this point into consideration when designing a direct sequence system using a composite sequence. Again the outer component sequence is involved because it is n_u slower than the inner component sequence and it is considered to be similar to the binary information or data just described.

The power spectral density of different composite sequences are shown in Figure 5.17. These are calculated from the auto-correlation

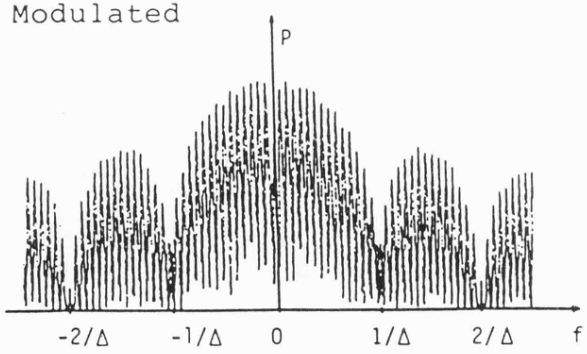


Unmodulated

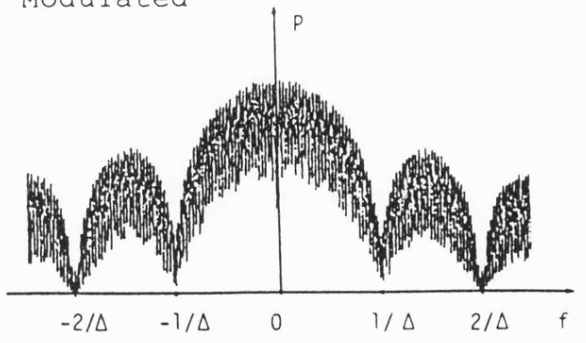


Unmodulated

Modulated



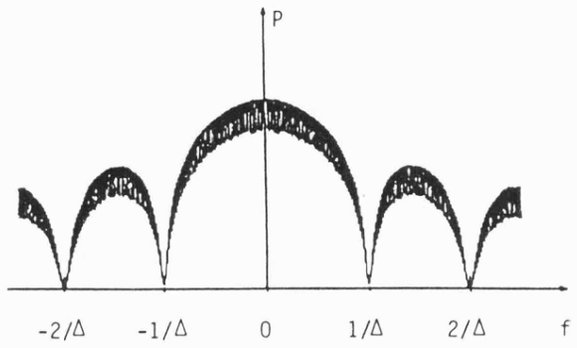
Modulated



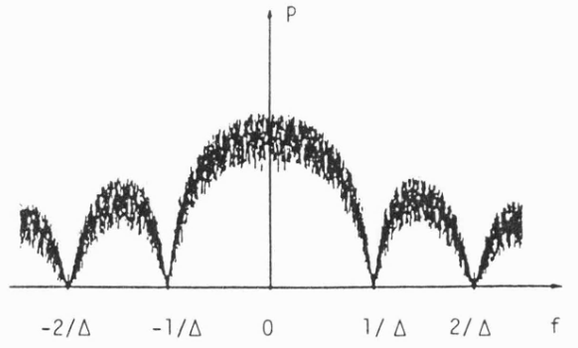
a) 15 bits sequence

b) 31 bits sequence

Figure 5.16. Power spectral density of different length maximal sequences, sequence rate = 10 kbps, data rate = 110 bps. [20].

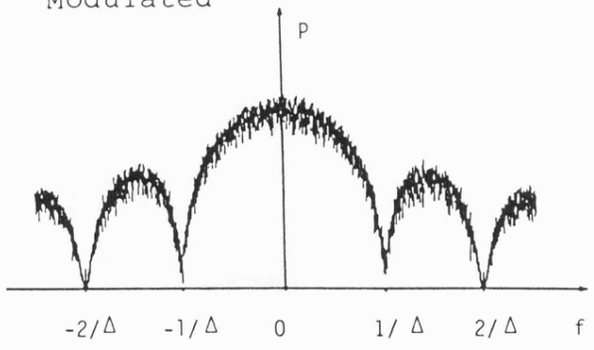


Unmodulated



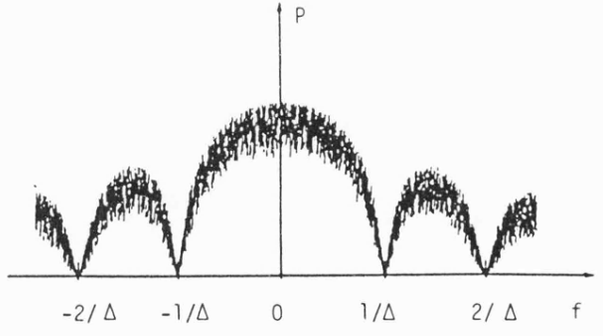
Unmodulated

Modulated



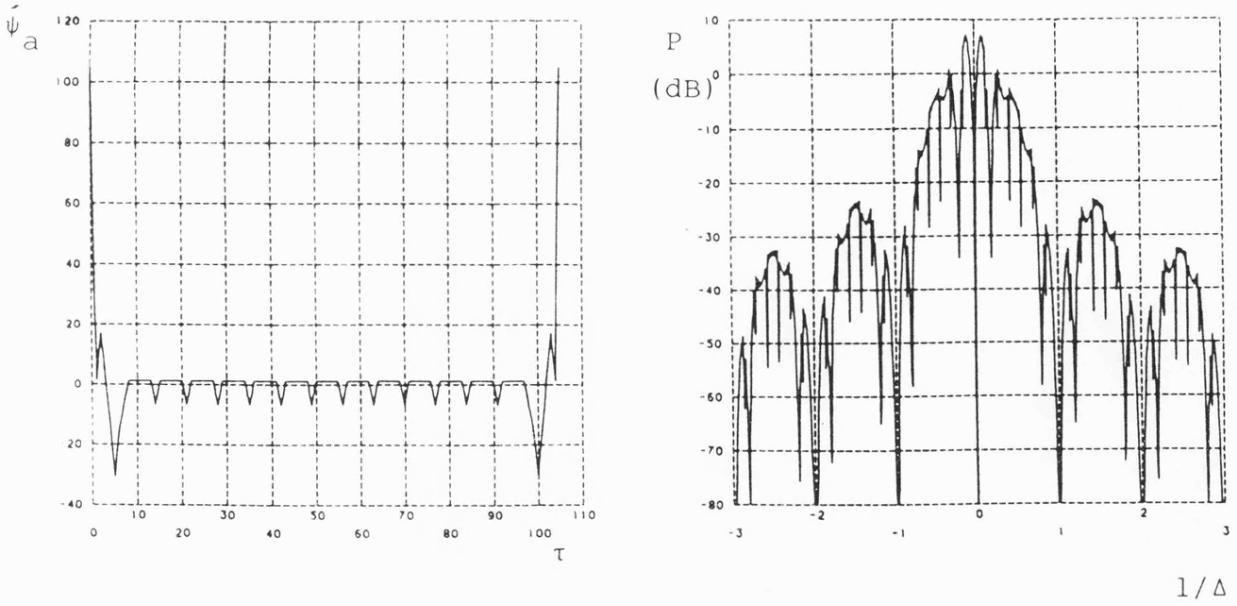
c) 63 bits sequence

Modulated

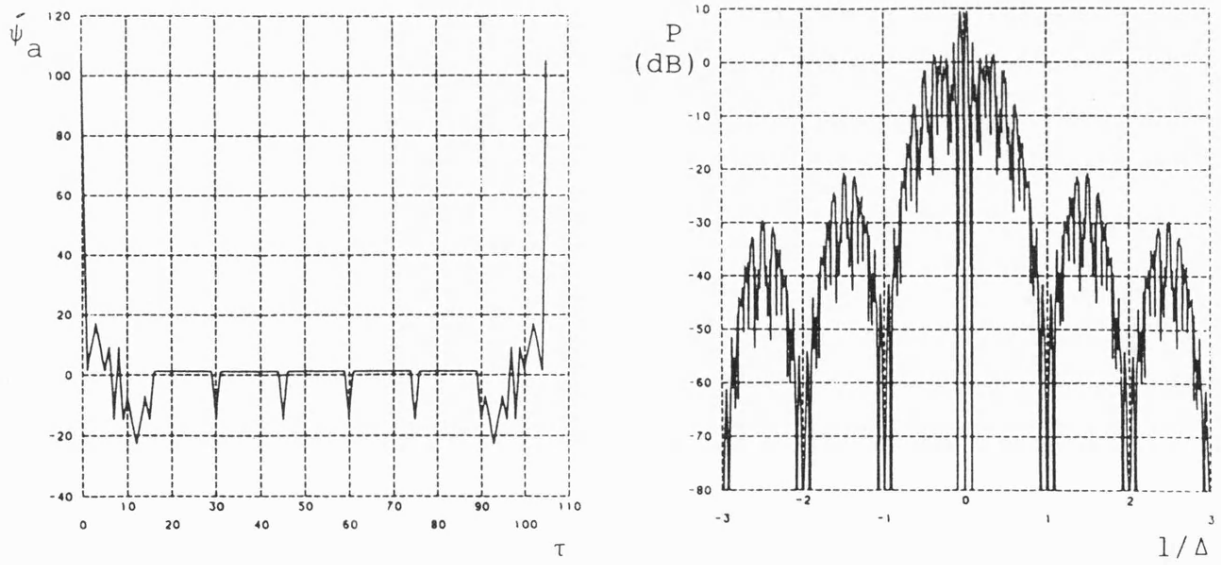


d) 511 bits sequence

Figure 5.16. (Continued).

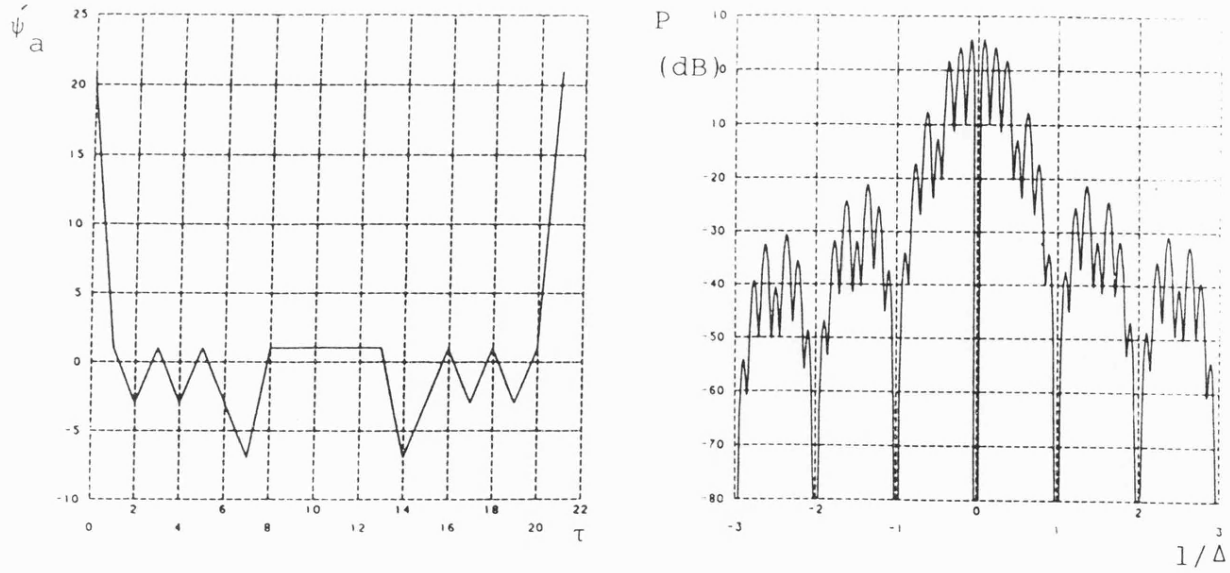


a) C7A3



b) A3C7

Figure 5.17. Some normalised power spectral density of different composite sequences and their autocorrelation functions.



c) B7D15

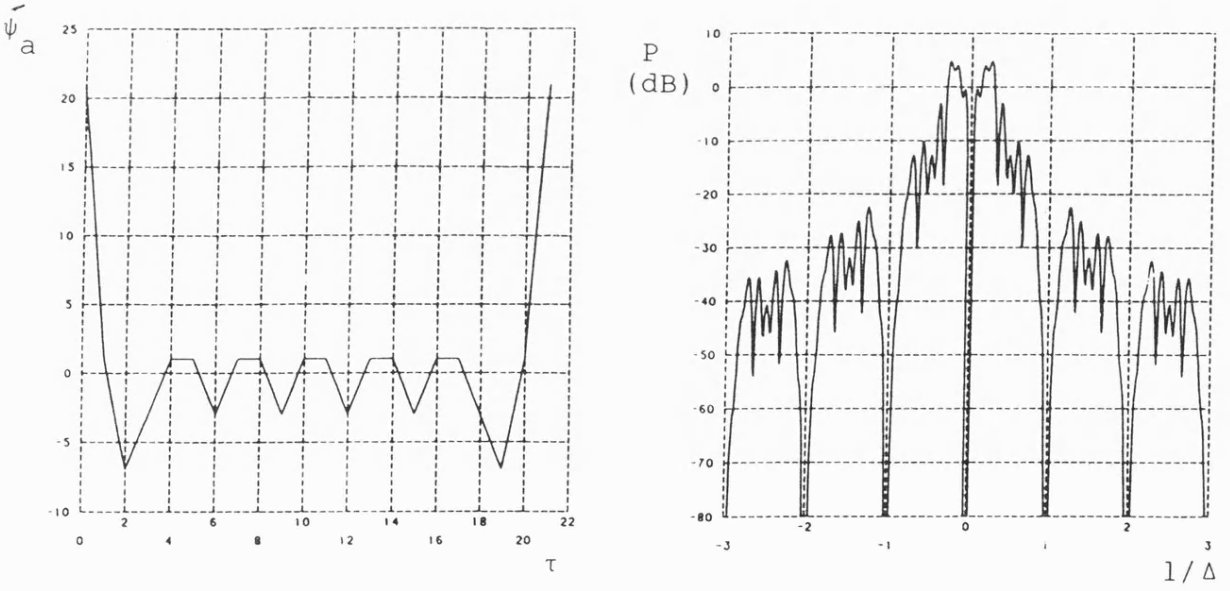
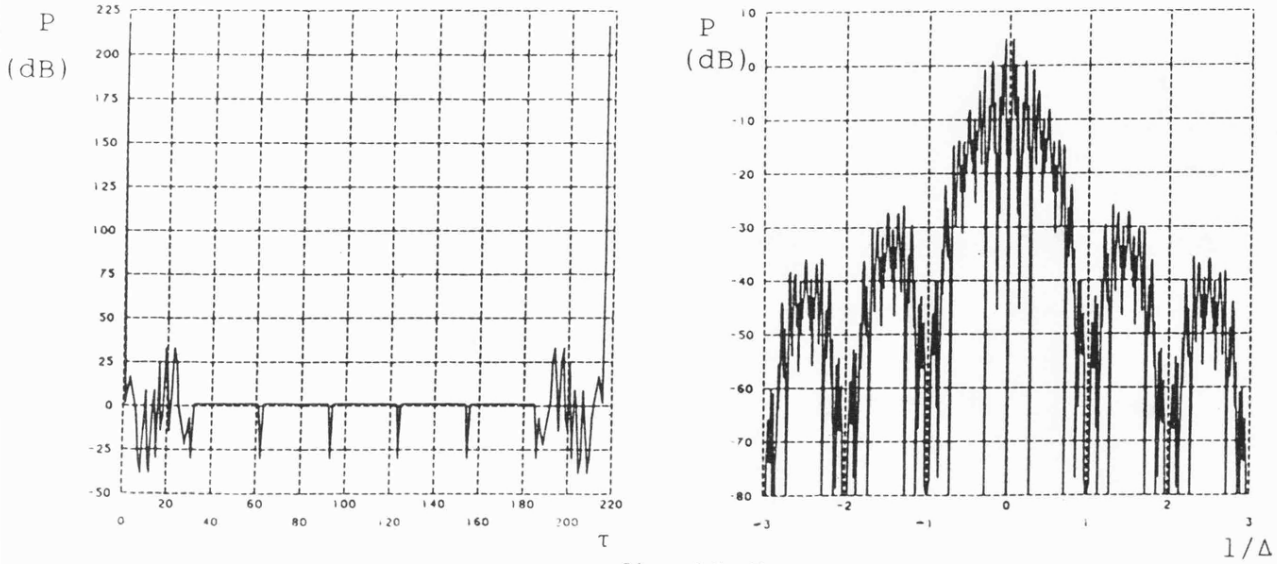


Figure 5.17 (Continued).



d) F31C7

Figure 5.17. (Continued).

function of their composite sequences themselves. The general shapes of these power spectral densities have the form of the sinc function. The space between the lines are wide for short codes as shown in Figure 5.17 (a,b) for C7A3 and A3C7 composite sequences respectively. When the sequence length increases as in (c, d, e) for B7D15, D15C7 and F31C7 respectively the spectra becomes closer to the noise like spectra. The null to null bandwidth is twice the bit rate of the inner component sequence.

5.4 RECEPTION OF THE COMPOSITE SEQUENCE

It is important for any spread spectrum receiver to synchronise and track the incoming signal, and codes used for this purpose should have two important properties. The first one is that the acquisition time should be as short as possible so that as little data as possible is lost, during synchronisation and also when the phase of the received sequence is being tracked. The second one is that it must be possible for the sequence to be recovered in very low signal to noise ratios which, as shown previously might be as low as -30dB.

If conventional loops for synchronisation such as the delay lock loop and Tau-dither loop are to be used to acquire synchronisation to the whole composite sequence, the acquisition time will be very long, when a long composite sequence is used. This may appear to be contradictory to one of the main reasons why the composite sequence is used and that is to minimise the acquisition time of synchronisation. So modifications to the existing synchronisation techniques are necessary to enable them to receive the composite sequences in short acquisition time.

Two different kinds of techniques will be presented here, which tackle the synchronisation problem of a composite sequence.

5.4.1 Rapid Acquisition Using Passive Correlators

The important parameters of the design of a matched filter for any sequence are the time delay required for the filter and its bandwidth. These two points are related to the duration of one period of the sequence and its chip-rate respectively. If a conventional sequence is to be used with a period n_z chip and a chip-rate of T_u second, we need a matched filter having a bandwidth of $1/T_u$ and a delay of $n_z T_u$ second. The capabilities of current surface acoustic wave devices do not permit the use of long sequences and/or very high chip-rate [21, 22].

However, a long composite sequence is made of two (or more) **short** component sequences, and the chip-rate of the outer component is much slower than the inner component sequence and the net clock rate of the composite sequence. This makes the use of the surface acoustic wave matched filter for a composite sequence more likely and regains the advantage of its rapid acquisition properties. However, these SAW devices cannot work under very low signal to noise ratios because of dynamic range problems, and this is considered a major disadvantage, which is different from an active correlator, as will be seen in the next section.

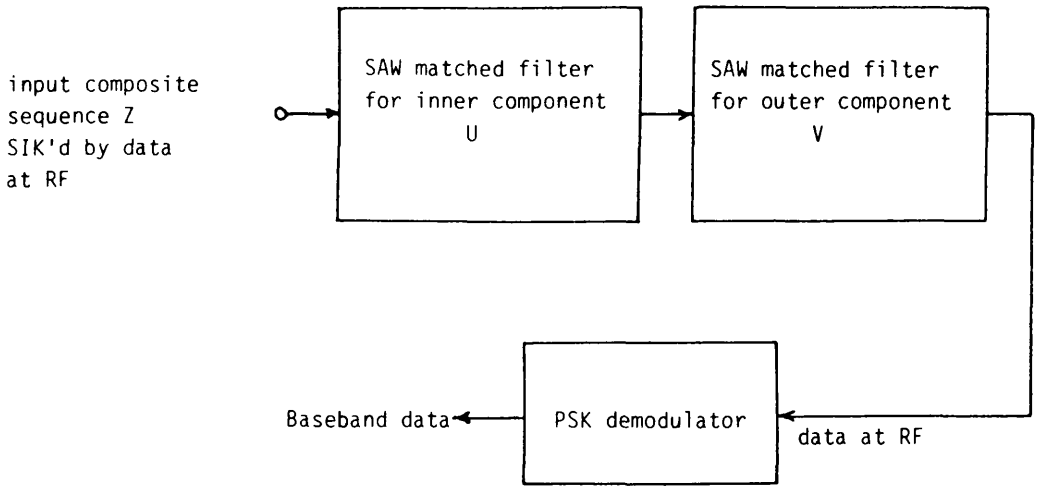
Consider a composite sequence Z constructed from an inner component sequence U of period n_u and an outer component sequence V of period n_v. The chip-rate of the composite sequence rate is the same as that of the inner component sequence rate, and let it be denoted by $1/T_u$ chips per second. The outer component rate is then

equal to $1/n_v T_u$ chips per second. The overall period, n_z, of the composite sequence Z is equal to, $n_u n_v$, chips.

Figure 5.18(a) shows a block diagram of a suggested technique by Beale [23], used to receive a composite sequence. It consists of two cascaded matched filters, one for each of the component sequence. The first one is to synchronise the inner component sequence, while the second one is to synchronise the outer component sequence. In this way, the restriction of using one matched filter for a conventional long sequence is overcome. More importantly, the acquisition time is reduced considerably. This could be explained and understood easily in the following numerical example.

Let the inner component sequence period n_u=255 chips, and the outer component sequence period n_v=63 chips. Thus the composite sequence period n_z=16065 chips. Let also the inner component sequence rate $1/T_u$=150 MHz or T_u=6.667 ns (which is equal to the chip-rate of the composite sequence). So the outer component sequence chip-rate $n_u T_u$=1.7μs. The first matched filter for the inner component U needs to provide a delay of $n_u T_u$=1.7μs with a bandwidth of 150MHz. The second matched filter for the outer component V needs to provide a delay of $n_u n_v T_u$=107μs with a much less bandwidth of $1/n_u T_u$=588 kHz only. Both of these matched filters can be designed using surface acoustic wave devices. But if a single matched filter is used for a conventional sequence of period n_z=16065 and a chip-rate =150MHz, it is required to provide a delay of 107μs over a large bandwidth of 150 MHz, which is beyond the capability of current technology [22].

Charge coupled device (CCD) tapped delay lines can be made to perform matched filtering in the same way as surface acoustic wave



a) SAW matched filter

b) Hybrid SAW/CCD

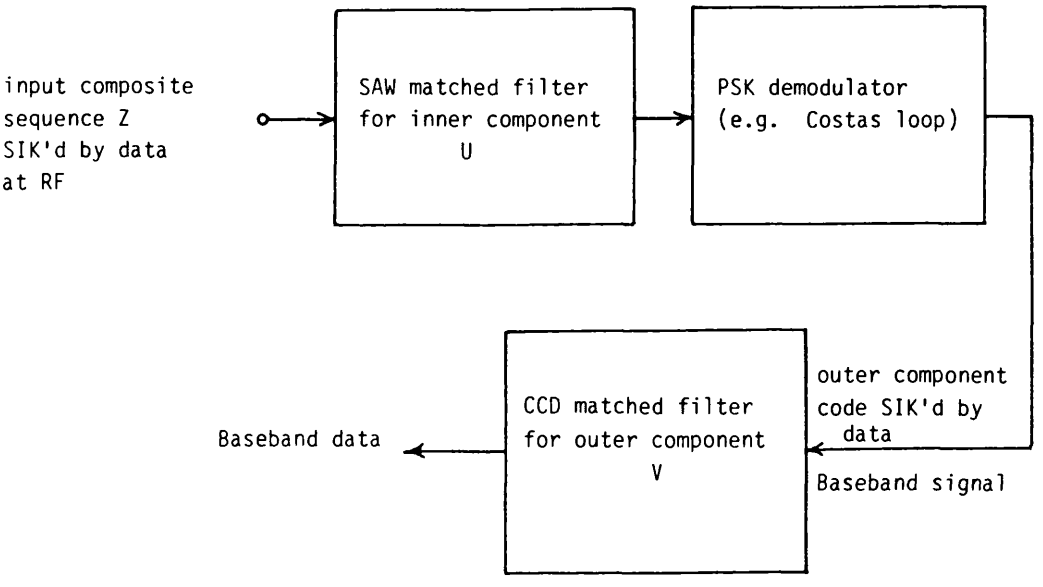


Figure 5.18. Reception of composite sequence using passive correlator [13].

devices except in over different range of time delay and bandwidths. Most practical charge coupled devices are limited to a bandwidth of 10MHz whereas surface acoustic devices can be much wider. But as far as the delay is concerned, the surface acoustic wave devices are limited to about 100 sec delay, whereas charge coupled devices can achieve up to 1 sec. of delay [21]. Therefore, and because the delay and bandwidth associated with the outer component sequence V are long and low respectively, Beale [23] has suggested a possibility of using a charge coupled device as a replacement of the second surface acoustic wave matched filter of Figure 5.18(a). This hybrid form of composite sequence receiver is illustrated in Figure 5.18(b).

As mentioned earlier, the surface acoustic wave matched filter can only work with relatively high input signal to noise ratio. A typical example of -8 dB is given by Baier, Dostert and Pandit [24]. Therefore an alternative technique will be presented in the next section to receive the composite sequence.

5.4.2 Rapid Acquisition Using Active Correlator

Instead of using passive correlators such as surface acoustic wave matched filter with its limited input signal to noise ratio, and short acquisition time, an active correlator will be presented here in order to receive the composite sequence under consideration.

The delay lock loop, which uses active correlators is considered to be a very powerful device to receive a binary spread spectrum signal under very low input signal to noise ratio (down to -30 dB). But its acquisition time becomes long if a long pseudonoise sequence is used. However, the acquisition time of a DLL can be reduced considerably by using a modified version of the delay lock loop as

discussed in Chapter 3. For a 2-Δ delay lock loop of damping factor 0.707, the acquisition time is reduced by a ratio of approximately 2.55, and higher if the damping ratio is also switched.

However, further reductions in acquisition time are possible if the maximal length sequence is replaced by a composite sequence which is constructed from two or more short component sequences. For example, a 32385 bit composite sequence (which is the nearest to 2^{15}-1) can be constructed from 127 and 255 bit maximal length component sequences (2^7-1 and 2^8-1 respectively). If the inner component sequence is chosen to be the 127 bits, that means it is 255 times shorter than the overall composite sequence.

Therefore, if a modified delay lock loop is used to recover, as a first step, the inner component sequence only, followed by rapid recovery of the outer component sequence, as will be explained shortly, it is possible to recover the whole composite sequence nearly **255x2.55≈650 times faster** than a conventional sequence of the same length using the conventional delay lock loop only, and, also gaining its advantage of very low input signal to noise ratio capability.

Figure 5.19 shows a block diagram of the proposed receiver to receive the composite sequence. The first part is a modified delay lock loop which locks and tracks the inner component sequence U of period n_u. The phase inversions of this code due to the outer code are removed in the same way as removing data in a conventional data modulated spread spectrum system. Once synchronisation is achieved, and due to the high process gain G_p of the delay lock (where G_p = bit rate of U/bit rate of B, which gives G_p times higher output signal to

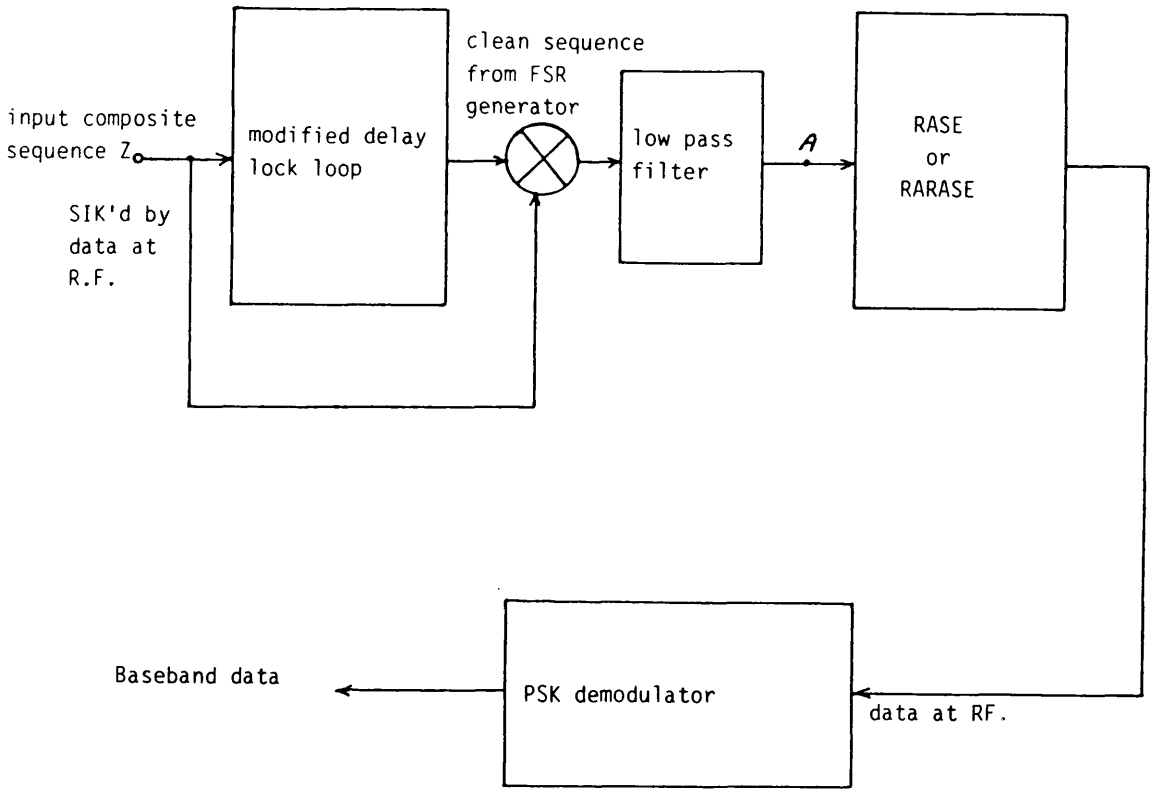


Figure 5.19. Reception of composite sequence using active correlator.

noise ratio than the input signal to noise ratio) the output signal, at point (A) in Figure 5.19, is now much cleaner because of the improvement in signal to noise ratio due to the high process gain G_p, and contains the bits of the outer component sequence V, which are ready to be loaded into the outer component sequence generator either by RASE (rapid acquisition by sequential estimation [5]) or RARASE (rapid acquisition aided sequential estimation [6]). Those techniques, usually make the estimate of the first n received bits, loads the local sequence generator with that estimate, and from that moment the sequence generator as well as the tracking circuit start functioning. This process takes $n_u T_u$ sec., which is considered a very short time indeed if compared with the acquisition time required by other conventional techniques for such long sequences having poor signal to noise ratio. The tracking will continue if the check of that estimate is positive, which is performed by cross-correlating the input signal and the local code sequence, and no further action is taken. However, if the check is negative which indicates an incorrect estimate was made, a new estimate of the input signal bits should be made, loaded and tracked. This process is continued until the final correct estimate is obtained.

It may seem, at the first instant, that this process takes time, and indeed it may do so if the signal to noise ratio at point A is poor. But obviously it is not, since the input to either of these techniques at point A has in fact a relatively good signal to noise ratio due to the existence of the modified delay lock loop which has a high process gain. Ward [5,6] stated that in the absence of noise, the optimum acquisition technique is simply to load the first n received bits into the receiver sequence generator and let the

generator start from that initial condition. It will then continue to produce a sequence which is approximately in-phase with the incoming sequence. Generally, the acquisition of pseudo-noise signal by sequential estimation is an effective method, particularly suitable for use in medium signal to noise ratio condition. Ward [5], has shown that the average acquisition time of 74 ms has been obtained experimentally for a -10 dB signal to noise ratio using a pseudonoise signal of length $2^{15}-1$ bits clocked at 1.5 M bit s^{-1}, which is the same length as that of the composite sequence taken in our example above.

As an example, consider the mean time to acquire lock for a composite sequence comprising two component maximal sequences of length (2^n-1) and (2^m-1).

Let the delay lock loop acquire lock for the inner component sequence of length $L=2^m-1$ and the RASE sequential estimator acquire lock for the outer component sequence of length $R=2^n-1$.

Let the inner sequence be clocked at some rate f_s and let this be the rate of the incoming (i.e. received) sequence. The IF bandwidth of the loop must be $2f_s$. However, the delay lock loop acquires the high speed inner code, and the mixer after the delay lock loop removes the inner sequence from the received signal. Thus, the low pass filter after the delay lock loop can be set to a value which allows through only the slow outer sequence.

The ratio of the IF bandwidth to the RASE bandwidth is just L, the length of the inner code. In other words the RASE system makes estimates on relatively clean outer sequences.

When choosing which is to be the inner and outer sequence there is obviously a trade off to be made. This is between (a) acquiring a

long inner sequence on a delay lock loop, which gives a short and relatively clean sequence to the RASE estimator; or (b) a shorter inner sequence on the delay lock loop, with a longer, less clean signal to the RASE system.

The choice depends on the time required to make the estimate of each bit and the time taken for a delay lock loop to perform a serial search when the received signal is corrupted by noise.

Let m=8, n=7 and f_s=1.5M bit s^{-1}

This is approximately equal to a maximal sequence of length 2^{15}-1 bits.

Once the delay lock has acquired the inner sequence let us assume that it must stay in lock for 1 hour. At a clock rate of 1.5M $bits^{-1}$ this corresponds to an error once every $5x10^9$ bits through the loop.

The possibility of a loss of lock occurs because of additive noise in the received composite sequence which jitters the local code relative to the received code. If the input noise is white Gaussian noise then the phase jitter has Gaussian statistics as well - if the loop is assumed linear. If the jitter exceeds Δ for a 2-Δ loop there is no delay information to pull the loop back and slippage may occur. Although a somewhat naive view, nevertheless, it is sufficiently accurate to give estimates of the probability of loss of lock.

The normalised standard deviation, $\left[\frac{\sigma}{\Delta}\right]$, of the rms phase jitter which will give a probability that the phase error $P(\varepsilon > \Delta) < 2 \times 10^{-10}$ is found to be $\left[\frac{\sigma}{\Delta}\right] = 0.1716$ for wideband Gaussian noise. Thus $\left[\frac{\sigma}{\Delta}\right]^2 = 0.0294$.

However, from [17], for the linearised second order loop for $G \rightarrow \infty$ and $\xi = 0.707$

$$\left[\frac{\sigma}{\Delta}\right]^2 = 1.06 \frac{N_o}{P_s} \omega_n \left[\frac{L}{L+I}\right]^2 \qquad 5.25$$

where N_o is the one sided noise spectral density at the input to the loop (assumed Gaussian), P_s is the signal power, ω_n is the natural frequency of the loop and L is the sequence length. $1.06\omega_n$ is simply the noise bandwidth of the loop for $\xi=0.707$, i.e. $B_n=\omega_n\ (1/4\ \xi+\xi)$ (See Chapter 3).

Let the signal bandwidth at the IF be B_{IF}. This will be the delay lock loop bandwidth. Thus the noise bandwidth will be B_{IF} also and the total input noise will be

$$N_T = N_o \times B_{IF}$$

$$\therefore \left[\frac{\sigma}{\Delta}\right]^2 = 1.06\ \frac{N_T\ \omega_n}{P_s\ B_{IF}}\ \left[\frac{L}{L+1}\right]^2 \qquad 5.26$$

This may be rearranged to give the loop bandwidth ($1.06\,\omega_n$) necessary to achieve the required normalised jitter variance in a given input SNR.

$$\omega_n = \left[\frac{\sigma}{\Delta}\right]^2 \frac{P_s\ B_{IF}}{1.06 N_T}\left[\frac{L+1}{L}\right]^2 = \left[\frac{\sigma}{\Delta}\right]^2 \frac{B_{IF}}{1.06}\left[\frac{L+1}{L}\right]^2 \times (SNR)_{IF} \qquad 5.27$$

If B_{IF} = 3.0MHz, and the input SNR at the IF is -30dB then

$$\omega_n = \frac{0.0294 \times 10^{-3} \times 3 \times 10^6 \times 2 \times \pi}{1.06}\left[\frac{256}{255}\right]^2 \qquad 5.28$$

ω_n = 523 rad s^{-1}.

Therefore the maximum search rate which may be employed on the basis of an acceptable probability of loss of lock is

$V_{max} = 2\omega_n$ = 1046 bit s^{-1}

Thus the time taken for the delay lock loop to acquire the inner (255 bit) sequences is:

T_{inner} = 255/1046 seconds

= 0.244 seconds

The SNR improvement at the input to the RASE system will be in the ratio of L=255, therefore the SNR at RASE input is -30 +24 dB = -6dB.

The bit rate of the outer sequence is only

$$\frac{1.5 \times 10^6}{255} = 5882 \text{ bit } s^{-1}$$

and the time taken to load the n bits of the $R=2^n-1$ bit outer sequence will be 1.19 ms. This is approximately the time taken to make an estimate of the code sequence. The search lock strategy may take an additional period of time, but the figure above provides a lower bound.

Let the period over which the n samples are collected and examined be the examination time T_e. From the work of Ward [5], it is found that for a input SNR of -6dB to the RASE system the probability of a correct sequence being predicted is p=0.68.

The mean acquisition time T_a is just $Te/_p n$

$$\text{Thus } T_a = \frac{1.19 \times 10^{-3}}{0.68^7} = 0.017 \text{ seconds}$$

The total acquisition time is thus

0.244 + 0.017 = 0.261 seconds

Even if the estimation time is doubled, it would have a small effect on the total acquisition time, which is dominated by the delay lock loop acquisition time.

Use of RARASE may achieve even shorter acquisition times.

As a comparison consider the inner sequence to be 127 bits and the outer sequence to be 255. Repeating the calculations gives a time to acquisition of the inner loop of:

T_{DL} = 0.12 seconds,

whilst the SNR improvement for the RASE system is now only 21dB and for -30dB input SNR, the SNR at the RASE system input is -9dB.

For this SNR p is 0.63. For this case however T_e is 6.77×10^{-4} seconds because of the higher bit rate in the RASE system.

Thus T_a = 0.027 seconds.

The total acquisition time is

0.12 + 0.027 = 0.147 seconds.

Which is shorter than the previous case for the same input SNR, clock rate and composite sequence length.

Finally, if a delay lock loop is used to acquire a maximal sequence of $2^{15}-1$ bits length, under the same condition of input SNR and clock rate the acquisition time will be:

T_{dL} = 31.3 seconds.

5.5 CONCLUSIONS

In this chapter a thorough explanation of composite or the so called Kronecker sequences have been discussed. Their generation, properties and auto- and cross-correlation function were examined in detail, illustrated by several different types of sequences, such as maximal length sequences and Barker codes. Some of these sequences show very good auto- and cross-correlation properties, while the properties of other sequences are not so good.

Several main points regarding these composite sequences have been predicted, and these points can help the user to choose the appropriate type and length of the inner and outer components of the composite sequence used in a particular spread spectrum system. The power spectral density of some of these composite sequences were also calculated and plotted.

Two methods of synchronisation and tracking of these special sequences have also been considered and it is shown that if a delay lock loop, followed by a RASE sequential estimation technique are used, then the acquisition time can be reduced tremendously, even with a low input signal to noise ratio. This aspect of the work is supported by numerical examples.

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CHAPTER SIX

EFFECT OF NOISE ON THE ACQUISITION OF PHASE SYNCHRONISATION USING A 2Δ DELAY LOCK LOOP

6.1 INTRODUCTION

In Chapter 3 a method of analysing the acquisition of phase synchronisation of both the standard and switched delay lock loops was introduced. The technique was based on the phase-plane acquisition trajectory, and acquisition trajectories of various delay lock loops were given under noise-free conditions. This is not a particularly realistic condition for a DLL operating in a multi-access spread spectrum system, however. In this chapter the method is modified to include the effect of noise, and results are obtained which show how external noise superimposed on the wanted signal affects the probability of initial acquisition of phase synchronisation. In particular, the effect of the initial search rate, $\dot{x}_s$, on the probability of lock is considered as a function of both noise on the discriminator characteristics and phase jitter. The results are then extended to consider the effect that phase noise has on the mean time to loss of lock.

Also, in this chapter are presented some experimental results of the effect of input signal to noise ratio on the maximum initial search rate, for an acceptable probability of acquisition on the first pass. In these experimental results the performance of a delay lock loop with an analogue (i.e. linear multiplier type) correlator is compared with a digital type of loop which uses hard limiters and EX OR gate multipliers. The analogue loop is tested with and without AGC.

In the next section, a review of some of the work on the effect of noise on the correlator perfomance of a delay lock loop is given.

6.2 CROSS-CORRELATOR ANALYSIS

Several authors have considered the effect of noise at the input to a spread-spectrum system on the discriminator characteristics of the delay lock loop mainly from the point of view of in-lock performance.

The delay lock loop can be modelled mathematically as shown in Figure 6.1 [1]. From the figure it can be seen that:

$$\tau_1-\tau_2=\Delta\tau= -\frac{KF(s)/s}{1+AKF(s)/s}\, n(t) \qquad 6.1$$

Working with power spectral densities, equation 6.1 can be written as:

$$S_{\Delta\tau}(f) = \left| \frac{jF(j\omega)/j\omega}{1+AKF(j\omega)/j\omega} \right|^2 S_n(f) \qquad 6.2$$

where $S_n(f)$ is the power spectral density of the noise, and $S_{\Delta\tau}(f)$ is the power spectral density of the loop tracking error. Figure 6.2 shows the cross-correlator network of a delay lock loop. It will be seen that the equivalent noise, n(t), for this model is related to the actual input noise by:

$$n(t) = n_i(t)[a(t-\tau_d)-a(t+\tau_d)] \qquad 6.3$$

where $n_i(t)$ is the actual input noise filtered by the receiver filter.

$a(t-\tau_d)$ is the reference PN code delay by τ_d bits

$a(t+\tau_d)$ is the reference PN code advanced by τ_d bits

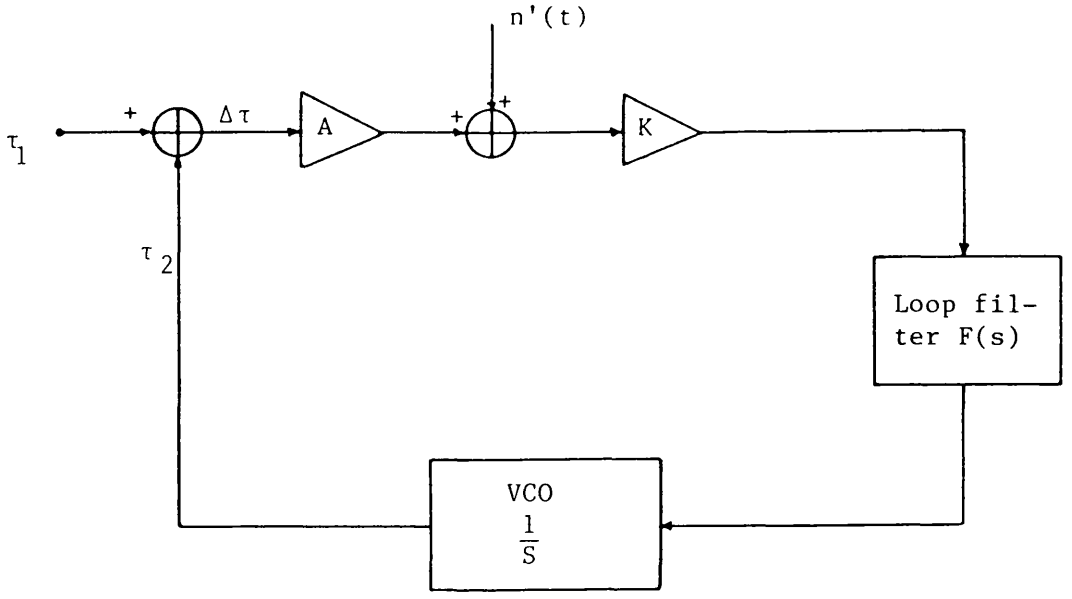


Figure 6.1 Mathematical model of delay lock loop.

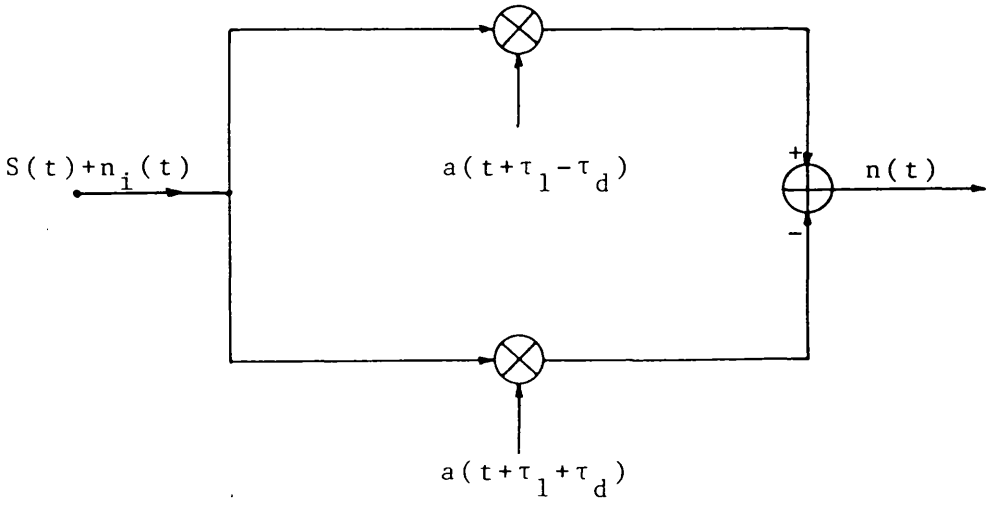


Figure 6.2. Delay lock loop correlator network (error discriminator).

Note this assumes that any time delays in each arm are equal and that the noise appearing at the two difference amplifier inputs is 100% correlated.

Denoting, A(f) as the power spectrum of the reference PN code with zero delay and $S_{n_i}(f)$ as the power spectrum density function of the received white Gaussian noise of value N_o watts/Hz, but limited to f_R Hz, the low pass equivalent bandwidth of the receiver filter. Thus the power spectral density of the equivalent noise at the output is given by:

$$N_{o_{(out)}} = N_o \int_o^{f_R} A(f)\left[2 - e^{-j\omega 2\tau_d} - e^{j\omega 2\tau_d}\right]df$$

$$= 2N_o\left[R(0)_{BL} - R(2\tau_d)_{BL}\right] \qquad 6.4$$

where $R(x)_{BL}$ is the bandlimited autocorrelation function of the PN code evaluated for a relative time delay of x seconds.

Thus equation 6.2 can now be written as:

$$S_{\Delta\tau}(f) = \frac{|H(j\omega)|^2}{A^2} 2N_o[R(0)_{BL} - R(2\tau_d)_{BL}] \qquad 6.5$$

where $H(j\omega)$ is the closed loop transfer function and A is now the error signal gain shown in the mathematical model. It is seen, [2], that A must:

a) convert a time displacement, $\Delta\tau$, between the incoming code and the reference code to an error voltage.

b) be solely a function of signal and not noise; i.e. is really the loop discriminator function.

c) have an output which is proportional to the signal level, $\sqrt{S}$

d) have a transfer function given by the slope of the discriminator characteristic.

Thus, based on the above considerations:

$$A = \sqrt{S}\,\frac{d}{d\tau_1}\,\langle a(t+\tau_1)a(t-\tau_2-\tau_d) - a(t+\tau_1)a(t+\tau_2+\tau_d)\rangle_{\Delta\tau=0} \qquad 6.6$$

$$= 2\sqrt{S}\,R'(\tau_d)_{BL} \qquad 6.7$$

where $\langle x \rangle$ is the time average value of x

and S is the signal power.

Consequently the variance of $S_{\Delta\tau}$ is:

$$\sigma^2_{\Delta\tau} = \int_0^\infty S_{\Delta\tau}(f)\,df$$

$$= \frac{2N_o}{S}\,\frac{R(0)_{BL} - R(2\tau_d)_{BL}}{[2R'(\tau_d)_{BL}]^2}\int_0^\infty |H(j\omega)|^2\,\frac{d\omega}{2\pi} \qquad 6.8$$

Defining the noise bandwidth of the loop as:

$$B_n = \int_0^\infty |H(j\omega)|^2\,\frac{d\omega}{2\pi} \qquad 6.9$$

equation 6.8 reduces to

$$\sigma_{\Delta\tau} = \frac{1}{\sqrt{\frac{S}{2N_o B_n}}} \times \frac{\sqrt{R(0)_{BL} - R(2\tau_d)_{BL}}}{2R'(\tau_d)_{BL}} \qquad 6.10$$

where B_n is the one sided loop noise bandwidth - which for the second order DLL is $B_n = \omega_n(\frac{1}{4\xi} + \xi)$

where ξ is the damping ratio

N_o is the one sided noise power density.

and S is the average signal power.

Cahn [2], has plotted the auto-correlation function and the slope of the auto-correlation function for different amounts of bandlimiting (i.e. as a function of the receiver cut off frequency f_R). He defines a bandlimiting parameter B which relates the rf cut off frequency f_R to the chip rate of the PN code, T_c, via: $B=2\pi f_R T_c$. This is shown in Figures 6.3 and 6.4 respectively. It is clear that when B is very large the correlation function is the ideal triangular shape, but as B is reduced to π the r.f. filtering considerably broadens, and reduces, the amplitude of the correlation function betweeen the received and locally generated replica sequence. As might be expected, this has an effect on the effective "process gain" of the delay lock loop, albeit by only 1dB.

From equation 6.10 the rms tracking error can be plotted as a function of $S/N_o B_n$ and also as a function of the bandlimiting parameter B and for different values of delay offset τ_d. This is

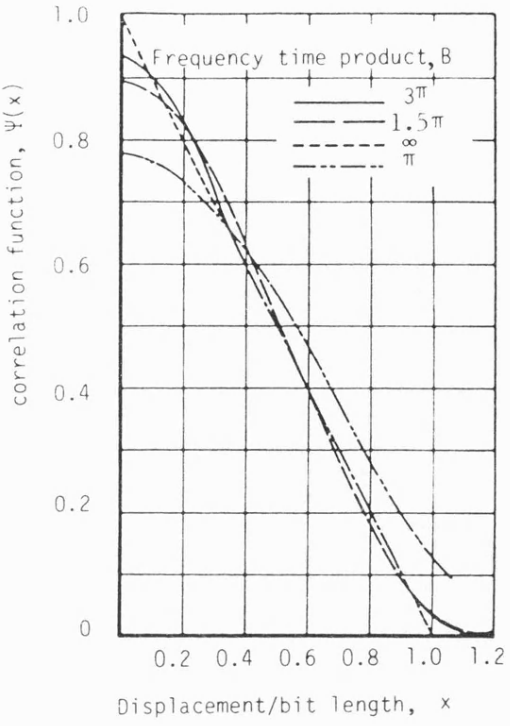


Figure 6.3 Correlation function Ψ(x) [2]

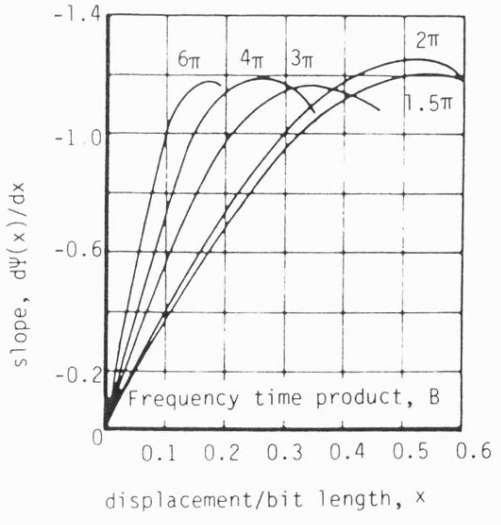


Figure 6.4 Slope of correlation function Ψ(x), [2].

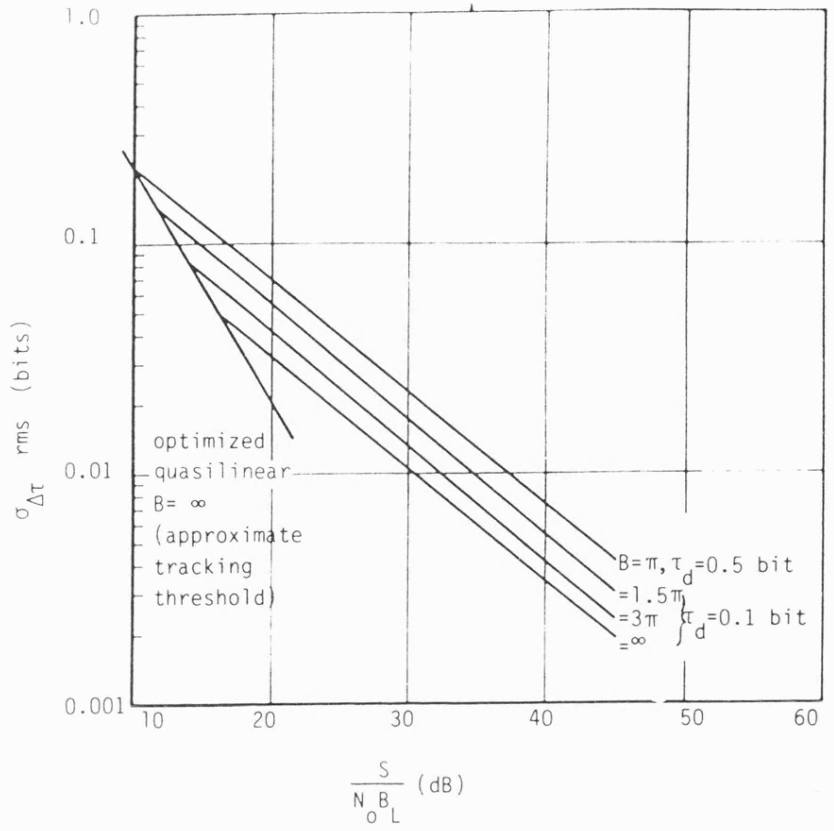


Figure 6.5 RMS tracking error verus loop SNR [2]

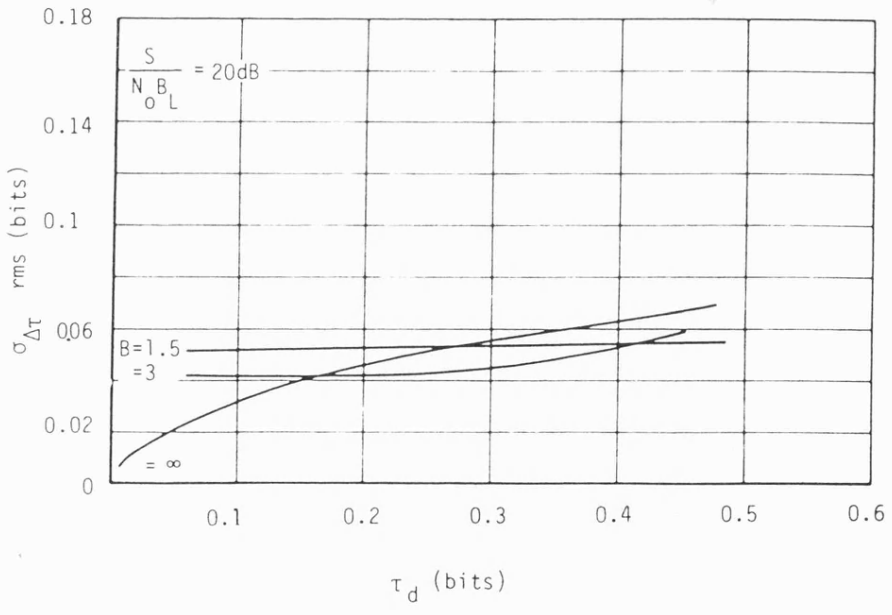


Figure 6.6. RMS tracking error as a function of displacement τ_d [2].

shown in Figure 6.5 and 6.6 respectively. It is interesting to note that for typical values of the bandlimiting factor B of about 1.5π, $\sigma_{\Delta\tau}$ changes very little as a function of the relative phase delay τ_d, but, as might be expected the rms tracking error is proportional to $^{-1}/\sqrt{SNR_i}$ over a wide range of input signal to noise ratios. However, at relatively low input SNR's a threshold effect occurs where $\sigma_{\Delta\tau}$ is proportional to $-(SNR_i)$.

From this brief introduction, the analysis by Cahn can be used in the development of a computer model to examine the effect of external noise on the initial acquisition of phase sychronisation. In particular, the results shown in figures 6.3 and 6.6 enable simplifications to be made to the model, which reduce computation time.

6.3 COMPUTER SIMULATION OF INITIAL ACQUISITION OF LOCK IN NOISY CONDITIONS

The analysis by Cahn [2] in the previous section showed that even when the noise in the two arms of the correlator is strongly correlated (i.e. the gains and propagation delays in each arm are perfectly matched) the fact that the noise is added to a band limited PN sequence and correlated against a perfect (i.e. not bandlimited) replica sequence, results in a net noise output being fed to the VCO. In practice however arm gain-imbalance and particularly differing group delay in the bandpass filters in each arm of an IF delay lock loop will ensure that the noise in each arm of the delay lock loop will not be correlated, and so a higher noise variance on the control signal to the VCO of the loop can be expected than be predicted by equation 6.8.

As might be expected from a simple physical understanding of the correlator, the results of Cahn's analysis shown in Figure 6.6 suggest that the noise variance is virtually independent of the relative phase delay between the two sequences. This enables one to propose a relatively simple computer algorithm for modelling code acquisition, which includes adding a random perturbation of known and constant standard deviation onto the discriminator charactersitics, which represents the error signal controlling the VCO of the loop. Thus for any relative delay between the sequences the noise perturbation on the error signal will also have the same standard deviation.

However, the acquisition of lock is very sensitive to the initial search rate, and it has been seen in Chapter 3 that if the value of $\dot{x}$ at x=0 in the upper quadrants of the phase-plane plot exceeds a critical value acquisition of lock will not be achieved. When noise is present on the error signal two main reasons for the loop acquiring and maintaining lock can be identified. Non acquisition of initial phase synchronisation occurs because:

(a) The noise voltage on the error signal causes the loop to FM or "accelerate" and "decelerate" during acquisition. This has an effect on the actual trajectory taken during acquisition and it is possible that the trajectory can be forced outside the maximum permitted trajectory from which lock can be achieved in noiseless conditions. This is illustrated in Figure 6.7. Clearly the noise can also pull back the trajectory to within the maximum trajectory normally allowed to guarantee lock. Thus the noise only really plays a critical role when the trajectory is in the upper RH quadrant of the phase plane

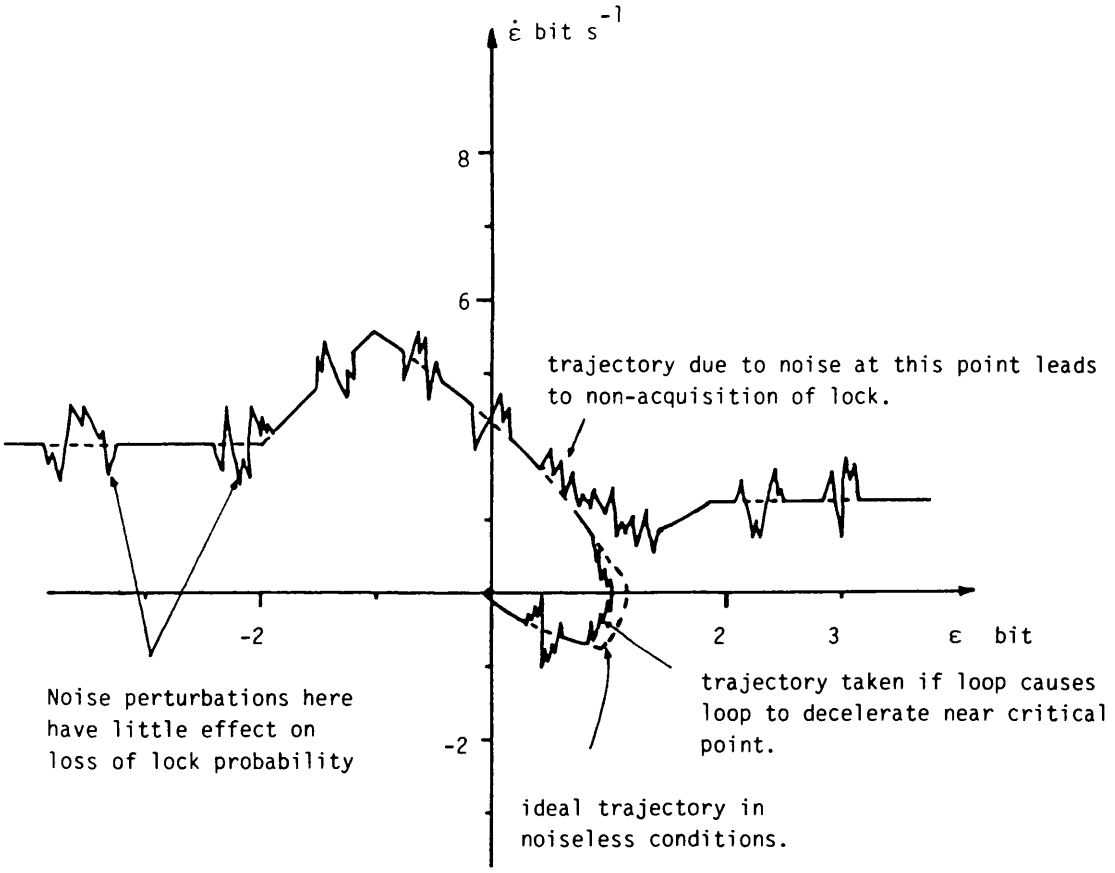


Figure 6.7. Illustrative diagram showing how noise may affect likelihood of acquiring lock.

and is about to cross the x axis into the lower RH quadrant, as illustrated in Figure 6.7. Clearly the greater the noise variance the greater the probability that the trajectory will be forced outside the maximum allowed trajectory.

b) The noise causes the VCO to FM and this causes a phase deviation between the two sequences. This may be so large that the loop has a very high probability of losing lock immediately after it has been acquired.

Essentially, these are two quite separate effects and the model presented in this chapter illustrates the importance of each effect.

6.3.1 The Model

The model is virtually identical to that used in chapter 3. It will be recalled that this is based on the phase-plane acquisition trajectory equation 3.12, and uses a Runge-Kutta-Merson numerical computation method to plot the trajectory for a given set of initial value conditions. The technique also requires knowledge of the discriminator characteristics.

In this new model the effect of the external noise is added to the signal from the discriminator during computation of the trajectory. This is done by adding a random signal of known standard deviation to the discriminator characteristics D(x) at each point of the trajectory and calculating $\dot{D}(x)$ from this, and the previous value, D(x-1). In this way the effect of phase jitter between the sequences can be removed, and this enables the effect of amplitude fluctuations on the probability of acquiring initial lock to be made.

This condition also represents the case where the loops may have a relatively high gain, but the VCO has a very low gain.

However, in the model it is also possible to add a random jitter to the locally generated sequence during computation of the phase-plane trajectory. To do this, essentially a different random sequence to that used to generate amplitude perturbations is applied to control the step number of the algorithm. The step number dictates the relative phase between the two sequences, and so the local code can be advanced or retarded relative to the incoming sequence. The standard deviation of this jitter can be controlled entirely separately from the amplitude jitter.

When using the random number generator on the computer care was taken to randomise the kernal of the RND function.

In the simulation, varying degrees of both amplitude and phase jitter were applied to the loop for a wide range of initial search velocities between the two sequences; and for each point of the graph **at least** 400 trials were carried out to see if the loop could achieve and maintain phase synchronisation. For poor SNR conditions and at critical parts of the characteristics where the probability of acquisition fell rapidly, over 1000 trials were carried out on each point of the graph. The loop was deemed to be in lock when the trajectory returned to zero (i.e. $x=0$, $\dot{x}=0$) and had remained in lock for the remainder of the steps used to obtain the trajectory. (Normally 1000 steps were used in the calculation of the trajectory, of which between 400 and 600 were actually needed to define the bulk of the trajectory and the remainder were used to determine the fine-settling of an essentially in-lock loop.)

From all these trials for a particular initial search rate, amplitude jitter on the discriminator characteristics and phase jitter the probability of acquiring and maintaining lock could be obtained for probabilities of lock as low as 1 in 10^3.

The in-lock performance of the loop could also be simulated using a similar technique. Here the loop was allowed to acquire lock in the normal way, in noiseless conditions, and then phase jitter was applied. Here the "time" taken for the loop to lose lock was obtained in terms of the number of program steps taken before loss of lock occurred. As above, over 100 trials were taken to obtain the mean "time" to loss of lock for each point.

In a practical spread-spectrum system, the parameter of greatest interest when specifying the noise behaviour is the noise at the input to the receiver.

However, because of the effect of bandlimiting and arm gain-imbalance etc. it is difficult to quantify the noise level at the delay lock loop correlator output with the signal to noise ratio at the input to the loop, or at the input of the receiver. Under ideal conditions, the variance of the noise at the correlator output can be related to the input noise spectral density using equation 6.8. In this simulation, an ideal triangular correlation function is assumed between the received and replica code, normalised to a peak amplitude of 1. The effective output power from the correlator is thus also $1V^2$. The noise levels quoted are the noise levels at the **output** of the correlator **not** at the receiver input. These values of signal and noise may be related back to an equivalent input SNR using equation 6.8 or 6.10 if desired. The SNR at the correlator output is quoted

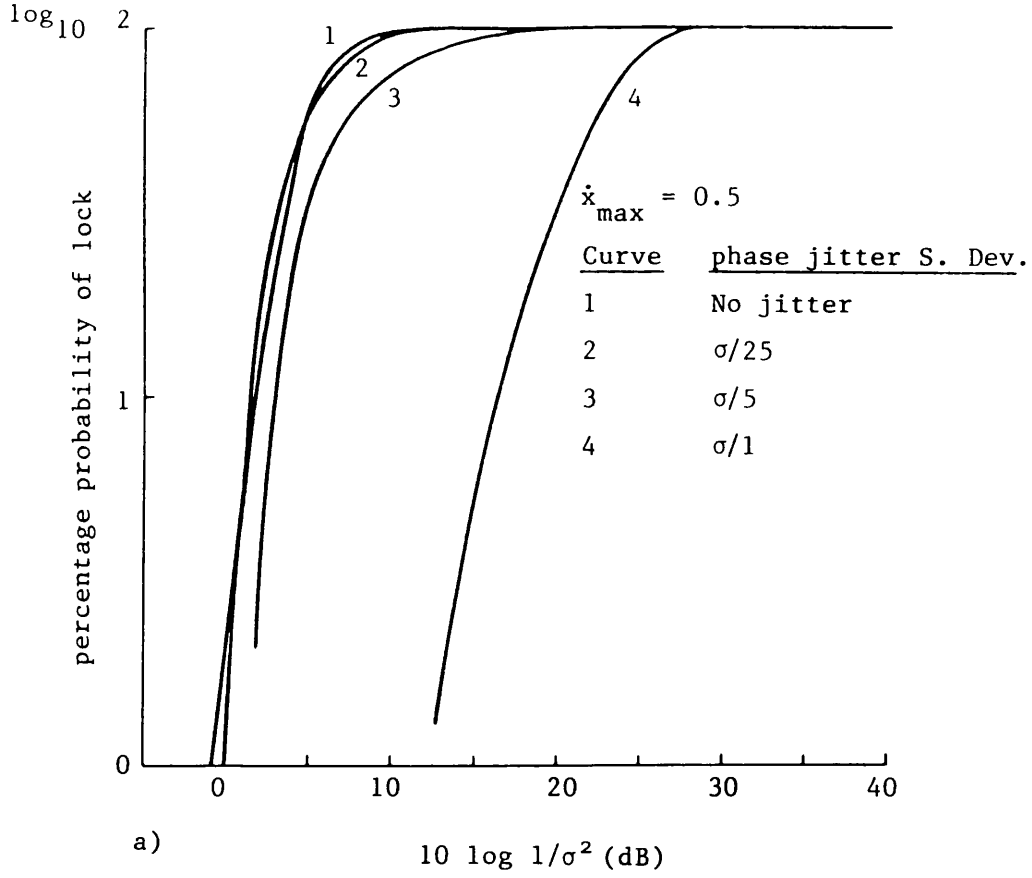
in terms of a power ratio, $SNR_c = 1/\sigma^2$, and hence the dB scale is calculate on the basis of $10 \log_{10} (1/\sigma^2)$.

Because of the computation required to achieve reliable points on the characteristics the results have been obtained only for the standard 2Δ delay lock loop, and it is assumed that the loop natural frequency, $\omega_n = 1$ rads^{-1}, $\xi = 0.707$ and the loop gain $G=\infty$.

6.3.2 Results of the Computer Simulation

In this section the probability of acquiring and maintaing phase lock is plotted against the variance of the amplitude noise on the discriminator characteristics, measured at the correlator output. The results are plotted in Figure 6.8 for different values of initial search rate, $\dot{x}_s$, and for different degrees of phase jitter between te two codes. Figure 6.8a shows how the probability of acquiring lock is reduced as the correlator SNR is reduced, for an initial search rate of $x_s = 0.5$ bit s^{-1}, and for different values of phase jitter. This value of search rate is much less than $\dot{x}_{s\,max} \approx 2.0$ bit s^{-1} obtainable in noiseless conditions for the 2Δ delay lock loop.

For the case of zero phase jitter it is clear that as the signal to noise ratio at the correlator output is decreased the probability of acquiring and maintaining lock remains good until the noise variance is -10dB of the wanted signal. For lower signal to noise ratios the probability of lock falls markedly and at 0 dB SNR the probability of acquiring lock on the first pass is very low. It should be noted that the noise bandwidth of the loop, $B_n = 1.06\,\omega_n$, is usually very much lower than the data rate which is modulating the PN code. As a consequence the signal to noise ratio at the output of



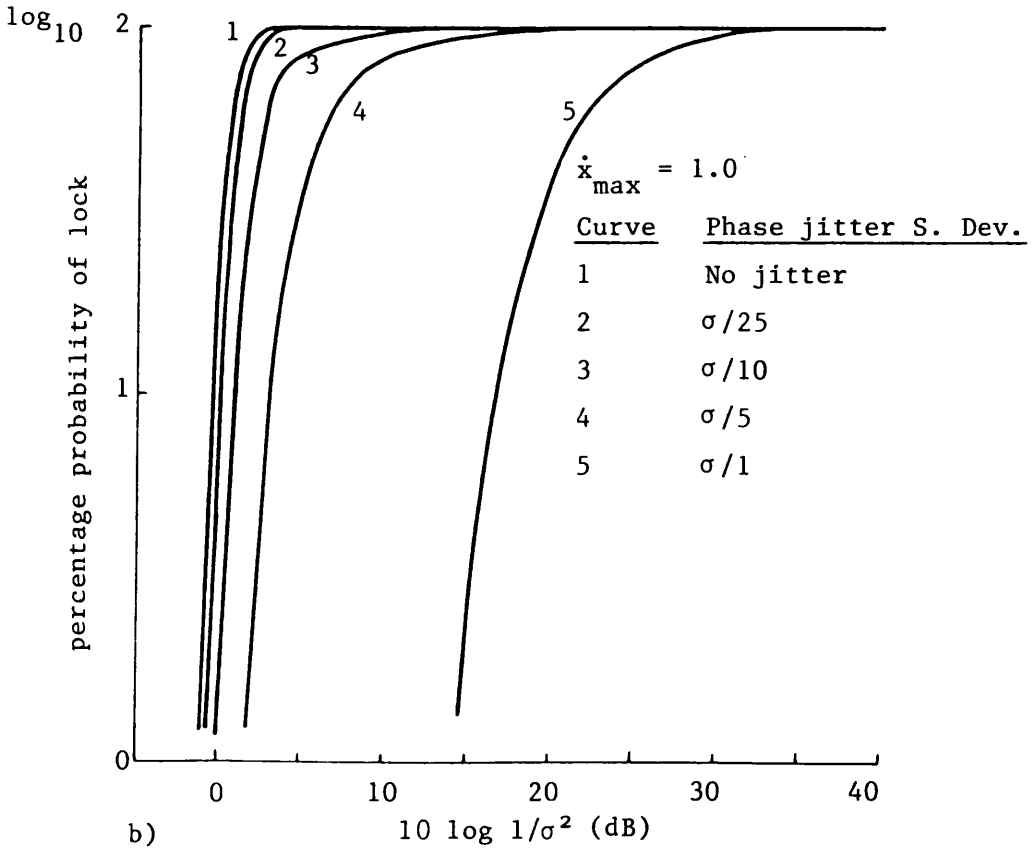
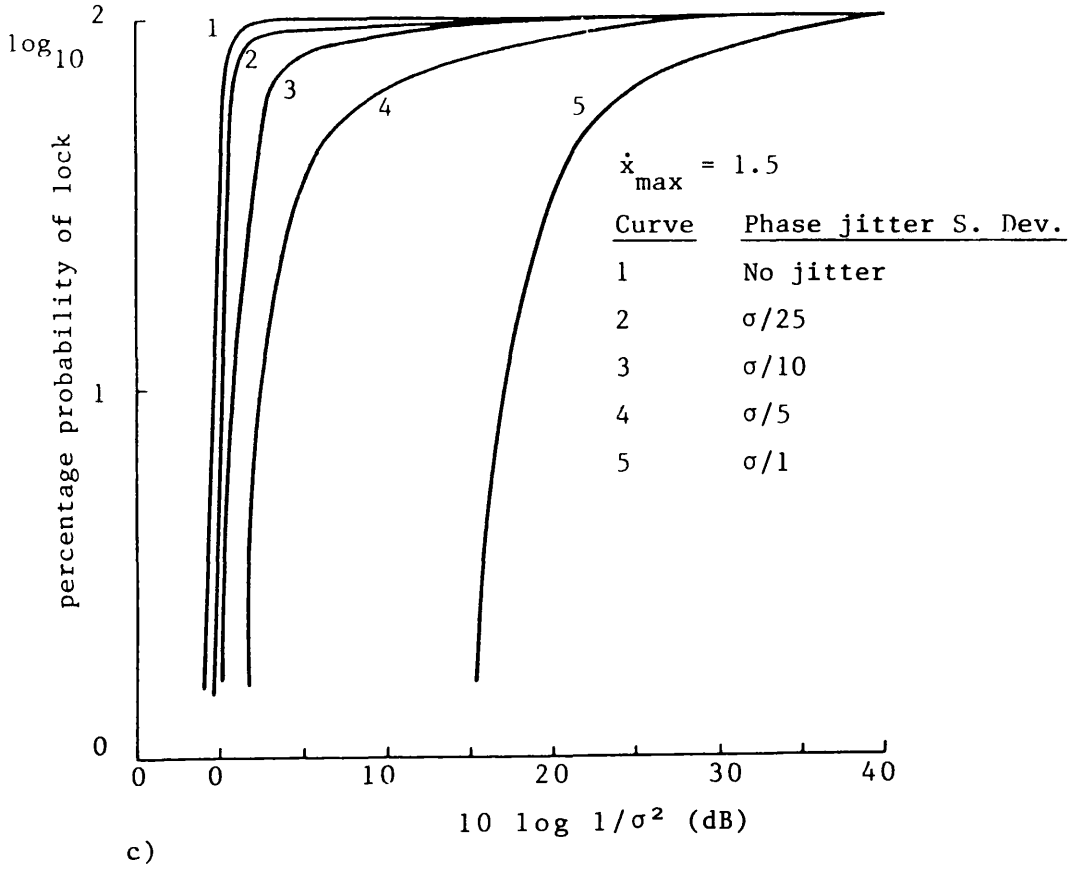
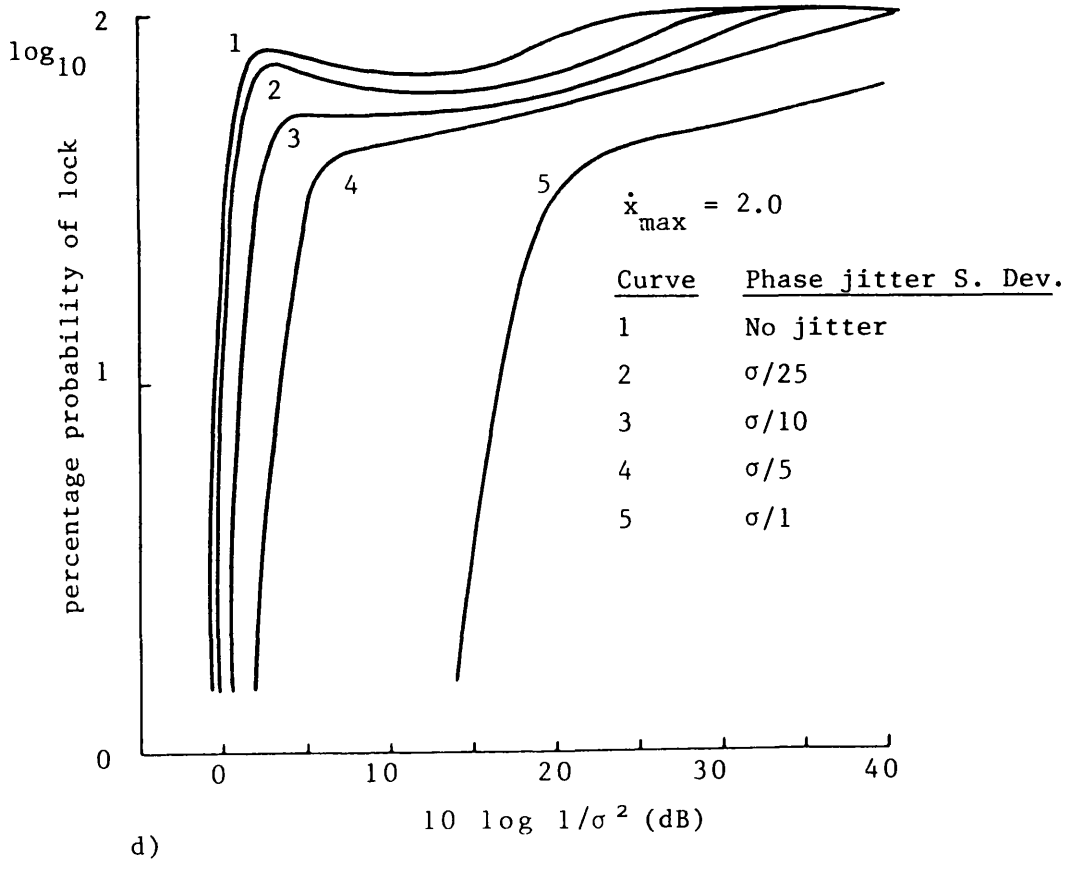


Figure 6.8. Effect on the probability of lock of the noise variance on the discriminator characteristics, for different values of phase jitter.



c)



d)

Figure 6.8 (Continued).

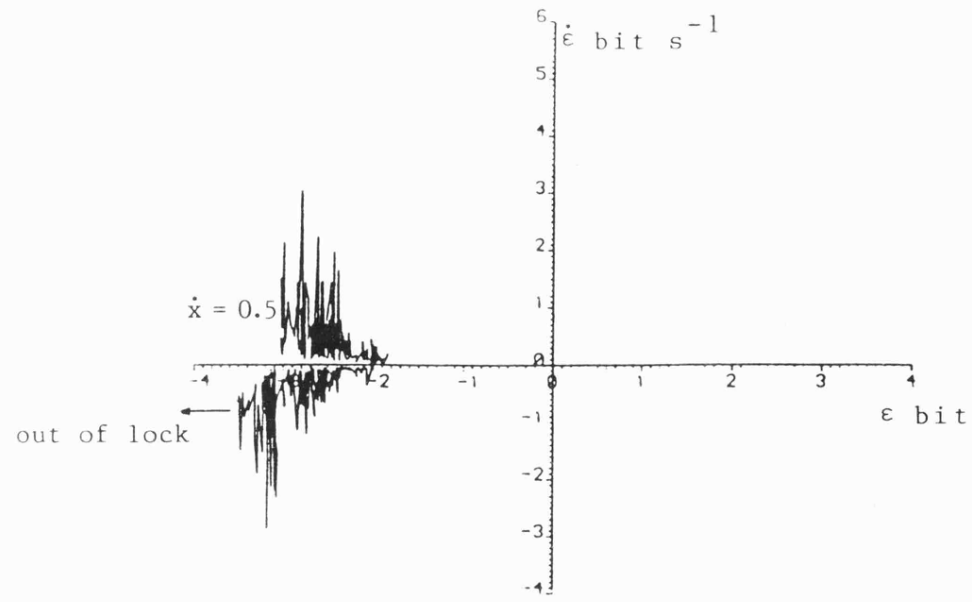
the spread-spectrum data correlator will be worse than that at the VCO input in the ratio B_{DATA}/B_n. Thus, for noise levels at which the probability of acquiring lock on the first pass becomes unacceptable the probability of correctly detecting the data will be vanishably small.

The effect of the phase jitter on the probability of lock is to reduce the value of amplitude jitter on the discriminator characteristic at which the probability starts to fall rapidly.

In figures 6.8b-6.8d the initial search rate is progressively increased. The general shape of the characteristics are the same for each case. However, it will be seen that with zero phase jitter "optimum" performance is obtained when $\dot{x}_s$ = 1.0 bit s^{-1}. This characteristic is optimum in the sense that a very high probability of acquiring lock on the first pass can be maintained down to the lowest correlator SNR.

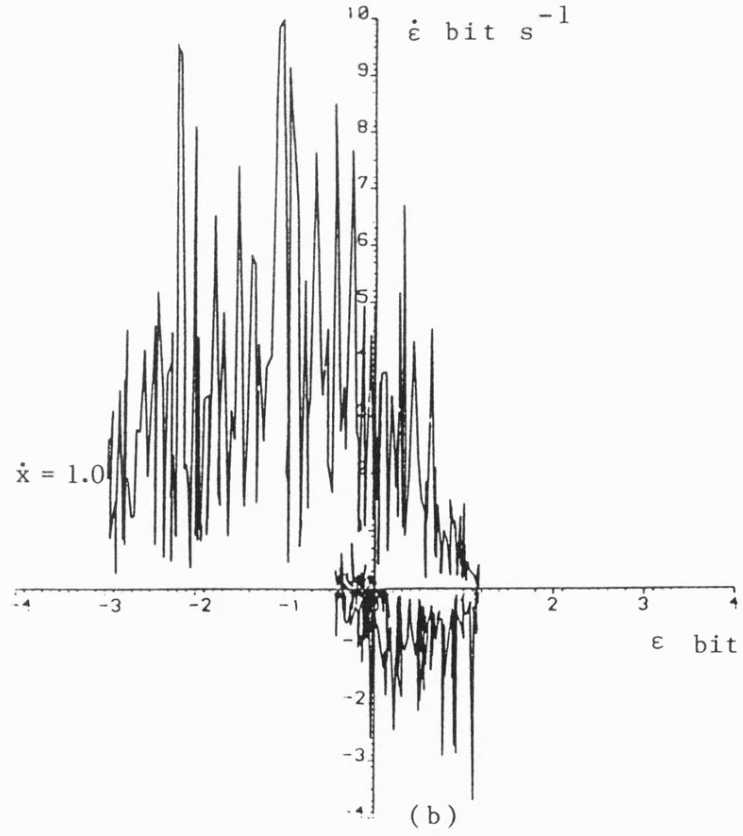
As the search rate is increased, or decreased from this value of $\dot{x}_s$, the correlator SNR must be increased to achieve the same probability of lock. The effect of increased phase jitter affects the characteristics for each search rate in much the same way as described above.

It is interesting to consider why reducing the initial search rate might worsen the probability of acquiring lock. In Chapter 3 it was shown that the area contained by the acquisition trajectory decreases as the initial search rate decreases. This means that the wanted error signal fed to the VCO must be low to achieve the desired search rate, and therefore prone noise signals. Figure 6.9a shows that for $\dot{x}_s$ = 0.5 bit s^{-1} the effect of the noise tends to slow down



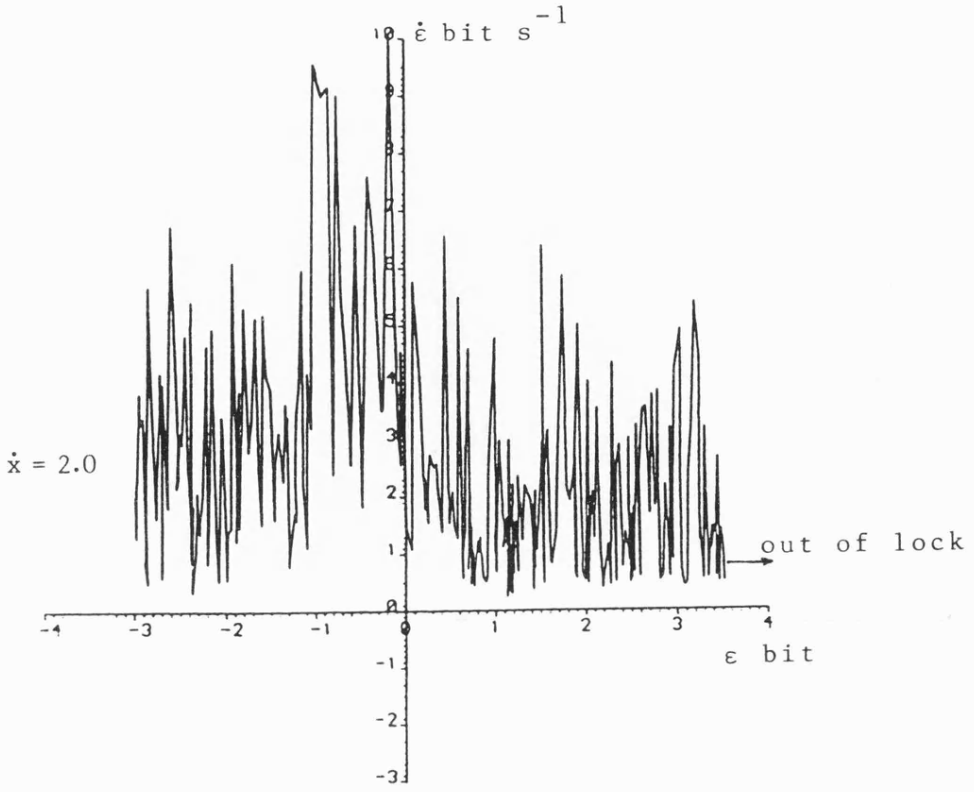
Note - noise reduces probability of initiating search.

(a)



(b)

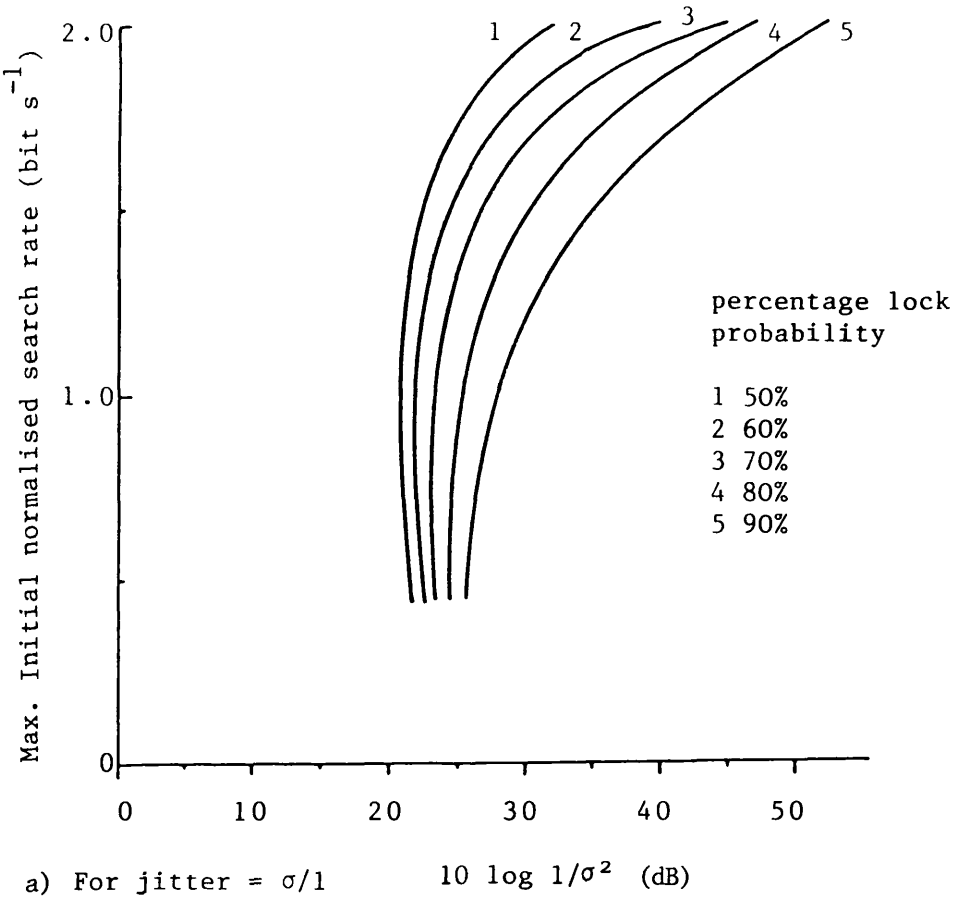
Figure 6.9 Typical acquisition trajectories for a 2Δ DLL, under the same conditions of noise, for 3 different initial search rates (ω_n=1 rad s^{-1}, ξ= 0.707, G =∞, σ= 0.5, J = σ/25).



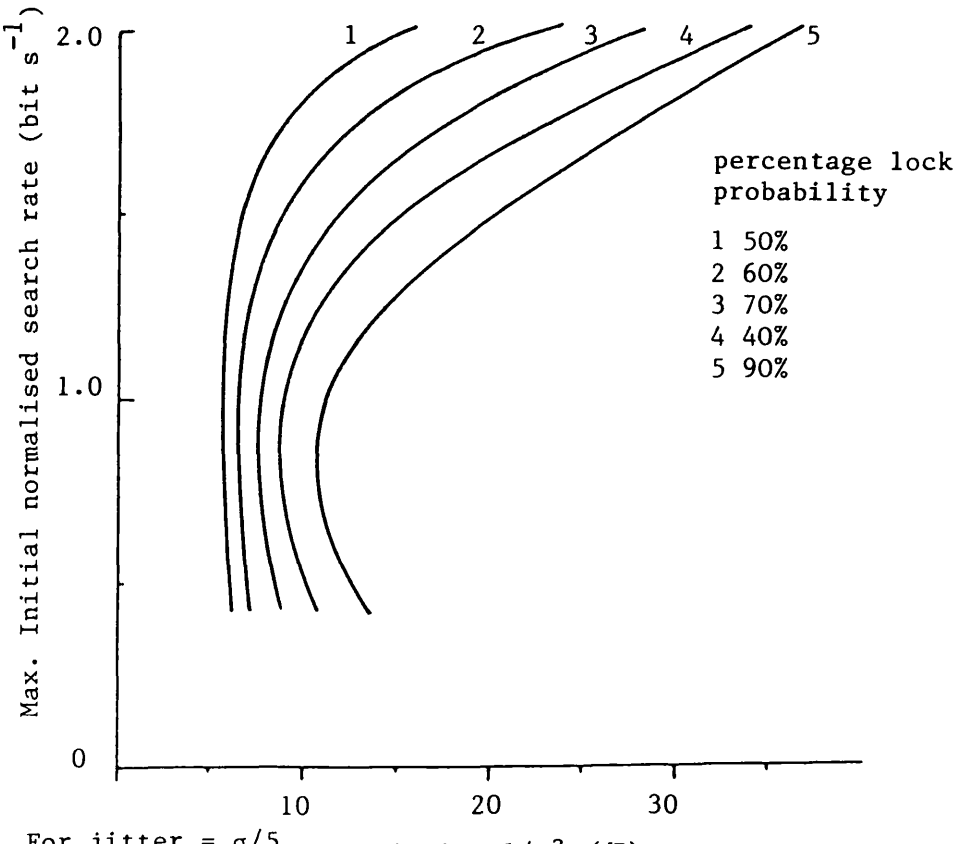
Note - noise prevents final acquisition.

(c)

Figure 6.9 (Continued).



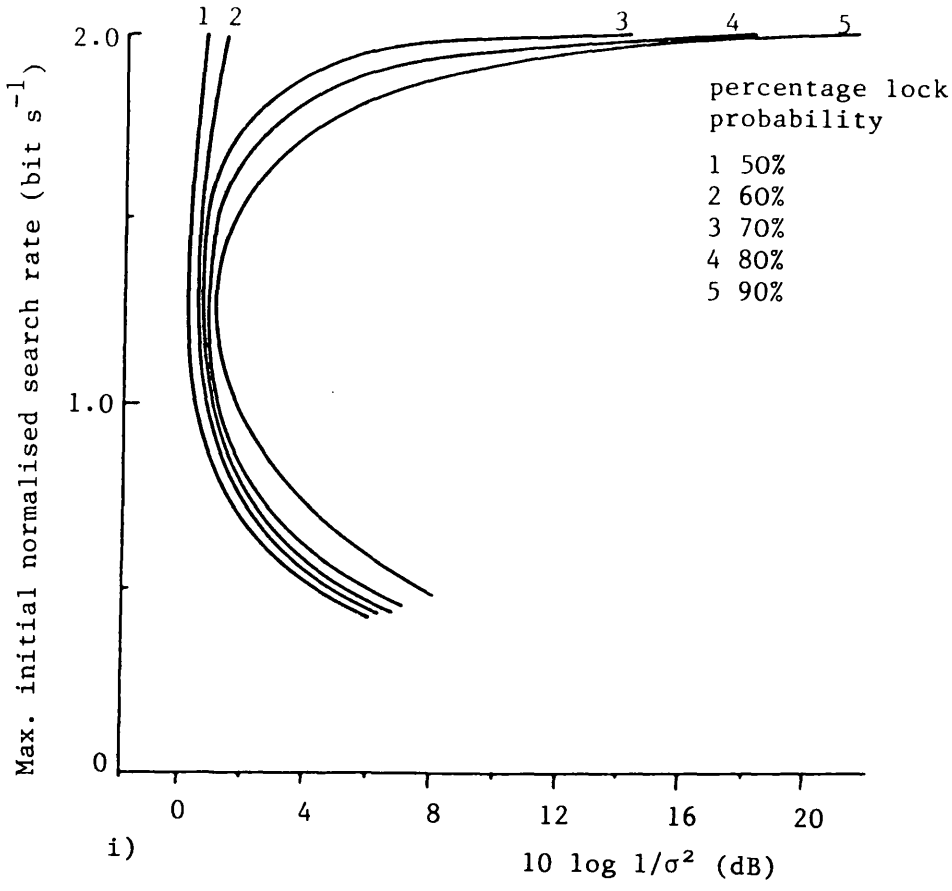
a) For jitter = σ/1



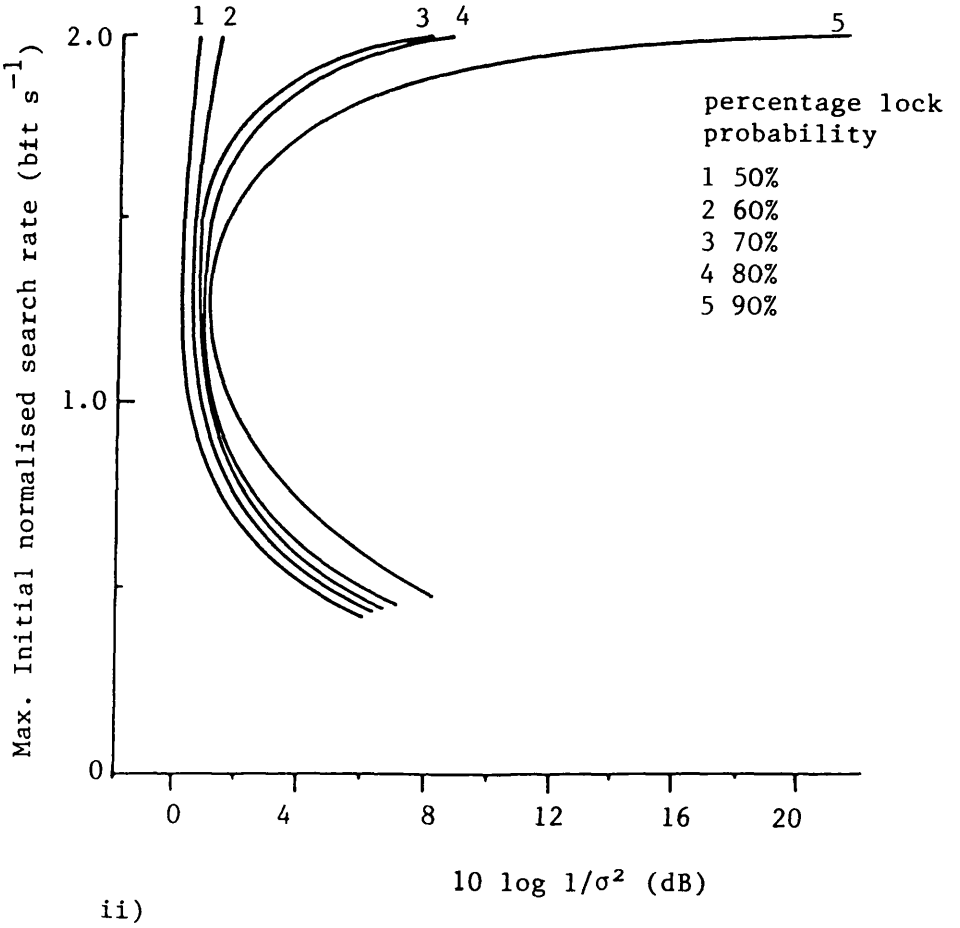
b) For jitter = σ/5

Figure 6.10. Effect of amplitude and phase jitter on the maximum initial search rate to achieve the stated probability of acquiring lock.

c) No Jitter.

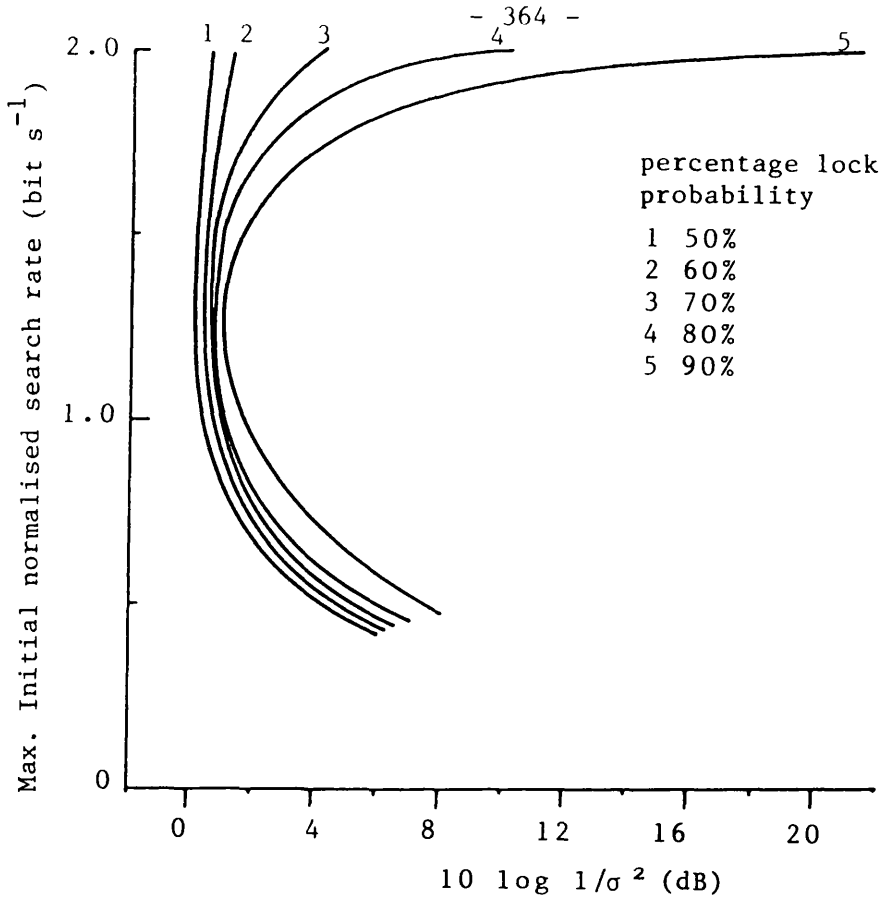


i)



ii)

Figure 6.10 (Continued).



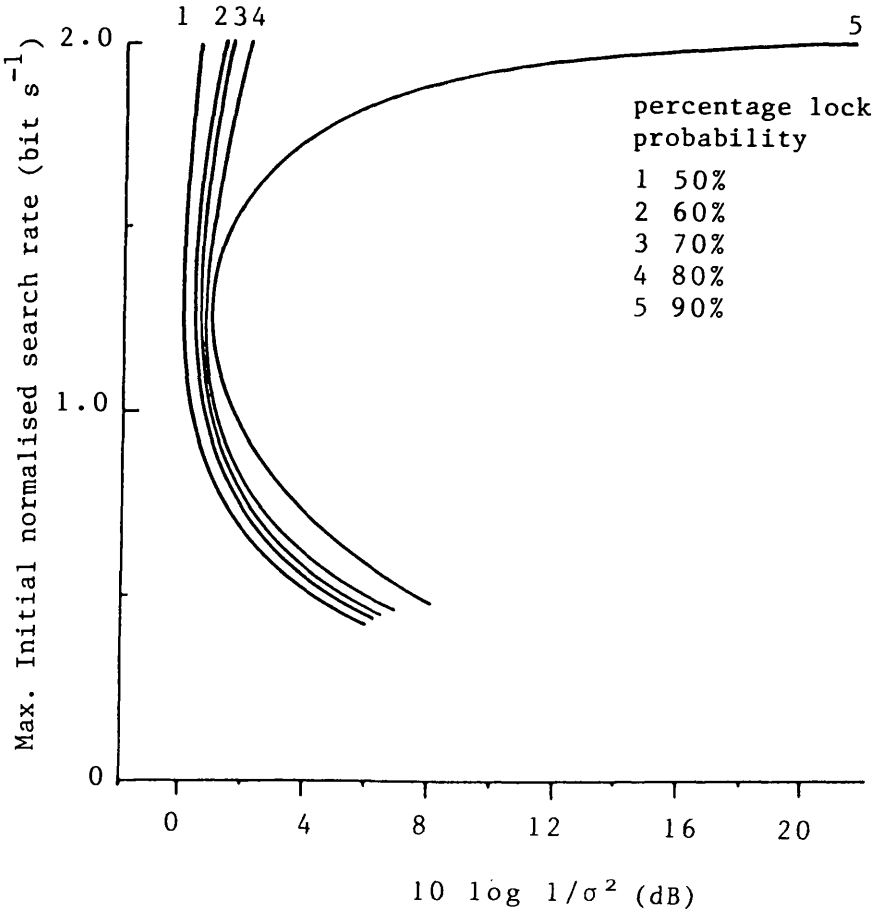


Figure 6.10 (Continued).

and stop the initial search process before coarse synchronisation can be achieved. The search can even reverse direction, as shown. For a higher search rate, say $\dot{x}_s$ = 1.0 bit s^{-1} as shown in Figure 6.9b the trajectory expands, and this reduces the probability that the search process will be stopped before coarse synchronisation is achieved. For search rates close to the maximum, however, typically $\dot{x}_s$=2.0 bit s^{-1}, as shown in Figure 6.9c there is now a greater probability that the noise will force the trajectory outside the maximum allowable in the upper RH quadrant, as discussed earlier, and negligible probability that the search process will be stopped in the upper LH quadrant of the phase-plane trajectory. Noise, therefore affects the three regimes in different ways.

It is instructive to redraw the curves of figure 6.8a-d so that they are expressed as the maximum slip rate vs the signal to noise ratio at the correlator output to achieve a given probability of acquiring lock on the first pass. These characteristics are plotted in figure 6.10 for different values of phase jitter. It will be seen from all these characteristics that if $0.5 < \dot{x}_s < 1.5$ bit s^{-1} the loop acquire lock to the stated probability in the worst correlator SNR conditions. For the case of results with no phase jitter 4 different sets of results had to be produced because of the kink in the characteristics.

6.3.3. Effect of noise on the Mean Time to Loss of Lock

Figure 6.11 shows the effect of correlator output signal to noise ratio on the mean 'time' to loss of lock. In this set of characteristics no phase jitter is assumed to exist, since the loop is now in-lock, and there is a negligible probability of the amplitude

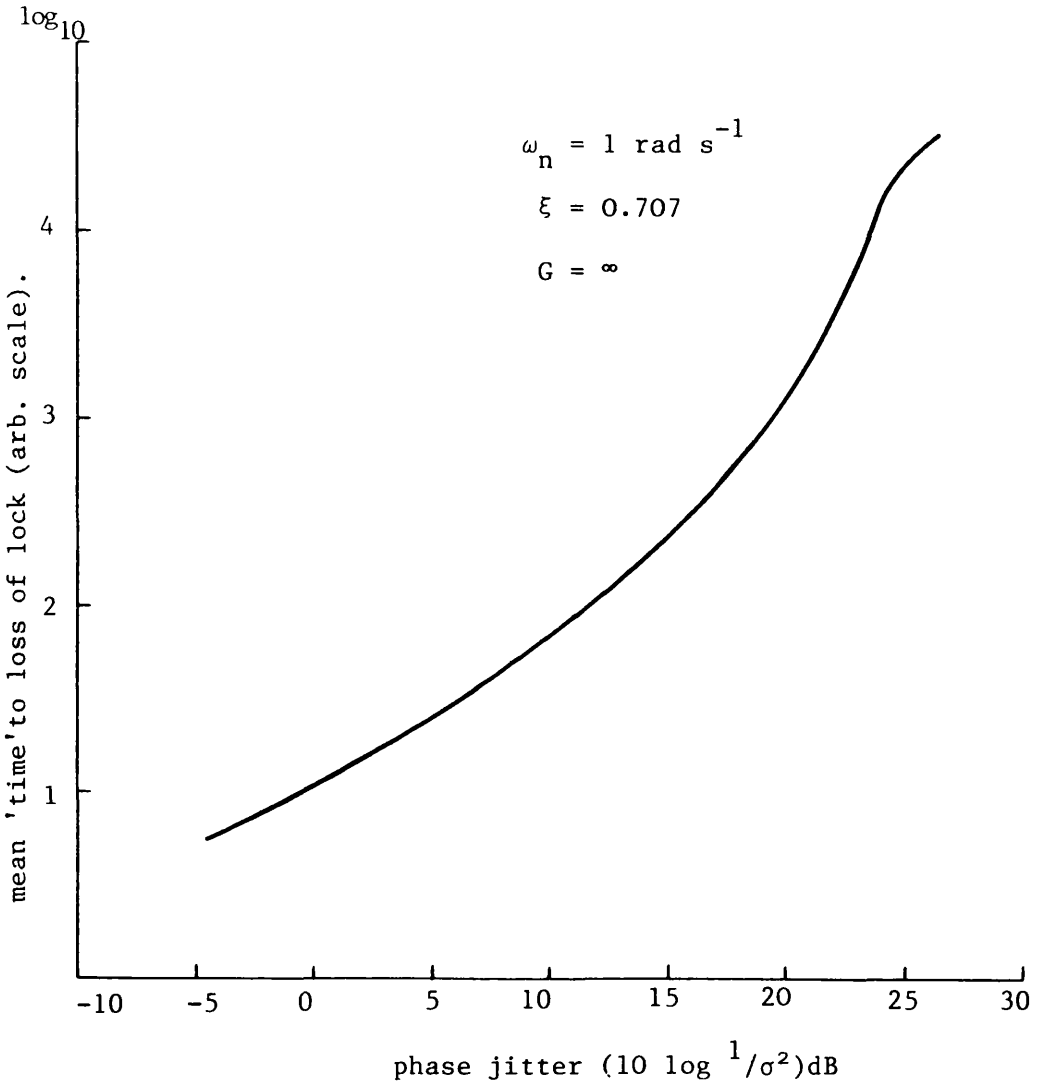


Figure 6.11. Graph of mean time to loss of lock of a 2Δ delay lock loop as a function of the variance of the phase jitter.

perturbation on the discriminator characteristics causing loss of lock. In this set of results mean time to loss of lock is taken as the number of programme steps in the Runge-Kutta procedure before loss of lock occurs. Each point on the graph was the result of averaging at least 100 trials. As expected the worse the SNR the lower the probability of lock. The general shape of the curve is close to that found by Holmes [3,4] using an analytic method.

6.4 EFFECT OF NOISE ON THE MAXIMUM SLIP RATE OF AN EXPERIMENTAL DELAY LOCK LOOP

An experimental model of a baseband 2Δ delay lock loop was constructed using high quality wide band analogue multiplier devices in each arm of the correlator network. The code sequence used was a maximal sequence of length, 1023 bit, clocked at a nominal 1 M bit s^{-1}. The natural frequency of the loop was set to a normalised value of $\omega_n = 1$ rad s^{-1} with a damping ratio of $\xi = 0.707$.

6.4.1 The Analogue Delay Lock Loop

The input signal to the delay locked loop was a summation of the received maximal length sequence and a white Gaussian noise taken from a wide-band white noise generator, and fed to a lowpass filter whose bandwidth is just enough to pass the main lobe of the PN code sequence used.

First, the delay lock loop was examined under the condition in which the received sequence level was set at a constant value, while the white Gaussian noise level was increased from zero until a -36 dB signal to noise ratio was obtained at the output of the mainlobe low

pass filter at the receiver input. No AGC was applied. It was found that increasing the noise level had very little effect on the maximum initial search rate from which lock could be achieved, as shown in Figure 6.12. For signal to noise ratio better than -25dB the maximum initial search rate was found to saturate to the value predicted for the noiseless case i.e. $\dot{x}_s$=2.0 bit s^{-1}. At very low signal to noise ratio down to -36 dB the maximum search rate to achieve lock must then be decreased. However, a further 6 dB signal to noise ratio improvement can be obtained by inserting a low pass filter whose bandwidth is 10x the bandwidth of the loop filter in each arm of the correlator network as shown by the broken line curve in Figure 6.12.

However, by using an automatic gain control i.e. keeping the wanted input sequence power + noise power to a constant value, both curves show exponential decrease in maximum initial search rate with input signal to noise decrese down to -36dB. Figure 6.13 shows that a 40 dB worsening of input signal to noise ratio from +10 dB results in a reduction of maximum initial search rate by approximately x10. The reason for this reduction is seen to be related to the reduction of the effective loop gain due to the decrease in signal to noise ratio with automatic gain control, as obtained by Ormondroyd [5] and Ormondroyd and Shipton [6]. By filtering each arm of the correlator network, a 6 dB better performance in signal to noise ratio is also obtained, as in the previous case. It will be appreciated that it is non agc delay lock loop described earlier which is modelled in section 6.3 and **not** the loop with agc as described above.

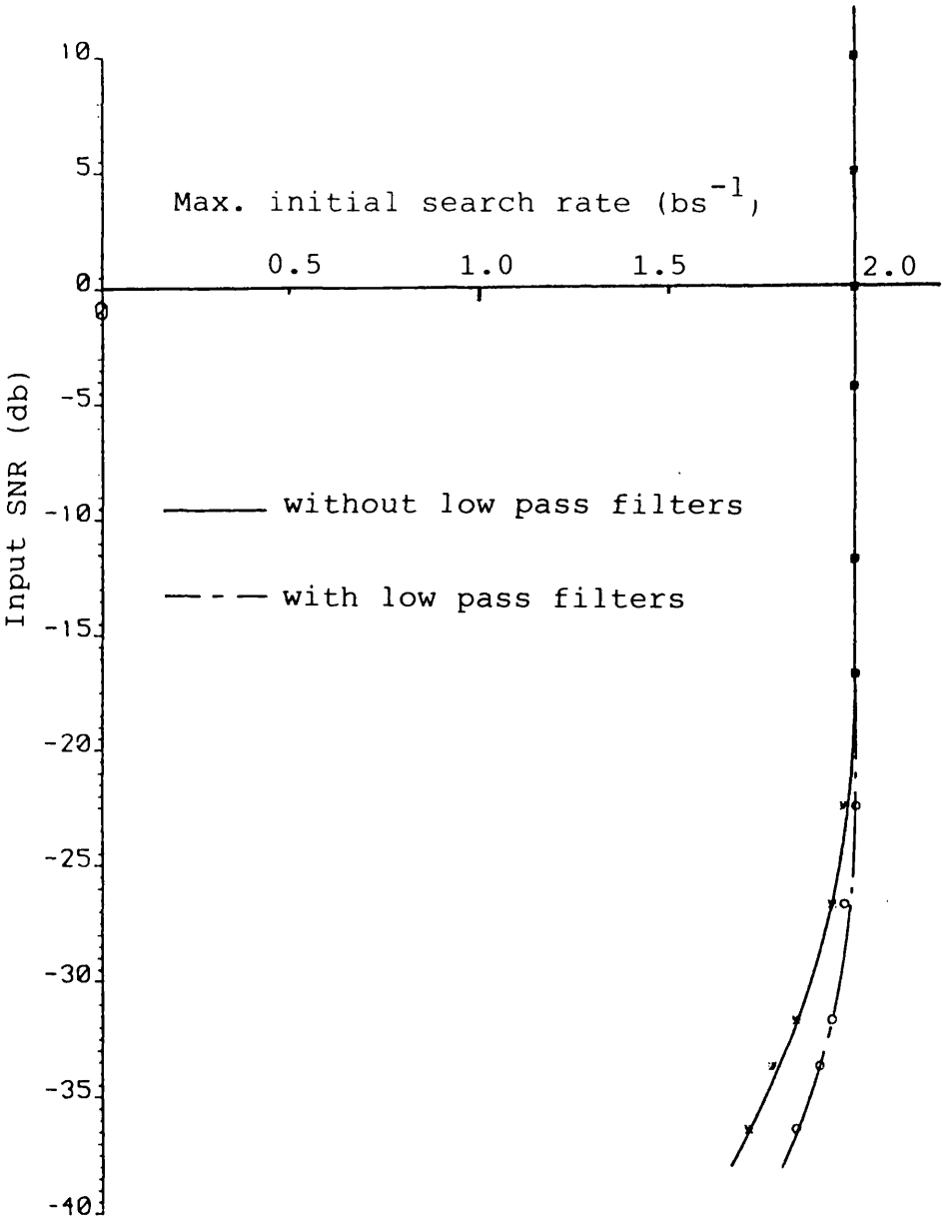


Figure 6.12. Effect of input SNR on maximum initial search rate for analogue multiplier loop without AGC.

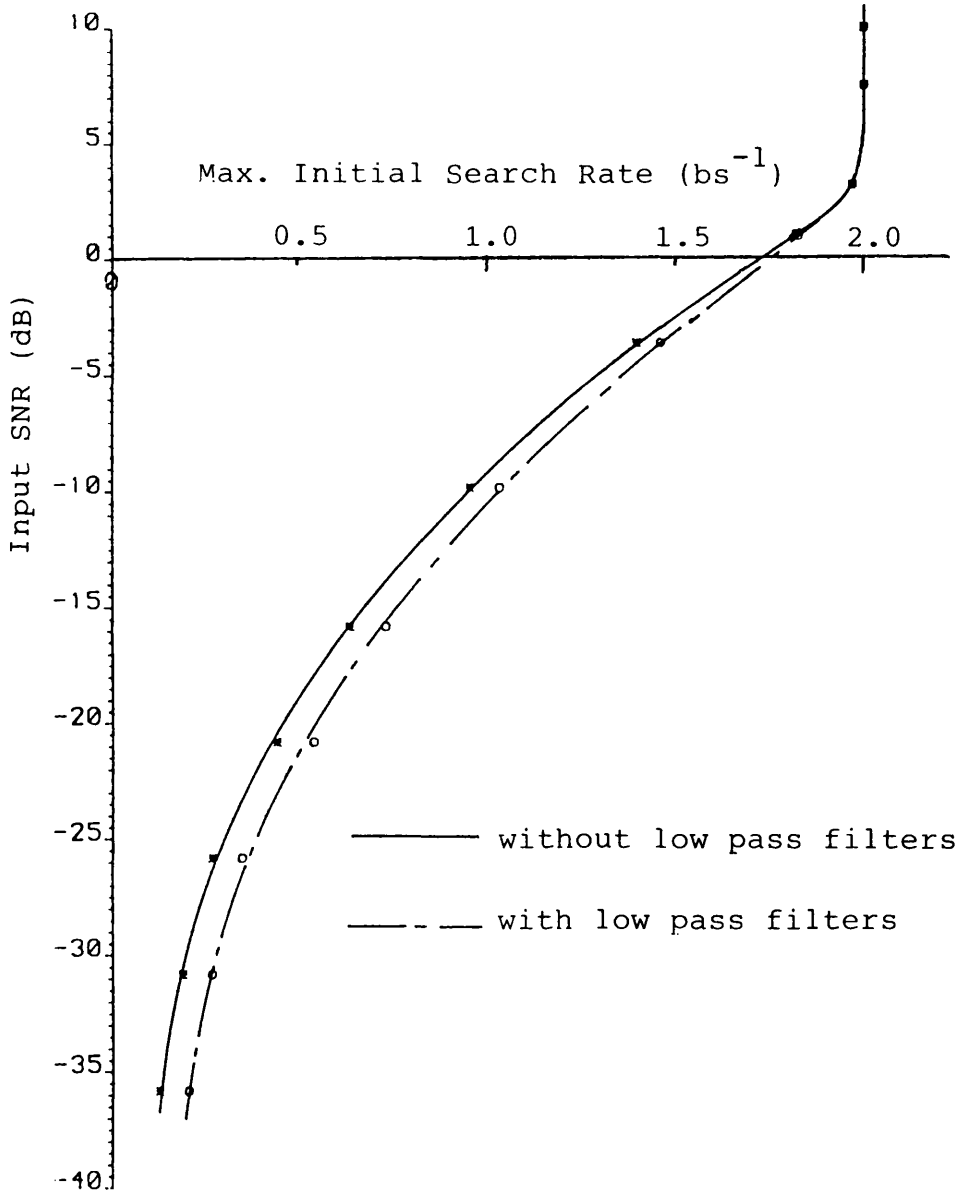


Figure 6.13. Effect of input SNR on maximum initial search rate for analgoue multiplier loop with AGC.

6.4.2 Digital Delay Lock Loop Performance

It is possible to use an EX-OR multiplier instead of the true analogue multiplier in the correlator network. In this case a hard limited circuit and a low pass filter is necessary prior to the cross-correlator network in order to clip the received sequence and to allow only two signal levels to be passed to the delay lock loop. It is noted that some loss is expected in performance when using hard limiters (also obtained by Tozer [7] of 1.96 dB loss). However, there is actually a marginal improvement in performance of the digital correlator over the analogue correlator with automatic gain control at up to -20dB SNR as found by Ormondroyd and Shipton [6] and Ormondroyd, Comley and Al-Rawas [8]. However, from -20 to -40 dB, the analogue correlator performs better. Figure 6.14 shows the maximum initial search rate versus the input signal to noise ratio for digital correlator with hard limiters with and without low pass filters in the cross-correlator networks arms.

The key features of the curves given in Figure 6.13 and Figure 6.14 [8] are: (1) The shape of both curves is similar, showing an approximate exponential decrease in maximum initial search rate with input signal to noise ratio (dB) for SNR < 0 dB: (2) the digital delay lock loop can tolerate approximately 2 dB worse input signal to noise ratio to maintain the same initial search rate: (3) for signal to noise ratio greater than 0 dB the maximum initial search rate saturates to the value predicted for the noiseless case: (4) a 6 dB improvement in signal to noise ratio is obtained in either of analogue or digital multiplier when followed by a low pass filter.

However, comparing those results with that shown in Figure 6.12, it is clear that by using analogue multipliers without AGC, the

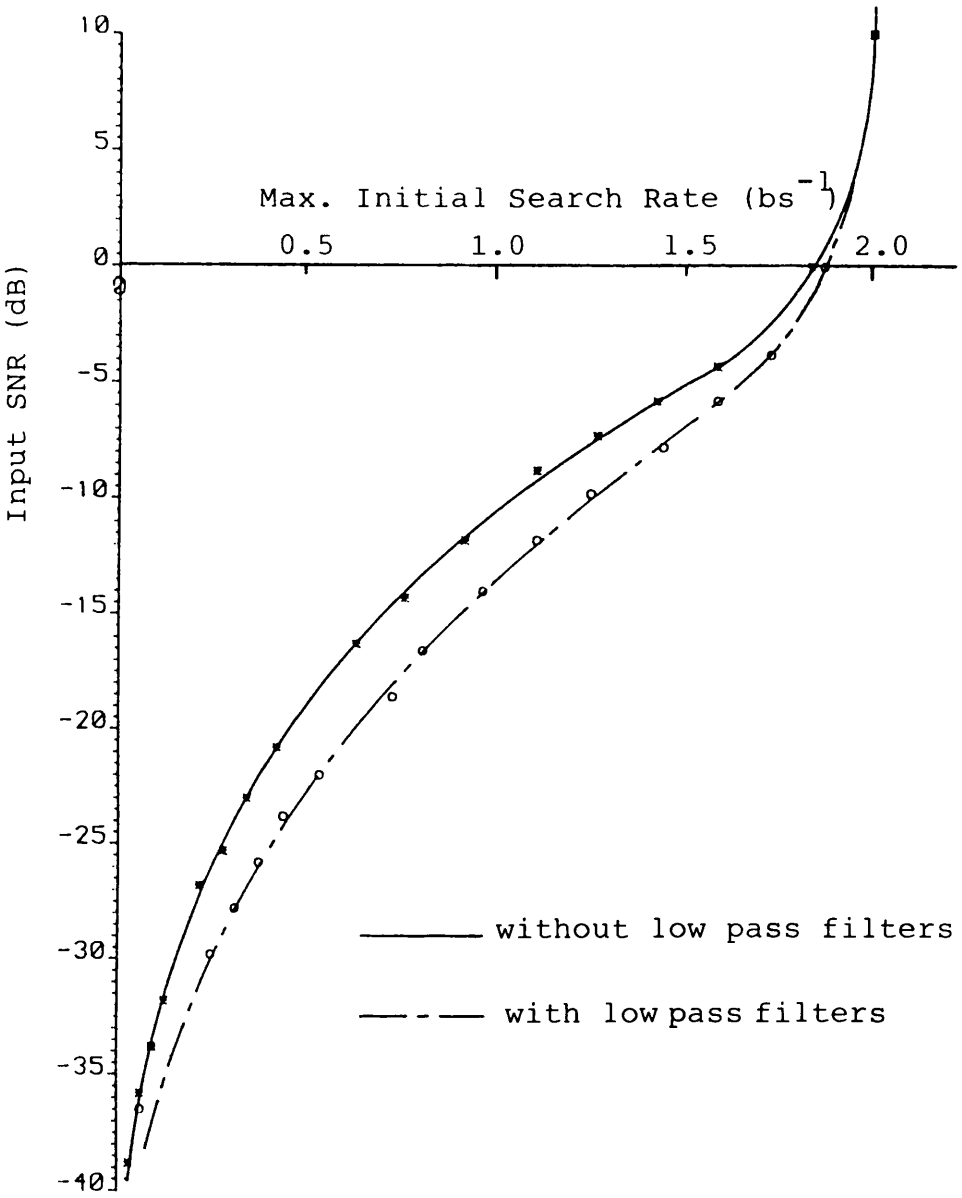


Figure 6.14. Effect of input SNR on maximum initial search rate for digitial multiplier with hard limiter.

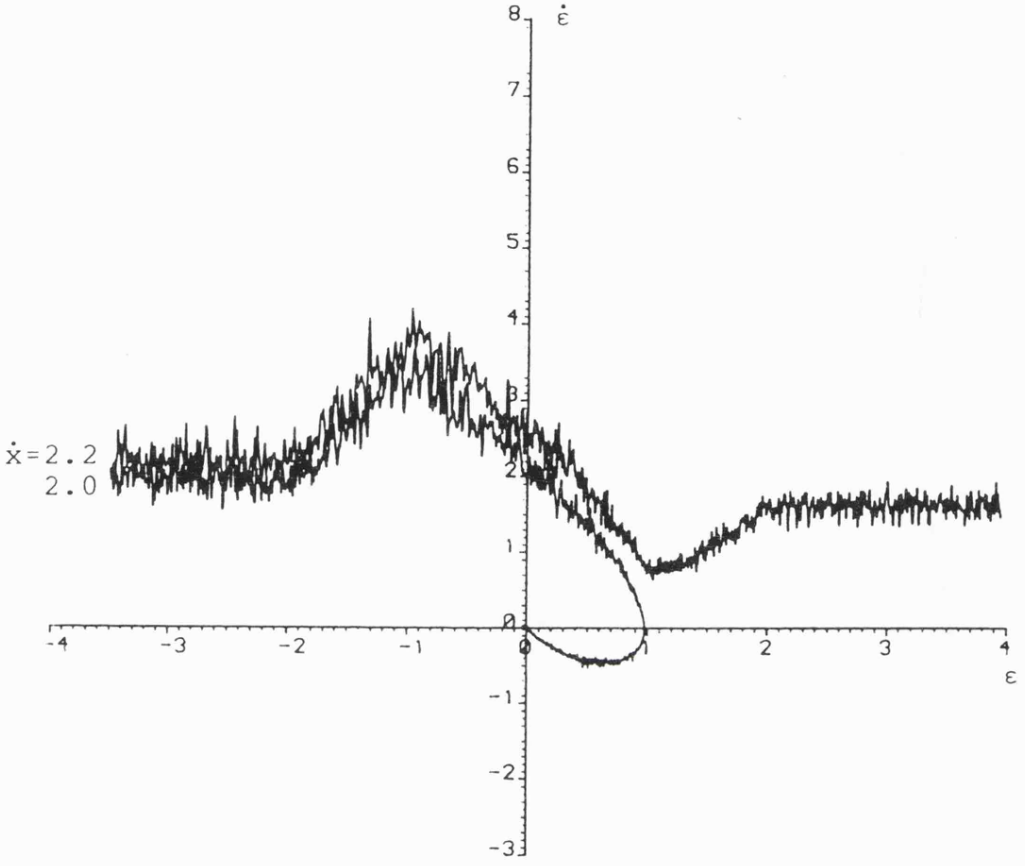


Figure 6.15. Acquisition trajectories of a 2-Δ delay lock loop in noisy condition.

maximum initial search rate can be maintained constant to at quite low input signal to noise ratio.

Figure 6.15 shows the acquisition trajectories of a 2-Δ delay lock loop in noisy conditions.

6.5 CONCLUSIONS

This chapter has introduced a computer model of the acquisition behaviour of a 2Δ delay lock loop in noisy conditions. The model allowed both amplitude and phase jitter to be applied separately. The results showed that both amplitude and phase jitter worsened the probability of acquiring initial synchronisation for any value of initial search rate.

It was seen that the SNR at the delay lock loop correlator output had to fall to about -10dB before the probability of acquiring lock on the first pass fell significantly, and for relatively high SNR initial search rate had very little effect on the probability of lock. Interestingly, however, it was found that there was an "optimum' search rate at which the loop could be operated in the worst case noise to achieve a given probability of lock. In particular, arbitrarily decreasing the initial search rate did not necessary improve the probability of acquiring lock.

The experimental results extended the analysis to include the effects of agc and hard limiting which are often applied to delay lock loops. These types of loop behaved in different ways to the simulated loop because of the decrease in effective loop gain as the noise level is increased. As a consequence the maximum allowable search rate was seen to decrease automatically as the input SNR ratio was increased.

CHAPTER SIX - REFERENCES

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CHAPTER SEVEN

SUMMARY OF CONCLUSIONS

In this thesis, an investigation has been carried out mainly into the synchronisation and tracking of pseudorandom sequences, as used in spread-spectrum communication systems and in ranging systems.

Four main problem areas have been defined, namely:

(a) The need to self synchronise the local code in a spread-spectrum receiver to the received, data modulated, code as quickly as possible.

(b) The need to simplify the design of the receiver in certain applications where a single transmitter communicates with a large number of receivers without compromising the system performance.

(c) The use of composite sequences to achieve reduced synchronisation time.

(d) The effect of white noise on the acquisition performance of a delay lock loop.

A further problem, that of optimising the power contained in the main lobe of the transmitted signal, has also been considered. These problems were considered in Chapters 3-6 of the thesis.

In Chapter 3, a computer model for the acquisition trajectory of a delay lock loop was obtained and it was found that the width of the discriminator characteristic of a delay lock loop had an important effect upon the maximum search rate which could be used between the

two codes under noiseless conditions, and an expression relating maximum search rate to the width of the discriminator characteristics was developed. Further, a novel method of obtaining considerably higher search rates in a delay lock loop was given which entailed controlling the discriminator characteristic from within the loop using an extra multiplier and a comparator. The new loop was tested exerimentally and found to be in extremely good agreement with the theoretically predicted results. The results show that the improvement obtained by switching the loop is by a factor of approximately 2.5 times, for a wide range of delay lock loops.

Unlike the standard delay lock loop, where the loop gain has very little effect on the maximum initial search rate for G>10, the switched delay lock loop was found to be dependent upon loop gain and particularly by the position in the acquisition process at which switchover occurred. And this was fully discussed.

The effect of initial search rate on pull-in time has also been considered. It was found that the characteristic of the pull-in time against the initial search rate can be split into three regions.

a) That region dominated by the epoch search process which is inversely proportional to the search rate.

b) That part of the characteristic dominated by initial fine phase synchronisation - or pull-in. Here it was found that pull-in time is largely independent of the initial conditions and dependent only on the loop parameters such as ω_n and ξ.

c) Settling time. This time is critically dependent upon the initial search rate, such that the closer the initial search rate is to V_{max} the longer the settling time.

It has also been found that the use of a high damping ratio can also increase the initial search rate, and a technique for switching the damping ratio from a large value during the initial search phase, back to 0.707 when an in-lock indication was given. A particularly important finding was that the technique of switching the damping ratio was **far less critical on the loop stability** than switching ω_n which is also a technique used to increase initial search rate. For a switched 2Δ delay lock loop the normalised search rate was found to increase from 5.1 to 9.2 to 13.3 $bits^{-1}$ when damping ratios of 0.707, 1.414 and 2.121 were used respectively. For the switched 4-Δ loop the search rate was found to increase from 9.9 to 26.5 $bits^{-1}$ when the damping ratio was increased from 0.707 to 2.121.

These various loop configurations were applied to two data modulated spread spectrum systems, one using a data source synchronised to the spreading sequence, and one which was asynchronous. The former type of modulation was detected using a novel type of receiver using data feedback, whilst the latter was detected in a loop with envelope detection. In each case **no degradation** in initial search rate performance was observed.

In Chapter Four, several novel spread spectrum configurations were described. First a method was given to reduce the complexity of the receiver to a single correlator (one local code sequence, and one linear multiplier). This was achieved by generating and transmitting multi-level sequences. This type of technique is particularly useful where several receivers are connected to a common transmitter. For a 2-Δ delay lock loop the transmitted signal has three-levels and for 4-Δ delay lock loop it has seven-levels. Experimental results for receiver systems having 2-Δ and 4-Δ delay lock loops showed no

degradation, in either the search rate or the white noise rejection performance, compared with a conventional system, as a result of these modifications. The 2-Δ and 4-Δ delay lock loops were tested experimentally under poor signal to noise ratio conditions down to -35dB for the 2Δ loop and -30dB for the 4Δ loops, using broadband white noise interference, with no degradation in performance.

Further delay lock loop variants were presented in Chapter Four which had the advantage of having both a higher search rate than the standard loop and a relative improvement in the signal to noise performance when the bandwidths of the receiver is reduced to 60% of the original mainlobe bandwidth (by virtue of the improved utilisation of the main lobe power spectrum). Some of the structures outlined are relatively simple to implement. These improvements were achieved by transmitting three level sequence generated in the transmitter simply by adding a half-bit shifted version of the transmitted sequence to itself. Other important points discussed in the Chapter, stated that the use of multi-level sequences at the transmitter in conjunction with loops such as 1-Δ and 2-Δ in the receiver can now generate wider N-shape error curves, with corresponding higher search rates. The only penalty paid by transmitting and receiving the multi-level sequence is the necessity of using a linear amplifier in both the transmitter and receiver rather than the commonly used non-linear one used to amplify the two level standard sequence.

Another, rather different type of sequence is described in Chapter Five. It is called a composite sequence or a Kronecker sequence, and has previously been applied by some authors to spread

spectrum systems. It is a two level sequence, but constructed from two or more short component sequences. The material in this chapter concentrates on two aspects: a) the properties of this type of sequence; and (b) process of synchronisation. The auto- and cross-correlation properties of the composite sequence were discussed in detail. Several different types of sequences were considered as component sequences, such as maximal length sequences and Barker codes. It was found that some of these sequences show very good auto- and cross-correlation properties, and a number of relationships were given from which the type and length of the component sequence, and consequently the resulting composite sequence, could be selected for spread spectrum applications. The relationship between the length of the inner and outer component sequence was found to be particularly important in the power spectral distribution of the transmitted sequence in which contiguous sidebands can be determined, and it is also important for the synchronisation process of the composite sequence in the receiver.

As far as synchronisation of this type of sequence is concerned a suggested method was given at the end of Chapter Five which involved the use of the modified switched delay lock loop discussed in Chapter three to synchronise the inner component sequence followed by a RASE or RARASE sequential estimation system to synchronise the outer component sequence. Using this technique the acquisition time could be reduced substantially, even at very low input signal to noise ratios.

Finally in Chapter Six, the effect of the white Gaussian noise on the maximum initial search rate was discussed. Experimental results for 2-Δ delay lock loop have shown that the maximum initial

search rate depends on the type of correlator used in the delay lock loop. In the case of an analogue multiplier, without automatic gain control, the maximum initial search rate remains constant down to about -30dB signal to noise ratio. However, with automatic gain control and a hard limiter, the maximum initial search rate drops to about 10% at about -30dB signal to noise ratio. Similar results were obtained for an EX-OR gates correlator. It was also noticed that about 6dB better signal to noise ratio could be obtained if a low pass filter, whose bandwidth is 10x the bandwidth of the loop filter, is used in each arm of the correlator network.

As further work, an area of work which immediately identifies itself is the extension of the noise analysis to cover the switched delay lock loop. Also the use of composite sequences to aid the initial synchronisation process is an area, which may yet yield important results in multi-user spread-spectrum systems. Of particular interest, is the combination of the delay lock loop and the RASE or RARASE sequential estimation systems. The use of multi-level sequences opens up many interesting possibilities in multi-receiver spread spectrum and ranging systems. In particular the half-bit shift, multi-level sequence system was only considered theoretically, and a practical implementation may be needed to confirm the theoretical predictions.

APPENDIX 1

EXPERIMENTAL DETAILS

Every delay lock loop implemented experimentally in this thesis was tested using a baseband model of the appropriate loop configuration. Particular care was taken in the design of the loop to ensure that the loop performed in an 'ideal way'. To achieve this the frequency of the PN sequence was scaled down to 1MHz and the loop natural frequency set to the normalised value of 1 rad s^{-1}. In this way, imperfections in the components used, such as the bandwidth and phase response of amplifiers, mixers and filters had a negligible effect on the operation of the loop. In practice, very high code clock frequencies and natural loop bandwidths place constraints on the choice of mixer and amplifier components, requiring them to have very wide bandwidths and linear phase responses. Failure to meet these requirements results in reduction in loop performance. Further reductions in performance also occur when circuit components such as envelope detectors and bandpass filters are placed in each arm of the loop, and particularly when the loop is operated at an IF frequency (say 10.7MHz) rather than at baseband.

In this work the analogue mixers used in the delay lock loop were Motorola 1495. These are widebandwidth low noise mixers with very wide dynamic range and a very low operating signal level requirement. The digital mixers were simply TTL EX OR gates which work well at 1MHz. All other digital circuitry was either TTL 74 series or 74S series.

A component of particular importance is the difference amplifier coupling both arms of the delay lock loop. Ormondroyd and Shipton [1] have shown that this particular component must not distort the differenced waveform if optimum performance is to be obtaine. A particular problem is arm-gain imbalance. To reduce signal distortion at this point the summing amplifier used was an LF157 operational amplifier which has a very high gain bandwidth product of 50MHz and a slow rate in excess of 70V/μs. To ensure that arm gain imbalance was estimated by careful impedance matching of the inputs of the difference amplifier. All active filters used in the loop were also implemented using LF157's. Where bandwidth was not a major design criteria TL'081 BiFet amplifiers were used. These amplifiers were used to make the threshold detectors and peak hold detectors.

The voltage controlled oscillator was a standard VCXO circuit using a 10MHz crystal oscillator, which was then divided to give a 1MHz square wave.

All analogue switches were either CMOS 4016 types of LF12333 types.

To make the measurements of phase an EX OR gate and integrator were used in conjunction with a precision voltimeter or an oscilloscope. Special broad range phase detectors are detailed in Chapter 3.

Reference

[1] Ormondroyd, R.F. and Shipton, M.S.: "The dynamic performance of delay lock loop code synchronisers..." IERE Conf. Proc. No. 50, pp 149-181, 1979.

APPENDIX 2

PRINTED PUBLICATIONS

The following is the list of publications that have arisen as a result of part of the work reported in this thesis.

1. Al-Rawas, L.A. and Ormondroyd, R.F. "Novel delay lock loop implementation for reduced acquisition time of PN sequences". Electronic letter, vol. 20, No. 1, pp. 22-24, 1984.

2. Ormondroyd, R.F., Al-Rawas, L.A., and Comley, V.E. "Imposed DLL configuration for PN code acquisition and tracking". IEE Conf. Proc. No. 235, pp. 175-180, 1984.

3. Ormondroyd, R.F., Comley, V.E. and Al-Rawas, L.A. "Accurate tracking of PN modulation in adverse SNR conditions". Proceedings of the IEE Conference on mobile radio systems and techniques. York. pp. 225-229, 1984.

4. Ormondroyd, R.F. and Al-Rawas, L.A. "An improved delay lock loop for use in ranging and data modulated spread spectrum systems". In Press, IEE Proc. Vol. 132, Part G, 1985.

NOVEL DELAY-LOCK-LOOP IMPLEMENTATION FOR REDUCED ACQUISITION TIME OF *PN* SEQUENCES

Indexing terms: Codes, Code synchronisation, Spread-spectrum techniques, Delay-lock loops

Pseudo-noise codes are widely used in spread-spectrum systems. A technique is described which significantly improves the acquisition speed of such codes. This consists of generating a broad discriminator characteristic whose phase may be controlled automatically by the loop filter output. Experimental and computed acquisition trajectories of the new loop are compared with standard loops.

Introduction: Delay-lock tracking loops (DLL)[1,2] are frequently used in spread-spectrum receiver systems to provide phase synchronisation between the pseudo-noise sequence embedded in the signal received from the transmitter and a locally generated replica sequence. This type of loop separately correlates the received sequence with several delayed replica sequences which are clocked from a voltage controlled oscillator (VCO). Each separate correlation between the sequences produces a triangular correlation function of width 2Δ bits. These are scalar weighted, differenced and filtered to produce the static N-shaped error curve, or discriminator characteristic, of the DLL which is used to control the frequency of the VCO. This characteristic is shown in Fig. 1 for a 2Δ loop. Because there is no delay error information provided beyond the N-shaped characteristic the VCO frequency is offset slightly from the clock frequency of the transmitted signal so that all relative phases between the codes may be searched serially until the codes come into phase synchronisation, at which point the delay error information is fed to the VCO to effect locking.

The dynamics of acquisition are determined by the loop gain, loop filter characteristics and the shape of the discriminator characteristic. In the standard loop configuration, when the sequences begin to come into synchronisation the positive slope of the error curve causes the search rate to accelerate. As the delay error decreases the error curve changes to having a negative slope and the search rate decelerates. The acceleration in search rate gives the loop a fast pull in time, but it also sets an upper limit on the maximum value of initial search velocity that the loop can handle and still acquire lock.

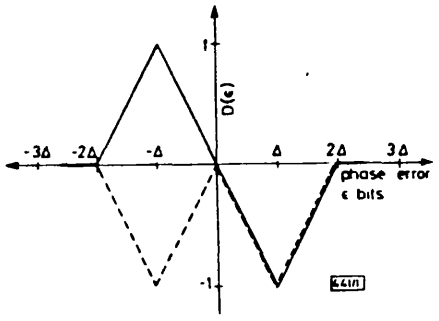

Fig. 1 *Discriminator characteristics of the standard 2Δ loop (———) and the switched 2Δ loop (- - - -), using sequences (S_{i-1} and S_{i-3}) and (S_{i-1} and $\overline{S_{i+1}}$), respectively*

The search rate is a far longer process than the pull in time, so it is vital that the initial search velocity is maximised without increasing the loop bandwidth, by increasing the ratio of the time that the loop decelerates relative to the initial acceleration even if this is at the expense of the pull-in time. Davies and Al-Rawas[3,4] have used this technique to advantage by broadening the discriminator characteristic beyond the normal 2Δ configuration. This letter shows that further significant reductions in acquisition time may be obtained by controlling the shape of the discriminator characteristic from within the loop so that there is minimal acceleration of the search rate during pull in.

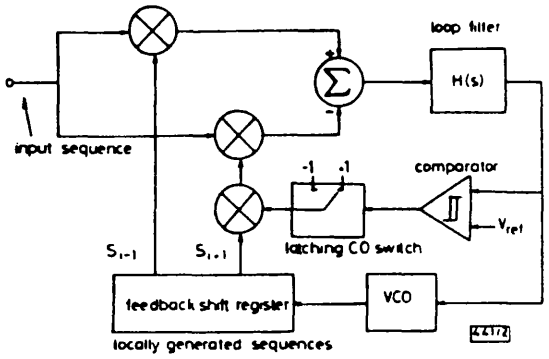

Fig. 2 *Schematic circuit diagram of new technique implemented on a 2Δ ranging loop*

Principle of method: Fig. 2 shows the new technique applied to a 2Δ DLL used in ranging receivers. This is purely for illustration and the technique may be applied to any DLL configuration. Control of the discriminator characteristic is achieved by the addition of a comparator, latching changeover switch and a linear multiplier in the S_{i-1} arm of the loop. For a binary sequence an exclusive-OR gate controlled by an R-S latch may be used instead of the multiplier and switch. The state of the DC input to the multiplier dictates whether S_{i-1} or $\overline{S_{i+1}}$ is fed to one arm of the DLL. If $\overline{S_{i+1}}$ is used the conventional discriminator characteristic of Fig. 1 is modified to the broken curve of Fig. 1. It should be noted that because the loop filter remains unchanged the in-lock noise performance of the new loop is similar to that of the conventional loop.

When the loop is in the initial search phase the comparator output is such as to cause $\overline{S_{i+1}}$ to be fed to the DLL correlator. When the codes are within 2 bits of synchronisation, the negative slope of the discriminator characteristic causes the search rate to be *decelerated*. When the codes are approximately 1 bit from synchronisation the discriminator output is at its maximum negative value. This is compared with a similar value reference voltage by the comparator, which changes state, causing the latching changeover switch to change state also. The polarity of $\overline{S_{i+1}}$ is reversed and the discriminator characteristic reverts to that of a conventional loop, i.e. the slope of the characteristic *remains* negative for a further 2 bits of delay error. A step change in discriminator output, and hence VCO frequency, does not occur because of the lag-lead transfer characteristic $H(s)$ of the active loop filter, but a small positive change is inevitable. For a loop filter which gives the DLL a damping factor of $\zeta = 0.7$ the period of acceleration is shorter than the 1 bit of a standard loop, and as a consequence a higher initial search velocity may be used. The increase in search velocity possible is determined by the loop filter characteristic and by the point at which the comparator changes state. Ideally the switchover should occur as close to the peak negative output of the correlator as possible if maximum benefit from the change in slope is to be achieved. The latch is necessary to ensure that the sequence cannot change polarity after triggering, even though the comparator changes state when the error voltage falls as the loop finally becomes phase synchronised. If the loop should lose lock an out-of-lock detector (not shown) resets the changeover switch to ensure that $\overline{S_{i+1}}$ is fed to the DLL during the serial search

Acquisition performance: For an idealised noise-free loop, of infinite gain, with the loop filter transfer function optimised to a linearly changing delay input the acquisition trajectory is the solution to the following nonlinear differential equations:

$$\dot{\phi} = -D(\varepsilon) - \sqrt{(2)}\phi \frac{\partial D(\varepsilon)}{\partial \varepsilon}$$

$$\dot{\varepsilon} = \phi \qquad (1)$$

where ε is the delay error between the received and locally generated sequences and $D(\varepsilon)$ is the discriminator characteristic normalised to a slope of unity at the origin.[5] For the case of the switched loop $D(\varepsilon)$ is the idealised switched discriminator characteristic. Figs. 3*a* and *b* show the computed acquisition trajectories for 2Δ and 4Δ[3,4] discriminator characteristics in switched and unswitched forms for the maximum search rate consistent with acquisition of lock. In the case of the switched loop, the point at which switching occurred was also adjusted to achieve the maximum initial search velocity. For the case of the 2Δ loop this occurred for $\varepsilon = -\Delta$, as expected. It will be seen that there is an impressive improvement in search rate possible by switching the loop. Further improvements could be made by continuing to widen the discriminator characteristics, but this would be at the expense of increased hardware in the receiver. Both the 2Δ and 4Δ switched loops show the marked deceleration in trajectory as the sequences come to within 2Δ of initial synchronisation, which may be compared with acceleration of the trajectory for the unswitched loops. When the loops have switched back to the normal loop configuration the switched loop tends to the same trajectory as the unswitched version.

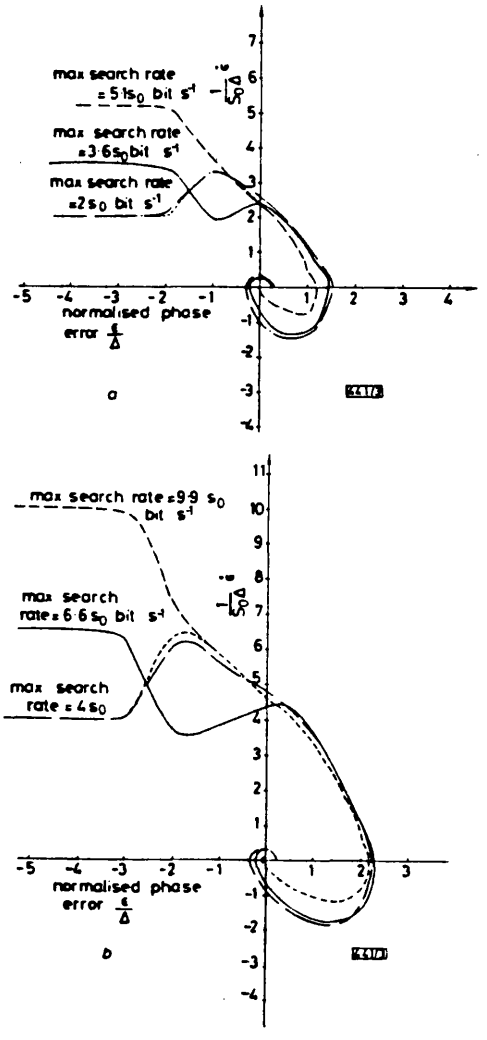

Fig. 3 *Theoretical and experimental acquisition trajectories of (a) 2Δ loop and (b) 4Δ loop, in switched and unswitched forms*

s_0 is the bandwidth of the loop filter
------- theoretical unswitched
- · - · - experimental unswitched
– – – – theoretical switched
——— experimental switched

Figs. 3*a* and *b* also show the experimental trajectories obtained on practical 2Δ and 4Δ loops. The pseudo-noise sequence was a 1023-bit maximal sequence clocked at a nominal 1 Mbits^{-1}.

It is clear that the unswitched 2Δ and 4Δ loops give a performance very close to that predicted theoretically. In the case of the switched loops there is a little more error, and the maximum search velocities found experimentally are slightly lower than that predicted theoretically. The principal reason for this is that the ideal switched discriminator characteristics cannot be achieved in practice because of the loop filter, and a small amount of acceleration is seen for both forms of the switched loop. Even so there is an 80% improvement in the search rate of the 2Δ loop and a 65% improvement in the search rate of a 4Δ loop when compared with the unswitched versions. The switched 4Δ loop is over three times faster than the unswitched 2Δ loop.

Conclusions: A new delay-lock-loop configuration has been presented which provides a substantial improvement in the maximum search rate obtainable. The cost in terms of additional hardware is minimal.

L. A. A. AL-RAWAS
R. F. ORMONDROYD
School of Electrical Engineering
University of Bath
Claverton Down, Bath, Avon BA2 7AY, England

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IMPROVED DLL CONFIGURATIONS FOR PN CODE ACQUISITION AND TRACKING

R.F. Ormondroyd, L.A.A. Al-Rawas and V.E. Comley

University of Bath, UK

INTRODUCTION

Pseudo noise (PN) spread-spectrum techniques are currently used in a wide variety of communications systems (1) such as code addressed multi-access systems, anti-jam protection, and ranging. In all these systems it is usual that some form of active or passive correlation is carried out in the receiver to extract the data or ranging information. In the most common systems, using active correlation, a locally generated replica sequence within the receiver is correlated against the received signal. This requires that the local sequence is synchronised to, and tracks, the received PN sequence, even in adverse input SNRs. Optimisation of the process gain of the system demands that phase synchronization is extremely good, even in these poor conditions. Another obvious requirement of the synchronization system is that acquisition of lock should be rapid, and phase shift tracking should be accurate. In spread-spectrum systems initial synchronization may be a two stage process using an active (or sliding) correlator (2) or a passive correlator such as a programmable SAW device (3) or CCDs (4) to provide coarse synchronization to within ± 1 bit. Fine synchronization and tracking may then be accomplished using either a delay lock loop (DLL) (5) or the tau dither loop (6). The use of a separate correlator for initial coarse synchronization is not vital, however, and either the DLL or tau dither loop may acquire initial synchronization as well as track the delay errors between the sequences. An advantage of using a loop for acquisition in code-addressed multi-access systems is that they are inherently programmable and that they may be applied to both coherent and non-coherent spread-spectrum systems.

Acquisition Using a Delay Lock Loop

The delay lock loop separately correlates the received sequence with several delayed sequences which are clocked from a voltage controlled oscillator (VCO). Each separate correlation between maximal length PN sequences produces a triangular correlation function of width 2Δ bits. These individual correlations are scalar weighted, summed or differenced as appropriate (7) to produce the static N shaped discriminator characteristic, or error curve, of the DLL which is used to control the frequency of the VCO in a feedback configuration. The error curve obtained for maximal sequences gives information regarding the relative phases of the codes only when the sequences are within $-n\Delta$ and $+m\Delta$ bits of synchronization, where $n = 1/2, 1, 2, 3 \ldots$ and $m = 1/2, 1, 2, 3 \ldots$ (7) and there is no further phase information beyond these extremes until the sequences next come into synchronization. Figure 1 illustrates the discriminator characteristics of the 1Δ ($n = m = 1/2$), 2Δ ($n = m = 1$) and 4Δ ($n = m = 2$) loops (7,8). The advantage of the wide Δ loop is that the phase information is supplied over a greater range of delay error and it has the advantage of being able to track greater phase deviations, but this is at the expense of increased hardware complexity. Because of the lack of phase information over much of the sequence it is necessary to force the DLL to search the sequence epochs by offsetting the DLL's VCO relative to the clock frequency of the received sequence. The acquisition time is thus the mean time taken to search the epochs of the sequence, plus the pull-in time required to achieve a given delay-error accuracy from the moment that delay error information is supplied by the correlator discriminator characteristic.

The dynamics of pull-in are determined by the loop gain, loop filter characteristics and the shape of the discriminator characteristics, as detailed below. In particular these parameters set the maximum rate of change of phase error which the loop will track. They also set the maximum rate of change of phase allowed in the initial epoch search. Even for moderately long sequences the mean search time is considerably longer than the pull-in time, yet, despite this fact, DLL's are generally designed on the basis of good pull-in performance rather than on the ability to search the epochs as rapidly as possible prior to achieving phase synchronization. However, by using DLL's with switched parameters it is possible to optimise the search rate without affecting the in-lock performance. The switching of the loop parameters may be achieved in several ways to achieve these performance improvements. This paper outlines the basic switched DLL configuration. The results of other improvements will be given in the presentation.

It is convenient to present the DLL as a linear equivalent circuit (1,5,10) in which the separate DLL correlator arms and sequence generators are replaced by the discriminator characteristics of figure 1 (say). The loop filter has a transfer function F(s) and the lumped gain of the VCO and mixers is given as G and is assumed to be a scalar multiplication. The linear model of the loop is shown in figure 3. From this it is apparent that the timing estimate $\hat{T}$ is expressed as:

$$\hat{T} = \frac{GF(s)}{s}\,[D(\epsilon)] \quad \text{seconds} \qquad (1)$$

$$\text{where } T - \hat{T} = \epsilon, \text{ the delay error} \qquad (2)$$

$D(\epsilon)$ is the normalised discriminator characteristic which relates the delay error ϵ into a control signal operated on by $GF(s)/s$. It is convenient to normalise the timing estimate and delay error into bits, rather than real time

Defining: $\epsilon/T_C = x$, $T/T_C = y$ and $D(\epsilon/T_C) = D(x)$

and using (2) with (1) gives:

$$s(y - x) = GF(s)[D(x)] \qquad (3)$$

Spilker (10) has shown that optimum performance is obtained if the loop is second order. $F(s)$ is generally assumed to take one of two forms, a passive lag-lead low pass filter

$$F_1(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s} \qquad (4)$$

or the active lag lead low pass filter

$$F_2(s) = \frac{1 + \tau_2 s}{\tau_1 s} \qquad (5)$$

Using the passive filter for the sake of generality, it is possible to define $\tau_1 = G/\omega_n^2$, $\tau_2 = (2\zeta/\omega_n - 1/G)$ and $g = G/\omega_n$ where ω_n is the natural frequency of the loop and ζ is the damping factor. If G is high, such that $1/g \ll 2\zeta$ then:

$$gF(s) \approx \frac{1 + 2\zeta s/\omega_n}{1/g + s/\omega_n} \qquad (6)$$

Substituting (6) into (3) yields the equation:

$$\frac{s}{\omega_n}(\dot{y} - \dot{x}) = \frac{1 + 2\zeta s/\omega_n}{1/g + s/\omega_n}[D(x)] \qquad (7)$$

and defining $\dot{y} = 1/\omega_n \, dy/dt$ and $\dot{x} = 1/\omega_n \, dx/dt$ as normalised rates of change of y and x in bits/second gives the result:

$$\frac{1}{g}(\dot{y} - \dot{x}) + \ddot{y} - \ddot{x} = D(x) + 2\zeta \frac{dD(x)}{dx}(\dot{x}) \qquad (8)$$

Because $\frac{\ddot{x}}{\dot{x}} = \frac{d\dot{x}}{dx}$ then the final result is:

$$\frac{d\dot{x}}{dx} = -\frac{D(x) - 2\zeta D(x)\dot{x} + \ddot{y} - 1/g(\dot{x} - \dot{y})}{\dot{x}}$$

This is the defining equation of the normalised phase plane of the acquisition trajectory. This nonlinear equation cannot be solved analytically. In this work a computer solution technique was used using the Runge-Kutta-Merson numerical method as an initial value problem. Normally $\ddot{y}$ may be assumed to be zero. This technique requires an initial search velocity, $\dot{y}$ bit s^{-1}, and from this the resulting trajectory indicates whether lock has been achieved. The initial search velocity is then modified appropriately until a trajectory indicating lock is achieved.

Figures 4 and 5 show the theoretical acquisition trajectories of the 2Δ and 4Δ loops for several initial search velocities. The loop parameters chosen were: ω_n = 1 rad s^{-1}, ζ = 0.7 g = ∞. Figure 6 shows the theoretical trajectories of the (2 - 3)Δ loop. In these analyses the slope of the discriminator characteristic D(ε) was normalised to 1, as pointed out by Nielsen (9), to ensure identical in-lock performance. Each trajectory shows that there is a maximum search velocity, $\dot{y}_{max}$. Above this, it is not possible to achieve lock. It is clear from these trajectories that generally the initial search velocity is improved for the wider Δ loops. We have found from this study that $\dot{y}_{max}$ is related to the width of the discriminator characteristic by the expression

$$\dot{y}_{max} = 2.3n - 0.3n$$

for ζ = 0.7, G = ∞

A simple explanation of these results can be given, as follows. The codes initially slide past each other at a constant rate. As they come into synchronization the slope of the discriminator characteristic is positive and the search rate accelerates. When the delay error is -nΔ the slope of the characteristic changes and the search rate decelerates. Lock is achieved if the search rate can be reduced to zero with minimum phase error. The initial search rate can be made higher if the period for which the loop decelerates (in bits) can be increased relative to the period of acceleration. It is clear that both the 4Δ and 2Δ-3Δ loops have longer periods of deceleration relative to the period of acceleration than for the 1Δ and 2Δ loops. In the case of the (3-2)Δ loop, although the period of deceleration is the same as the (2-3)Δ loop the initial acceleration is twice as fast. Further significant improvements in acquisition speed are possible if the initial acceleration can be reduced or eliminated.

SWITCHED DLL FOR IMPROVED SEARCH RATE

Figure 7 and 8 show schematic diagrams of switched 2Δ and 4Δ loops applied to ranging receivers. The 4Δ implementation, shown in figure 8, is only one of several possible implementations (7). The basis of the modification is to control the shape of the discriminator characteristics, from that of the standard discriminator characteristic of figure 1 to that of figure 2, shown drawn for the 1Δ, 2Δ and 4Δ loops respectively. The exact position at which the characteristics are changed is determined from the output of the loop filter and the value of V_{ref}. In general the loop is first switched to produce the discriminator characteristic of figure 2 during the initial acquisition or searching phase. As the loops come into synchronization the slope of the characteristic is negative and the search rate decelerates rather than accelerates. When the delay error is at its peak negative value the loop is switched and the discriminator characteristic reverts to that of figure 1. The slope of the characteristic remains negative. The step change in correlator output, implied by the change in the characteristic, does not result in a step change in delay error because of the lowpass characteristics of the loop filter H(s). However, there is a reduction in the deceleration of the search rate immediately after switching the characteristics when the dynamics of pull-in take over from the initial search procedure. It is found that both loop gain and damping factor, ζ, have an effect on the actual acquisition trajectory.

The control of the discriminator characteristics may be described more easily for the 2Δ loop than the 4Δ loop, although the basic principle is identical. In the circuit of figure 7 either S_{i+1} or $\overline{S_{i+1}}$ may be fed to the appropriate arm of the DLL under the control of the comparator. This controls the state of a latching change-over switch, and ultimately the voltage fed to the multiplier inserted in the arm of the DLL. For the case of binary sequences the latching change-over switch and multiplier may be replaced by an exclusive OR gate and an R-S latch. Inverting the sequence S_{i+1} results in the discrimination characteristic of figure 2b. The latch is necessary to ensure that the sequence cannot change polarity after triggering, even though the comparator changes state when the error voltage falls as the loop finally becomes phase synchronised. The change-over is controlled automatically, depending upon the level of the voltage V_{ref}. Further, an "out of lock" detector, not shown, automatically resets the latch to ensure that $\overline{S_{i+1}}$ is fed to the DLL during the subsequent search. The implement ations shown in figures 7 and 8 represent only one method of achieving a switched discriminator characteristic.

Using the analysis technique described earlier the theoretical acquisition trajectories of the switched 2Δ and 4Δ loops were calculated, and the results are shown in figure 9 and 10. These are compared with the unswitched loop trajectories. The loop parameters are identical for each loop. It is clear from the foregoing that the absolute maximum search velocity of the switched loop is dependent upon the exact point at which the characteristics are at their maximum negative value. The results of figures 9 and 10 are taken for this optimum switch position for loop parameters ω_n = 1 rad s^{-1}, G = ∞, ζ = 0.7. Modifying these parameters also modifies the maximum initial search velocity. The theoretical results for the switched loop show the initial reduction in search rate as the sequences come into synchronization. At the point of switch over the deceleration is reduced and the characteristics of the switched and unswitched loops are identical in the right hand half of the phase-plane plot for the case of their respective maximum search velocities. This identical behaviour in the right hand of the plane is to be expected and also indicates that the search rate of the switched loop is at the optimum, for the conditions stated. If the switch over position is delayed or advanced from the optimum position the maximum search rate is reduced. This is shown in figure 11. The position required to give the maximum search rate for the 2Δ loop is -1 bit, and -2 bit for the 4Δ loop.

PERFORMANCE OF EXPERIMENTAL 2Δ AND 4Δ DLLs

Experimental 2Δ and 4Δ loops were constructed to enable comparison of the experimental trajectories with the theoretical trajectories. The loop parameters were identical to those used in the theoretical model, with the exception of the gain G, and each could be used in conventional or switched mode. The pseudo-noise code was a 1023 bit maximal sequence clocked at a nominal 1 M bit s^{-1}. Figures 9 and 10 compare the experimental trajectories with the theoretical trajectories. It is clear that the unswitched 2Δ and 4Δ loops give a performance

very close to that observed theoretically. In the case of the switched loop there is more error in the left half of the trajectory and the maximum initial search velocity is lower than predicted theoretically, but still considerably faster than for the unswitched loop. Both loops show a small degree of acceleration immediately after switch over, but their trajectories in the right half of the plane are almost identical to the unswitched and theoretical results. We have examined possible causes of this acceleration theoretically and we believe that several factors conspire to give the reduced performance. The three major factors are:

i) Im - perfect correlation characteristics. The characteristics given in figures 1 and 2 assume a very slow slip-rate. In practice the slip-rate between the sequences may be quite high. This causes rounding of thediscriminator characteristics. Ormondroyd and Comley (11) have shown that if the slip rate is in excess of 1.4 bit/sequence the correlation performance between sliding codes is significantly worsened with the injection of spurious correlations. Clearly in these high acquisition speed loops decorrelation effects become more important.

ii) Propagation delay around the loop. It can be shown theoretically that a delay of 0.7 bit before switch over occurs gives acquisition trajectories almost identical to the experimental results. Causes of this delay include the filter delay, VCO response time, delay in switching over the discriminator characteristics and the time taken to establish the new correlation level.

iii) Loop parameters. It can also be shown that reduction of the loop gain and modification of the damping factor also affects acquisition trajectories so that they give acceleration immediately after switch over, and characteristics similar to the experimental curves. Modification of the loop parameters from those required for optimum tracking performance is in fact yet another means of improving the maximum initial search velocity. In such circumstances acquisition of lock causes the loop parameters to be changed back to the optimum for good in-lock performance. This aspect of the loop is currently under investigation.

CONCLUSIONS

Although the experimental results suggest that the maximum search rate obtainable is less than achievable theoretically from the ideal 2nd order delay lock loop, nevertheless the very simple expedient of switching the loop causes significant improvements in the initial search velocity, without worsening the in-lock tracking performance in any way. It has been found that there is an 80% improvement in the search rate of the 2Δ loop and a 65% improvement in the search rate of the 4Δ loop. Further, the switched 4Δ loop is over three times faster than the unswitched loop. We are confident that modification of the loop parameters will result in further improvements in maximum search rate.

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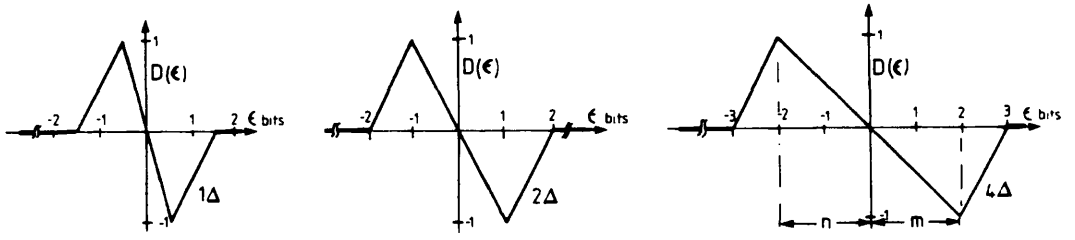

Figure 1 Normalised discriminator characteristics of 1,2 and 4Δ DLL implementations

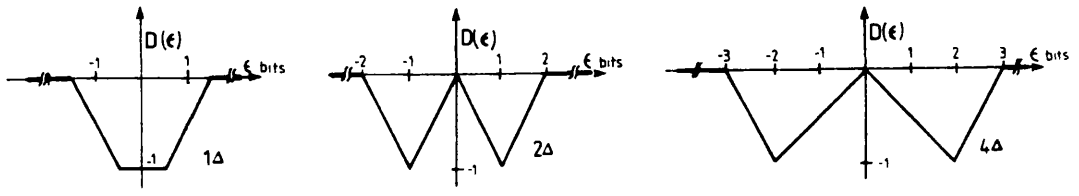

Figure 2 Normalised discriminator characteristics of the switched DLL implementations

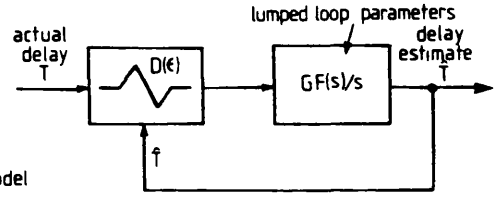

Figure 3 Linearised DLL model

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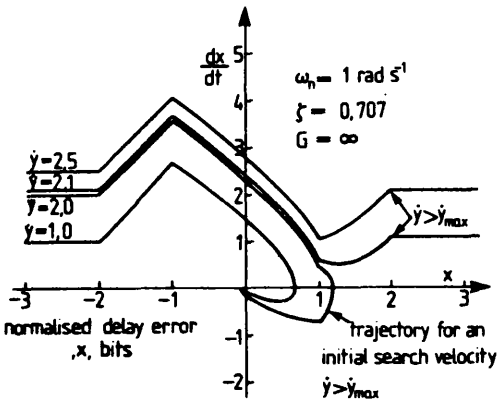

Figure 4 Acquisition trajectories of a 2Δ loop

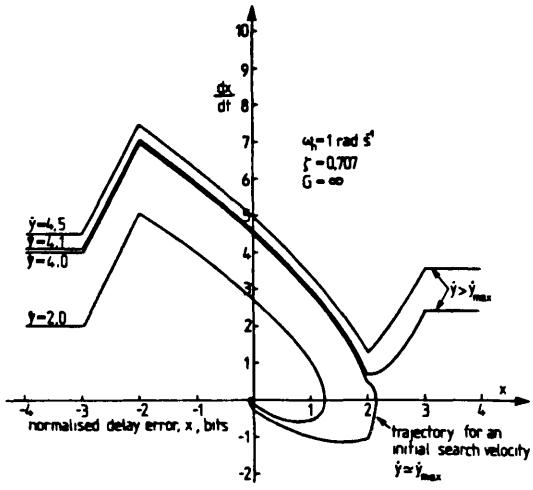

Figure 5 Acquisition trajectories of a 4Δ loop

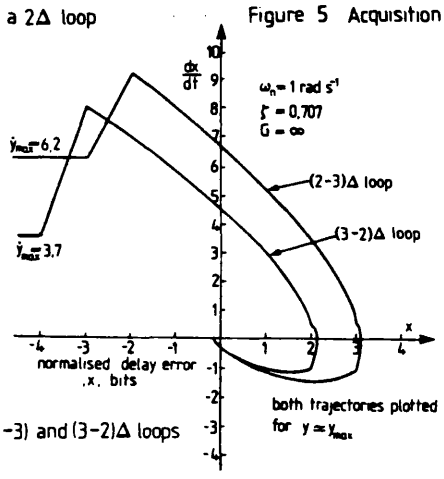

Figure 6 Acquisition trajectories of (2-3) and (3-2)Δ loops

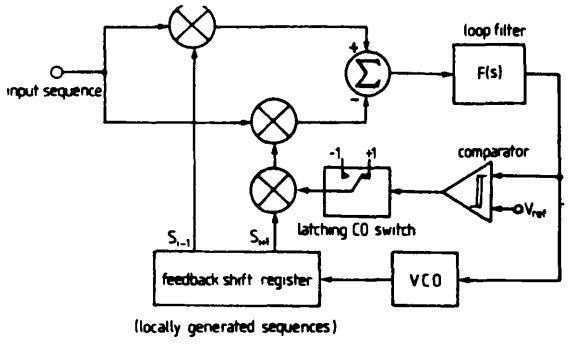

Figure 7 Switched 2Δ loop schematic

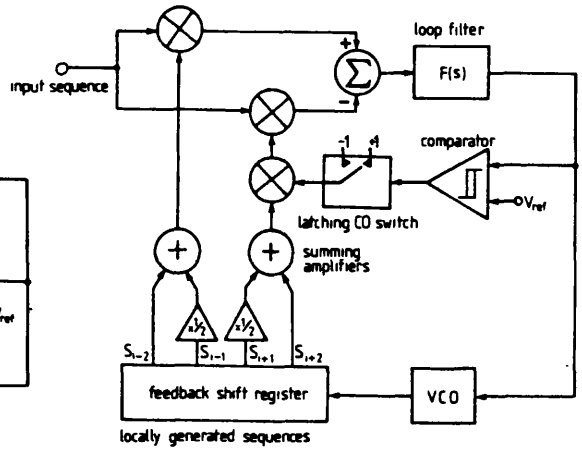

Figure 8 Variant of 4Δ switched loop

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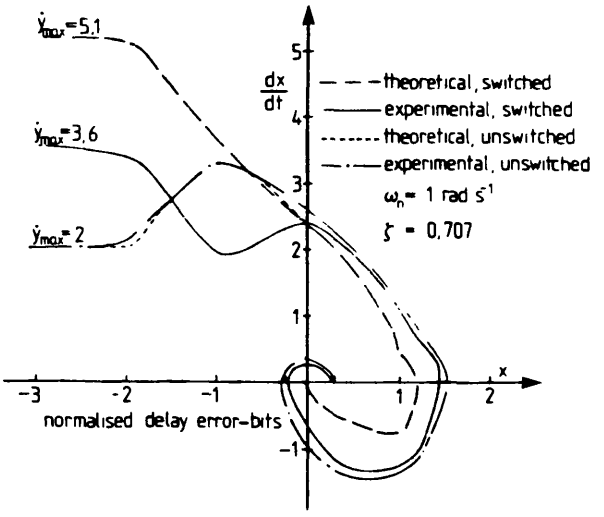

Figure 9 Comparison of the acquisition trajectories of the switched and conventional 2Δ loops

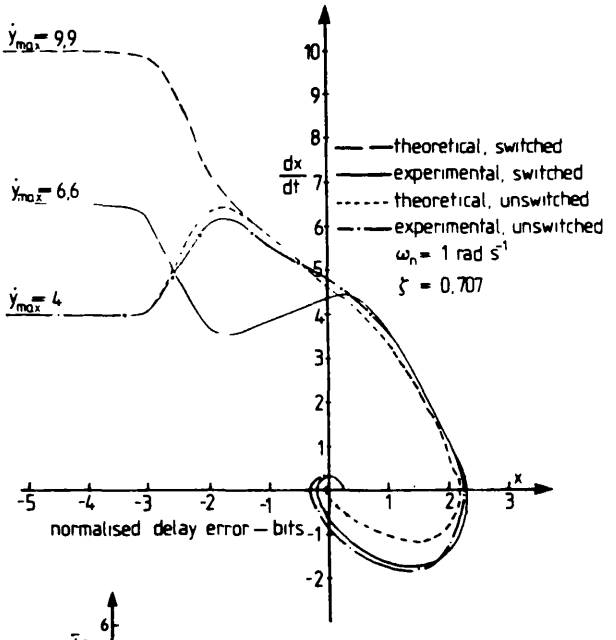

Figure 10 Comparison of the acquisition trajectories of the switched and conventional 4Δ loops

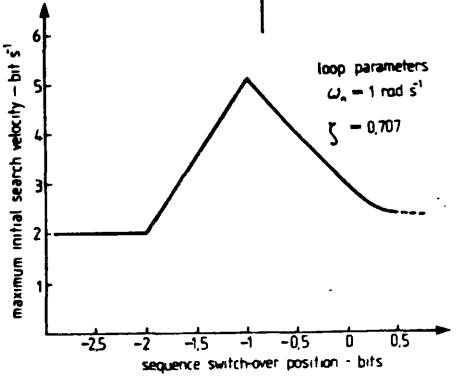

Figure 11 Effect of sequence switch-over position on the maximum initial search velocity

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ACCURATE TRACKING OF PN MODULATION IN ADVERSE SNR CONDITIONS

R.F. Ormondroyd, V.E. Comley, and L.A. Al-Rawas

University of Bath, UK.

SUMMARY

The delay lock loop is used frequently to acquire and maintain phase synchronisation between the incoming and locally generated pn sequences in direct-sequence spread-spectrum systems. Extreme accuracy is prevented because arm gain-imbalance and rectification of the input noise signals by the mixers and amplifiers within the loop result in phase offsets between the pn sequences. The paper proposes a novel variant of the delay lock loop which removes the problem of arm gain-imbalance, drift and noise generated offsets in phase. Experimental results are presented which show that the loop can operate in input SNR's worse than -30 dB yet have a mean phase error of only 0.01 bit.

INTRODUCTION

Pseudo-noise modulation techniques are finding increased use in tactical radio systems, navigation and aerospace communication systems because they offer low spectral energy densities in the transmitted signal and because of the inherent address present in each code when used in multi-user systems. The feasibility of such techniques, however, is dependent upon the ability of the receiver to remove the wanted signal from large levels of background noise, either by correlation or convolution techniques. In the former, accurate synchronisation is required between the incoming sequence and a locally generated replica sequence to maximise the correlation between the two codes, and in the latter case the clock frequency must be precise and the filter matched to the sequence. The delay lock loop (DLL) (1) is commonly used to acquire initial phase synchronisation in correlation receivers, and to track the phase of the incoming sequence under conditions of Doppler shift and frequency drift.

A typical DLL is shown in figure 1, and is of the 2Δ type. The incoming pn sequence is separately correlated with early and late replicas of the sequence generated by the VCO. For maximal sequences each correlation produces a triangular correlation function, one delayed by 2Δ relative to the other, where Δ is the chip width of the sequence. The filtered output of the difference amplifier linking both arms of the loop produces an N shaped discriminator characteristic, or error curve, as shown in figure 2. Phase error between the sequences results in an error voltage being generated which controls the frequency of the VCO in a feedback configuration. It is clear from the discriminator characteristic that the feedback is only negative for delay errors in the range $\pm\Delta$ (for the case of the 2Δ loop). Between $|\Delta|$ and $|2\Delta|$ the feedback is positive, and beyond $\pm 2\Delta$ no delay error information is available until the codes next come into synchronisation. In this case the VCO idles. It is possible to broaden the range of delay error which gives an error voltage output by using extra early and late correlators to broaden the discriminator characteristics (2-4). These "wide-Δ" loops allow a higher initial search velocity, and a greater tracking range, but at the expense of increased hardware complexity and cost. The dynamics of acquisition and tracking are controlled by the shape of the discriminator characteristics, the loop gain and the loop filter characteristic.

As there is no delay error information supplied to the loop for delay errors $> \pm 2\Delta$ it is necessary for the VCO to idle at a slightly different frequency to the clock frequency of the incoming sequence so that every epoch of the sequence may be searched serially. The maximum offset in frequency gives the epoch search rate, and this is determined by the loop dynamics and the level of noise at the input to the DLL.

The offset in frequency of the VCO gives rise to "loop-stress" (5). The result of this is that when the two sequences are finally in frequency lock an error voltage is generated to compensate for the offset frequency of the VCO. Because of the finite loop gain the error voltage gives rise to a steady-state in-lock phase error between the two sequences. This problem is compounded by two other major problems which further limit the accuracy of phase synchronisation. The first of these is arm gain-imbalance. This occurs because it is difficult to match the gains of the mixers, bandpass filters and amplifiers in each arm of the practical delay lock loop correlator. This means that there is a slight change of slope in the discriminator characteristics about $\epsilon = 0$. If noise is present at the input to the loop this results in phase jitter which is effectively 'rectified' by the non-linearity in the discriminator characteristic to give a mean phase offset. This effect is dependent upon the input noise level, and may counteract, or reinforce, the phase offset due to loop stress.

The second problem occurs as a result of limited dynamic range of the components in a spread-spectrum system, and non-linearity and gain-compression in the DLL mixers in particular. The signal at the input to the DLL is corrupted by broad-band noise which may be 30-40 dB more than the signal. The signal is recovered only after the DLL mixers in each arm, and the noise is removed by the loop filter, which will have a cut off frequency much lower than the code clock frequency. Non-linearities in these components rectify the large noise level to produce a dc offset voltage which produces a further phase error.

Two consequences of these phase errors are: (i) there is loss of the wanted despread signal in the data correlator section of the receiver because of decorrelation and (ii) loss of lock occurs at much lower input SNRs than predicted by simple linear theory (6). In this paper we consider two aspects of the delay lock loop. The main aim of this paper is to present a novel variant of the delay lock loop in which phase offset due to arm gain-imbalance, rectification of the input noise, loop stress and VCO drift is removed to a very large extent. The expected improvements in performance are supported by experiment. The results are presented for the case of a spread-spectrum ranging receiver, in which the pn sequence is not data-modulated. However, the technique may be applied to the case of a sequence inversion keyed data modulated direct-sequence system for a small increase in hardware complexity.

These modifications allow the loop to be used in more adverse input SNR conditions than otherwise possible. However, in the first section of the paper we present experimental data comparing the acquisition performance of DLLs under noisy conditions using analogue multipliers and AGC, with DLLs using hard limiters and EXOR multipliers. To the authors' knowledge this data has not been presented before, yet it is important since the acquisition of lock is non-linear and has not been solved for the case with noise.

EFFECT OF INPUT SIGNAL TO NOISE RATIO ON THE INITIAL SEARCH RATE

The in-lock performance of analogue delay lock loops (i.e. using analogue mixers) with AGC and digital delay lock loops using hard limiter and EXOR multipliers is well documented (6). Analysis is straightforward because the loop can often be considered linear. However, the initial acquisition performance in noise has not been considered in detail. In this section we present experimental data showing the effect of the input SNR on the maximum initial search velocity of a DLL commensurate with almost 100% probability of lock. In the experiment two identical baseband DLLs were constructed using maximal sequences of length 1023 bit, clocked at a nominal 1 MHz. The natural frequency of each loop was set to a normalised value ω_n = 1 rad s^{-1} and the damping ratio was chosen as ζ = 0.707. One of the loops used high quality wideband analogue multipliers, together with ideal agc, whilst the other used a hard limiter and EXOR multipliers. Although the loop gains of the two loops were different Nielsen (7) and Spilker (6) have shown that loop gain has negligible effect on acquisition trajectories of DLLs under noiseless conditions when the loop gain, G >> 10, which is the case for both loops.

Figure 3 compares the effect of input SNR on the maximum initial search rate of the two loops which can be tolerated to give almost 100% lock probability. The key features of the two curves are: (i) the shape of both curves is similar, showing an approximate exponential decrease in maximum initial search rate with input SNR (dB) for SNR < 0 dB; (ii) the digital DLL can tolerate approximately 2 dB worse input SNR to maintain the same initial search velocity; (iii) for SNR > 0 dB the maximum initial search velocity saturates to the value predicted for the noiseless case (6). It is interesting to note that a 40 dB worsening of input SNR from + 10 dB results in a reduction of initial search rate by approx x 10.

MODIFIED DELAY LOCK LOOP TO MINIMISE PHASE OFFSET ERRORS IN NOISY CONDITIONS

In this section we propose a variant of the DLL which minimises phase offsets. Under noisy conditions, the error signal fed to the VCO via the loop filter consists of a wanted error signal, representing the genuine phase error due to Doppler shift and loop stress, and an unwanted component due to arm gain-imbalance and noise rectification. It is necessary to remove the latter without modifying the former. Fortunately the two signals are effectively generated at two different parts of the loop. The wanted phase error information, due to frequency drift and Doppler shift may be lumped together and associated with the VCO, whilst arm gain-imbalance and noise rectification are both associated with the mixers, arm filters and the difference amplifier. The physical separation of the two signal sources can be used to advantage when processing the corrupted signals.

Figure 4 shows the basic technique used. The amplitude of both the early (S_{i-1}) and late (S_{i+1}) locally generated reference codes are reversed periodically at a rate determined by the code repetition rate. This causes the discriminator characteristics to be switched alternately between normal and inverted, as shown in figure 2. Any dc phase error signal representing the wanted portion of the control signal is thus converted to a square wave signal of amplitude equal to the phase error signal. This signal cannot be applied directly to the VCO because the sense of the feedback changes periodically from negative to positive and the loop would dither. The error signal is restored back to a dc level by reinverting immediately before application to the VCO. This is carried out in phase synchronism with the reversal of the discriminator characteristic, as in a chopper amplifier. Unwanted dc offsets that occur at any point within the loop between the switches are converted into a square wave ripple component of zero mean which may be removed by lowpass filtering. The wanted signal is not affected, and any small switching transients are removed by the same low pass filter.

Inversion of the discriminator characteristics may be achieved in two ways: (i) polarity inversion of each local reference code; (ii) interchanging the early and late reference codes to each arm of the loop. In practice polarity inversion is easily implemented using EXOR gates. The switching signal is generated from the "all 1's" detector of the sequence generator via a ÷ 2 counter. However, amplitude non-linearities within the analogue multipliers in each arm of the DLL cause switching rate offsets in voltage to be generated which appear as valid control signals. These signals are periodically inverted by the switch after the loop filter, where they cause the phase of the locally generated code to dither. Although much more complex, interchanging the early and late reference codes was found to overcome this problem to a large extent and was implemented in the loop presented in this paper.

The discriminator characteristics are reversed every code repetition period. This is much higher than the loop filter cut-off frequency. An obvious place to reinvert the error signal to the VCO is before the loop filter, using the filter to average out the unwanted signal component and remove switching transients from the wanted signal. However an active loop filter may be a source of the drift and poor dynamic range problems referred to earlier. In this work we chose to reinvert the error signal after the loop filter. Normally, this would distort the error signal after reinversion. To prevent this the active loop filter is also switched at the same rate, as shown in figure 5. This still provides noise filtering but translated to the switching frequency. The transients associated with switching the filter were found to last for only 5% of the duration between phase reversal, and therefore had a negligible effect. However, it is probable that this transient sets the limit on the ultimate performance attainable by the loop. Figure 6 shows the circuit used to reinvert the error signal after the loop filter.

The low pass filter used to remove the square wave modulation caused by unwanted dc offsets, and unwanted switching transients was formed by the capacitance of the varactor, controlling the VCO frequency, and the 10 MΩ series resistance, shown in figure 6. Further low pass filtering was found to be unnecessary.

PERFORMANCE OF THE SWITCHED DELAY LOCK LOOP

A delay lock loop was constructed in which the loop configuration could be switched between a standard loop and the modified loop. In this way the loop stress and non-linearities in the major loop components remained the same during the tests. The active loop filter could also be replaced by a passive loop filter, adjusted to give the same noise bandwidth.

RMS Phase Jitter

It is important that any modification to the loop should not affect the in-lock jitter performance of the loop adversely when compared with a standard loop. This is particularly important since this sets the probability of the loop losing lock. In this test broadband noise was used to corrupt the incoming sequence to the loop. Figure 7 compares the phase jitter resulting from the additive noise for (i) the standard DLL, (ii) modified DLL and (iii) standard DLL with passive filter. It is seen that switching the loop does not contribute to any additional jitter. It is further seen that the active filter begins to contribute to a worse jitter performance when the input SNR becomes worse than -20 dB. This is not seen in the passive filter, and does not become apparent in the switched loop until the input SNR is -30 dB.

Mean Phase Offsets in Noisy Conditions

Figure 8 shows the effect of the input SNR on the mean phase offset of the switched loop, compared with the standard loop. Both loops use an active filter. The curves are plotted for several values of loop stress, Δf. This is the offset frequency of the locally generated code relative to the transmitted code frequency. In this test the code repetition frequency was 3.185 MHz.

Considering the case of the standard loop with active filter shown in figure 8a, it is seen that loop stress has little effect in adverse signal to noise ratio conditions. The mean phase offset in this case is due entirely to noise rectification and arm gain imbalance. It is clear from this graph that at input SNR's worse than -25 dB the mean phase offset takes the value 1 Δ. In practice the rms jitter combined with the large phase offset cause the loop to lose lock at an input SNR $\approx$ 20 - 22 dB.

Although not plotted the mean phase offset for the case of a standard delay lock loop with low loop gain and passive loop filter is considerably worse when the loop is stressed by offsetting the local VCO frequency relative to the transmitted code frequency.

The cases may be contrasted with that obtained for the switched loop, shown in figure 8b. It should be noted that the scales are enlarged and linear. For the case of zero loop stress it is seen that the switched loop maintains a mean phase offset to better than $\pm$ 0.006 bit under input SNR conditions as low as - 26 dB, for the loop tested. At - 30 dB the mean phase offset has risen, but is still only 0.01 bit. Increasing loop stress has an effect upon the mean phase offset, but even so, the worst case phase offset is still within the range $\pm$ 0.03 bit at - 30 dB. It is interesting to note that loop stress becomes more important at low input SNR conditions. In the previous case the effect of noise rectification on phase offset was so important that the effect of loop stress was minor. The graph also highlights the fairly random nature of the phase offset with input SNR. This may, in fact be due to slow drift within the components, rather than due entirely to noise rectification.

CONCLUSIONS

This paper has presented a delay lock loop variant which is successful in overcoming the effects of arm gain imbalance and rectification of the input noise. The experimental delay lock loop showed that mean phase offsets as low as 0.01 bit could be achieved at - 30 dB for zero loop stress, and even with loop stress the mean phase error was within 0.03 bit at - 30 dB. A similar unswitched loop was shown to have a mean phase offset of about 1 bit at - 26 dB. The loop has also been found to be immune to deliberately injected dc offset voltages and long term component drift.

This type of loop should now enable the successful accurate synchronisation of sequences in a direct sequence spread spectrum system in input SNR conditions worse than - 30 dB.

ACKNOWLEDGEMENTS

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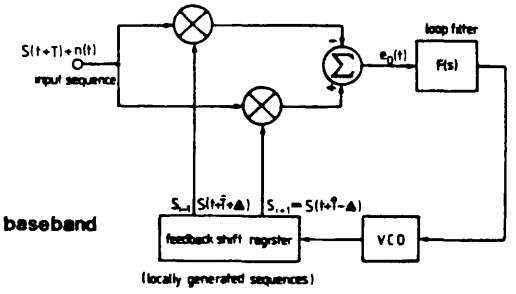
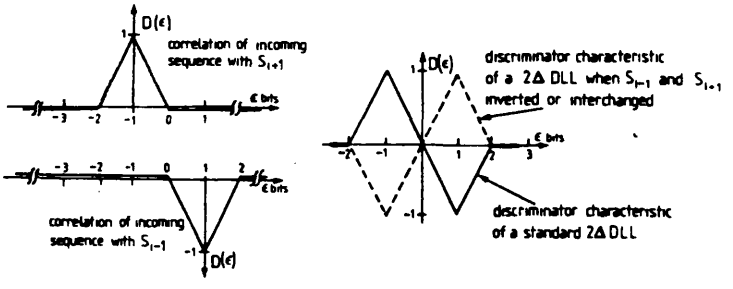


Figure 1. Schematic of standard 2Δ baseband delay lock loop system



The delay error, ε, is normalised by the chip period Δ

Figure 2. Normalised 'early' and 'late' correlations and discriminator chacteristics of 2Δ DLL

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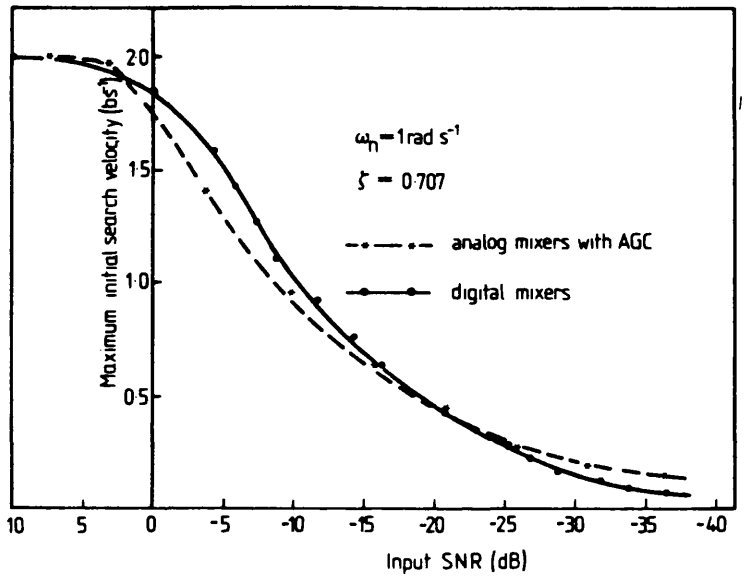

Figure 3. Effect of input SNR on maximum initial search rate for [a] analog loop, [b] digital loop

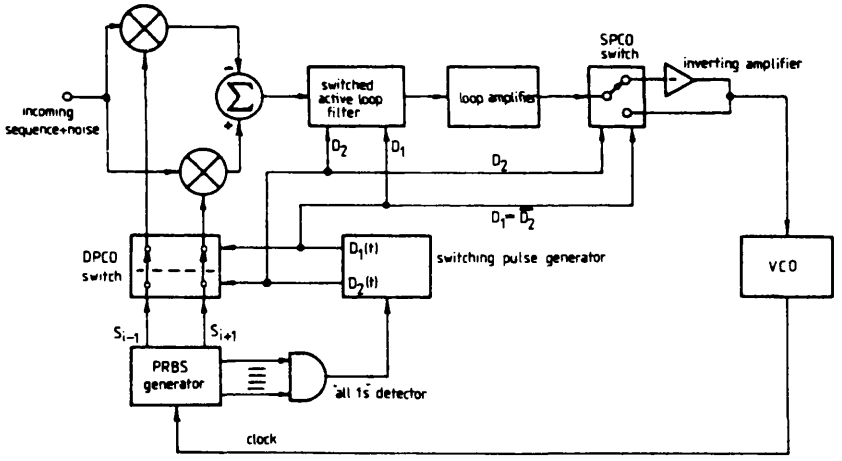

Figure 4. Switched 2Δ DLL variant for reduced mean phase offsets in noisy conditions

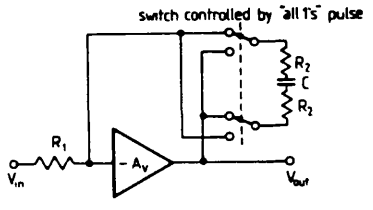

Figure 5. Switched active loop filter

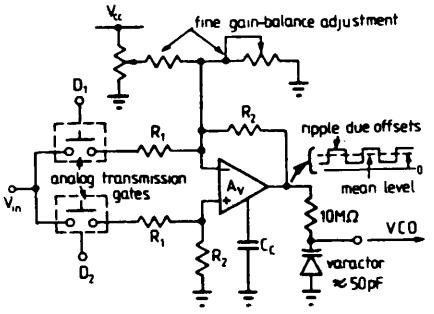

Figure 6. Switched inverting/non-inverting amplifier

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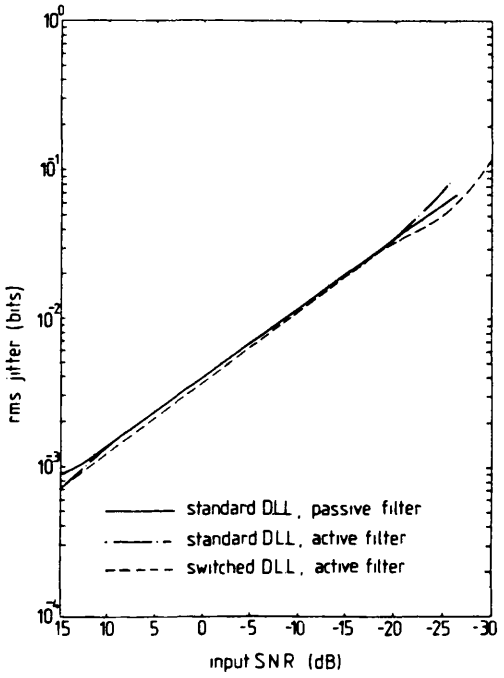

Figure 7. RMS Phase jitter characteristics of standard and switched 2Δ DLLs, when in lock

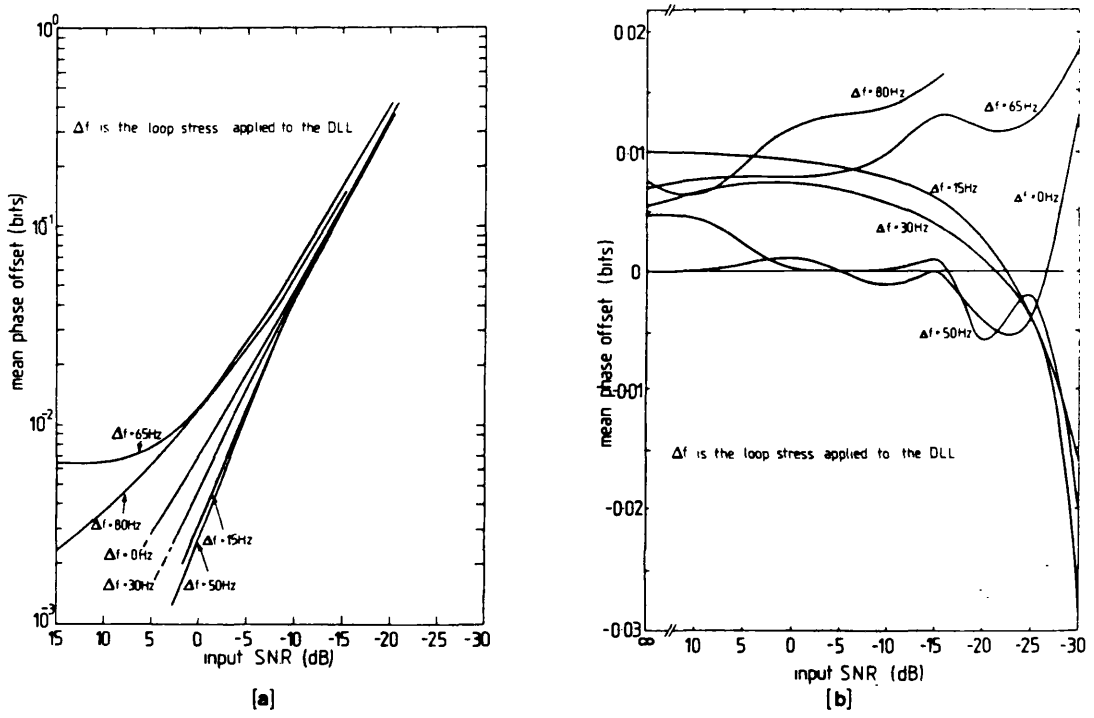

Figure 8. The effect of input noise level on mean phase offset for (a) standard, (b) switched 2Δ DLLs

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09-R.F. Ormondroyd:L.A.A. Al-Rawas.
10An improved delay lock loop for use in ranging and data modulated spread-spectrum systems

An improved delay lock loop for use in ranging and data modulated spread-spectrum systems

R.F. Ormondroyd, B.Eng., Ph.D., C.Eng., M.I.E.E., and L.A.A. Al-Rawas, B.Sc., M.Phil.

Indexing terms: *Electronic circuits, Circuit theory and design*

Abstract: Switching the phase of the discriminator characteristics of a delay lock loop (DLL) has previously been shown to improve the maximum search rate possible when the DLL is used to acquire initial synchronisation between two maximal length pseudonoise sequences. However, the theoretical analysis in this earlier work was found to be over optimistic when compared with the experimental results, because the analysis failed to take into account the effects of switching transients. The paper shows how the loop may be modified to remove switching transients, and hence achieve results which are as good as the original predictions. The paper shows the effect of the maximum initial search rate on the pull-in time of both standard and switched DLLs, and it is seen that increasing the epoch search rate can worsen the pull-in time of the loop near the maximum allowable value. The paper also shows how the switched DLL may be applied, in a cost effective way, to the case of a spread-spectrum system with data modulation using a form of data feedback which enables the DLL to acquire lock with no loss of performance.

1 Introduction

Pseudonoise (PN) spread-spectrum techniques are used in a wide variety of communication systems, such as ranging systems and multiple access communications systems [1, 2]. In direct sequence spread-spectrum systems the data to be transmitted is first modulo-2 added to a high speed PN sequence to achieve bandwidth spreading and reduction of the peak value of the power spectral density of the data signal. This spread signal is then modulated on to an RF carrier in the usual way. However, to recover the transmitted data it is necessary to despread the signal in the receiver. If active correlation is used, a locally generated replica PN sequence within the receiver is correlated against the received PN modulated signal. Maximum signal level is achieved at the output of the correlator when the two sequences are aligned exactly. Although external synchronisation channels may be used, this technique is wasteful of spectrum and is particularly prone to jamming, and it is usual in most ranging or multi-access systems for the local sequence to self-synchronise with the received signal using a synchronisation circuit in the receiver. An obvious requirement of the synchronisation system is that the initial acquisition of lock should be as rapid as possible, and tracking of phase changes due to doppler shift etc. should be accurate and fast.

In some spread-spectrum systems initial synchronisation may be a two-stage process using an active correlator [3] or a passive correlator or convolver [4, 5] to provide coarse synchronisation to within ± 1 bit. Fine synchronisation and subsequent tracking may then be accomplished using either a delay lock loop (DLL) [6] or the tau dither loop [7]. However, both loops may be used to acquire initial synchronisation as well as track the delay error between the sequences, and this has obvious system benefits of reduced cost and complexity; although, under given input signal-to-noise ratio (SNR) conditions, the maximum search rate attainable by either of the two loops is not as high as for the case of separate sliding correlation using an appropriate search/lock strategy [8, 9].

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The authors are with the School of Electrical Engineering, University of Bath, Claverton Down, Bath BA2 7AY, United Kingdom

1.1 Acquisition using a delay lock loop

The choice of PN sequence is particularly important in both multi-access and ranging systems, and both require sequences with 'good' 2-level autocorrelation performance and low values of cross-correlation when the wanted sequence is correlated with other, similar length, PN sequences. Maximal length PN sequences have relatively good cross-correlation properties and a 2-level autocorrelation function, and for sequence lengths in excess of 1023 bits there is an adequate number of different sequences for a code division multiple access system to be viable [1, 2]. As a consequence, maximal length sequences have found widespread use in spread-spectrum systems.

Consider the case of a simple ranging system in which the maximal length PN sequence is not modulated with data. In this case the standard 2Δ DLL separately correlates the received sequence with 'early' and 'late' locally generated replica sequences which are clocked from a voltage-controlled oscillator (VCO) [6]. Each separate correlation between maximal-length PN sequences produces a triangular correlation function of width 2Δ bits. These individual correlations are differenced to produce the static N-shaped discriminator characteristic, or error curve, of the DLL which is used to control the frequency of the VCO in a feedback configuration. The error curve gives information regarding the relative phases of the codes and, in the case of maximal sequences, the 2Δ DLL has phase information available only for $\pm 2\Delta$ bits. Beyond this range of delay error, no phase information is available to the VCO until the sequences next come into synchronisation, and it is necessary to force the DLL to search the sequence epochs serially by offsetting the VCO clock frequency relative to the clock frequency of the received sequence. This is usually to a slightly higher frequency.

Codes other than maximal length sequences have also been proposed for multi-access applications. Gold codes [12], for example, provide a large number of codes with a cross-correlation performance which can be no worse than the cross-correlation performance between two maximal length codes. However, these codes do not have 2-level autocorrelation functions, and, although the corresponding DLL discriminator characteristic may be nonzero for delay errors beyond $\pm 2\Delta$ bits, unambiguous information leading to phase lock is only available over the same range

of delays as for maximal length sequences and a serial s arch strategy must still be employed.

The acquisition time of the DLL is the mean time taken to search all the epochs of the sequence, plus the pull-in time required to achieve a given delay error accuracy. Pull-in occurs from the moment that delay error information is supplied to the correlator. However, even in noiseless conditions, final acquisition can only be guaranteed if the maximum initial search rate is less than a critical value which, specifically for the 2Δ 2nd-order loop, has been found to be [10]

$$v_{max} = 2\omega_n \quad \text{bit s}^{-1} \tag{1}$$

here ω_n is the natural frequency of the loop (rad s^{-1}).

For search rates above this value, it is not possible for standard 2Δ DLL to acquire phase lock. In noisy conions, it is only possible to specify a probability that lock l be achieved [11] even when the search rate is less than maximum given by eqn. 1.

The search rate can, of course, be increased arbitrarily increasing ω_n or the damping ratio ζ. However, this is the expense of an increased equivalent noise bandwidth the loop. For a 2nd-order loop with active lag-lead filter is is given by

$$B_n = \omega_n(\zeta + 1/4\zeta) \tag{2}$$

ined for the frequency range $-\infty < \omega < \infty$.

This would worsen the in-lock phase jitter of the loop, d the DLL design must be a compromise between good uisition performance and in-lock jitter performance d hence mean-time to loss of lock).

Davis and Al-Rawas [13, 14] have shown that the rch rate may be increased without increasing ω_n by adening the discriminator characteristics beyond the rmal widths of the 1Δ or 2Δ loops by the use of addinal 'early' and 'late' correlations which are scalar ighted and summed or differenced, as appropriate. For case of a general $(n - m)\Delta$ asymmetric 2nd-order DLL have found [15] that the maximum search velocity is en by

$$v_{max} \approx (2.3m - 0.3n)\omega_n \quad \text{bit s}^{-1} \tag{3}$$

the case of a DLL having a damping ratio, $\zeta = 0.707$ l loop gain $G \to \infty$.

It can be seen that v_{max} may be increased almost arbiily by increasing the width of the discriminator characstics. The limit is set by the length of the feedback uence generator, and the cost is increased hardware nplexity. In effect, the extra correlations provide parallel cessing of the code epochs.

Further, the authors have shown [15, 16] that additional, significant increases in search rate of a DLL used in nging receiver may be achieved without increasing ω_n l hence noise bandwidth) by controlling the phase of discriminator characteristics from within the loop ng acquisition. Fig. 1 shows the technique applied to a loop used in a ranging receiver application. In this gram, the input sequence S_i is assumed to be phase ked to the replica sequence, and is separately correlated h the early sequence, S_{i+1}, which is advanced by 1 bit ative to S_i, and S_{i-1}, which is delayed by 1 bit relative S_i. The phase of sequence S_{i+1} may be controlled by anging the state of the changeover switch. The technique applicable to arbitrarily wide DLL characteristics as own in Reference 15.

In References 15 and 16 there were significant devions between the theoretically predicted maximum initial search rates of an ideal switched loop and those observed experimentally, despite careful optimisation of the switch-

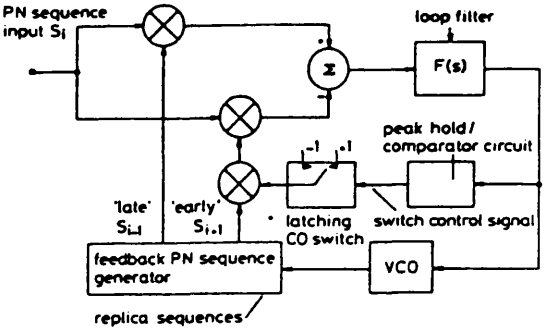

Fig. 1 *Schematic circuit diagram of a 2Δ switched delay lock loop in a ranging receiver*
The delay error signal is used to control the state of sequence S_{i-1}

over position of the discriminator characteristics. The error amounted to a reduction in maximum search velocity of approximately 33%. However, there was no significant error between the experimental and theoretical maximum search rates for the unswitched loops, from which eqn. 3 was found to hold. The reason for this has been found to be due to switching transients on the error signal to the VCO which the model failed to take into account. In this paper, we show how this shortcoming may be removed by a minor increase in hardware complexity. However, the ranging receiver application may be considered as a special case. In the majority of cases the DLL will be used in multi-access communications systems in which the PN sequences are data modulated. This paper considers the application of the switched DLL to the case of a data modulated spread-spectrum system, using a data feedback system. It is seen that data modulation has very little effect on the maximum initial search rate using this technique. The paper also considers the effect of the initial search rate on the pull-in time of both switched and unswitched DLLs.

2 Computer simulation of the acquisition trajectory of a DLL

The dynamics of pull-in are determined by the loop gain, loop filter characteristics and the shape of the discriminator characteristics. In particular, these parameters set the maximum rate of change of phase error which the loop is able to track. More importantly, they also set the maximum rate of change of phase allowed in the initial epoch search from which the loop can still acquire lock.

It is convenient to present the DLL as a linear equivalent circuit [2, 6, 17] in which the separate DLL correlator arms and sequence generators are replaced by the discriminator characteristic. This represents the mean value of the delay error signal fed to the loop filter for a given delay error between the two sequences. The linear model of the loop is shown in Fig. 2. The input to this model is the

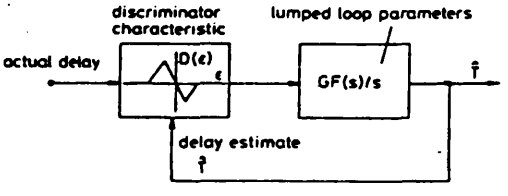

Fig. 2 *Linearised delay lock loop model*

arbitrary delay, T, with which the sequence $S(t - T)$ arrives at the receiver and the output is the delay estimate $\hat{T}$ of the local sequence $S(t - \hat{T})$ generated in the loop. The loop filter has a transfer function $F(s)$ and the lumped gain of the VCO and mixers is given as G. From this it is apparent that the timing estimate $\hat{T}$ is expressed as

$$\hat{T} = \frac{GF(s)}{s}[D(\varepsilon)] \quad \text{seconds} \tag{4}$$

where $T - \hat{T} = \varepsilon$ is the delay error, and $D(\varepsilon)$ is the normalised discriminator characteristic which relates the delay error ε between the sequences to the control signal operated on by $GF(s)/s$.

Normalising the timing estimate and delay error into bits rather than real time we may define new variables x and y such that

$$\varepsilon/T_c = x, \quad T/T_c = y \quad \text{and} \quad D(\varepsilon/T_c) = D(x)$$

where T_c is the period of one chip of the maximal sequence.

Eqn. 4 becomes

$$s(y - x) = GF(s)[D(x)] \tag{5}$$

$F(s)$ is generally either a passive lag-lead lowpass filter,

$$F_1(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s} \tag{6}$$

or an active lag-lead lowpass filter

$$F_2(s) = \frac{1 + \tau_2 s}{\tau_1 s} \tag{7}$$

Using the passive filter for the sake of generality, it is possible to define $\tau_1 = G/\omega_n^2$, $\tau_2 = (2\zeta/\omega_n - 1/G)$ and $g = G/\omega_n$ [17]. If G is high, such that $1/g \ll 2\zeta$ then

$$gF_1(s) \approx \frac{1 + 2\zeta s/\omega_n}{1/g + s/\omega_n} \tag{8}$$

and thus

$$\frac{s}{\omega_n}(y - x) \approx \frac{1 + 2\zeta s/\omega_n}{1/g + s/\omega_n}[D(x)] \tag{9}$$

Defining [2]

$$\dot{y} = \frac{1}{\omega_n}\frac{dy}{dt} \quad \text{and} \quad \dot{x} = \frac{1}{\omega_n}\frac{dx}{dt}$$

as normalised rates of change of y and x (bit/s) gives the result

$$\frac{1}{g}(\dot{y} - \dot{x}) + \ddot{y} - \ddot{x} = D(x) + 2\zeta\frac{dD(x)}{dx}\dot{x} \tag{10}$$

which may be rewritten as

$$\frac{d\dot{x}}{dx} = -\frac{D(x) + 2\zeta\dot{D}(x)\dot{x} - \ddot{y} + \frac{1}{g}(\dot{x} - \dot{y})}{\dot{x}} \tag{11}$$

This is the defining equation of the normalised phase plane of the acquisition trajectory. This nonlinear equation cannot be solved analytically. If it is assumed that the spread-spectrum system is operated between fixed sites, or that any Doppler shift is very small, the normalised rate of phase shift of the incoming sequence ($\dot{y}$) will be small and $\ddot{y}$ may be assumed to be zero. This allows the phase plane equation to be split into two simultaneous 1st-order differential equations. These were solved using the Runge–Kutta–Merson numerical technique. The method simply requires an initial search velocity between the two sequences $\dot{x}_s$ from which the trajectory may be obtained. The initial search velocity is then adjusted and a new trajectory computed until the maximum search velocity $\dot{x}_{smax}$ is found. The phase plane equation (eqn. 11) does not require the discriminator characteristic to be a specific shape, and the technique may be applied to switched and standard DLLs.

3 Modified switched DLL to optimise the initial maximum search rate

3.1 Switched DLL

In a standard 2Δ DLL, as the codes come into phase synchronisation the curve (shown as the —·—·— curve of Fig. 3*b*) causes the VCO frequency to increase, and the search rate increases. When the codes are within 1 bit of synchronisation the slope of the error curve changes sign and the search rate decreases. The dynamics of the loop dictate the maximum rate of change of phase error from which acquisition may be achieved ultimately. If the initial acceleration of the search process can be removed or reduced, it is possible to increase the initial search rate of the DLL yet still ensure that the maximum rate of phase change allows acquisition. Controlling the discriminator characteristic from within the loop enables this improvement to be effected.

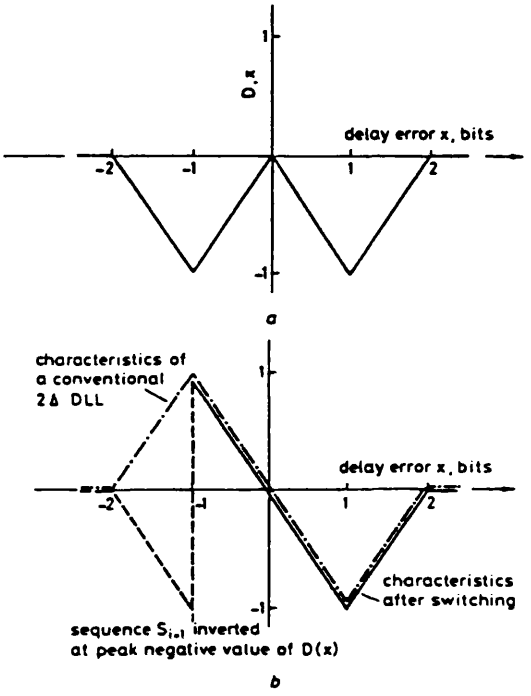

Fig. 3 *Discriminator characteristics of the 2Δ delay lock loop*
a During initial acquisition
b After switching the phase of sequence $\overline{S_{i-1}}$

In this technique, outlined in Fig. 1, the phase of part of the discriminator characteristic may be controlled by inverting the 'early' sequence, S_{i+1}, under the control of the delay error control voltage fed to the VCO. The sequences are initially switched so that S_{i-1} and $\overline{S_{i+1}}$ are fed to the arms of the DLL to give the discriminator characteristic shown in Fig. 3*a*. As the sequences come into

lock the delay error voltage to the VCO reduces and the search rate decreases (compared with an increase in search rate of the conventional DLL). When the delay error is such that the discriminator characteristic has reached its peak negative value, the state of the changeover switch changes and $\overline{S_{i-1}}$ is inverted back to the original sequence, S_{i+1}. This causes the correlation between the codes to change sign and the discriminator characteristics change, as shown in Fig. 3*b*. Although it is permissible to switch sequence $\overline{S_{i+1}}$ at other values of delay error during pull-in, switching over at the peak negative value gives the maximum improvement in search rate. Switchover may be controlled by comparing the delay error voltage with a fixed reference voltage in a Schmitt comparator, as in Reference 16, or using the peak hold/comparator circuit shown in Fig. 1 and detailed later. It is clear that, to maximise the initial search rate, the acquisition trajectory of the loop must always show a decelerating search rate in the upper quadrants of the phase plane of the trajectory.

By inverting the sequence during pull-in, the mean value of the delay error voltage at the summing junction has a step increase, but after this step change the delay error voltage continues to decrease. The step change would cause a large acceleration of the search process if allowed to pass directly to the VCO, removing any benefit gained. However, this does not occur because of the lowpass loop filter. Nevertheless, some acceleration of loop is inevitable and this limits the maximum search velocity from which acquisition can occur.

Fig. 4 compares the theoretically predicted acquisition

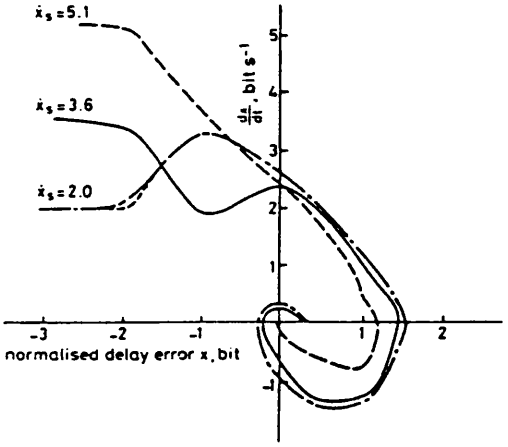

Fig. 4 Theoretical and experimental acquisition trajectories of a 2Δ delay lock loop in switched and unswitched forms

- - - - theoretical, switched
——— experimental, switched
····· theoretical, unswitched
— · — experimental, unswitched
ω_n = 1 rad s^{-1}
ζ = 0.707

trajectory of switched and unswitched 2Δ DLLs with the corresponding experimental trajectory [16]. It is clear that switching the discriminator characteristic results in a significant increase in the maximum value of the initial search rate compared with the unswitched version. However, the maximum initial search velocity, leading to acquisition, of the experimental switched loop is significantly less than the corresponding theoretical value, although the results for the unswitched loop are in excellent agreement. The reason for this is shown in the time dependence of the error voltage and rate of change of error voltage, of the experimental loop, illustrated in Fig. 5. It is seen that, immediately after switching the phase of the sequence $\overline{S_{i+1}}$, the

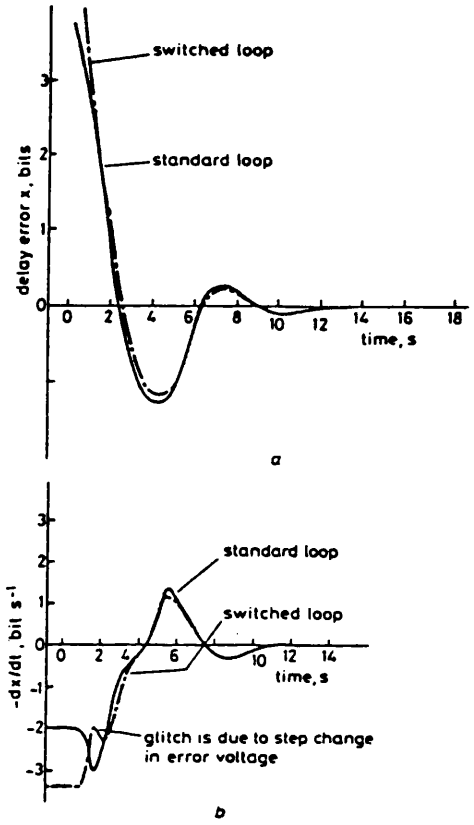

Fig. 5 Time dependence of the delay error and derivatives of the delay error signals fed to the VCO of an experimental switched 2Δ loop showing the increase in the derivative of the delay error voltage after switching the phase of $\overline{S_{i-1}}$

rate of change of error signal increases momentarily. This corresponds to the slight acceleration of the search process shown in Fig. 4. This is due entirely to the filtered step change in error voltage. In these experiments a 1023 bit maximal length sequence was clocked at a nominal 1 MHz. The loop filter parameters were adjusted to give $\omega_n = 1$ rad s^{-1} and $\zeta = 0.707$. Note that the trajectories in the upper RH quadrant of Fig. 4 are almost identical for switched and unswitched loops, indicating that for a given ζ it is the value of $\dot{x}$ at $x = 0$ which is the critical parameter to ensure acquisition.

In the theoretical analysis used in the comparison, the step change in discriminator characteristic was not allowed for, and switching over the discriminator characteristic was assumed to result in a continued negative slope to the discriminator characteristic, thereby maximising the period for which the loop decelerates. This is confirmed by Fig. 4. Lock occurs with no acceleration of the loop in the upper quadrants of the phase plane plot.

3.2 Modified switched DLL

It is possible to get the full benefit of the switched DLL (in terms of maximum initial search rate) by a modification to the structure of the loop to remove the offset voltage after switching. The new loop is detailed in Fig. 6 for the 2Δ loop. The technique is applicable to other wide-Δ and 1Δ loops.

The difference between this loop and the switched loop, discussed earlier, is the use of a DPCO switch SW1. SW2

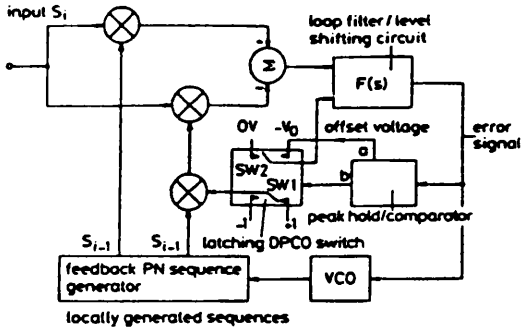

Fig. 6 *Schematic circuit diagram of a modified switched 2Δ delay lock loop to remove the problem of step changes in delay error voltage after switch over*

a 2 × analogue 'held' voltage
b Digital switch control output

and a simple summing junction applied to the active loop filter to provide a level shifting network. The analogue voltage ($-V_0$) is generated by the peak hold/comparator circuit connected to the delay error output from the loop filter, as shown in Fig. 7.

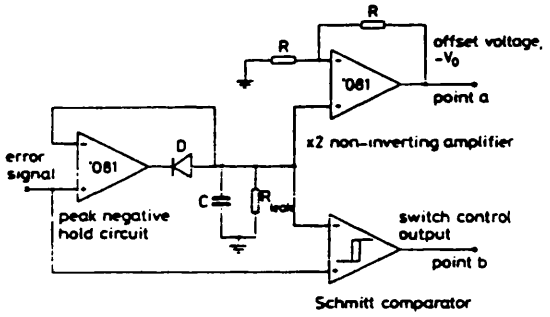

Fig. 7 *Peak hold/comparator circuit used to control the state of sequence S_{i-1} and generate the offset voltage $-V_0$*

The operation of the loop is as follows. When the loop is acquiring initial synchronisation, sequence S_{i+1} is inverted to give the discriminator characteristic of Fig. 3*a*. This is achieved by the state of switch SW1. At the same time, the state of SW2 ensures that 0 V level offset is fed to the level-shifting network in the loop filter and the VCO idles at a slightly higher frequency than the clock frequency of the received sequence. As the delay error voltage is reduced, the VCO frequency reduces towards that of the received sequence. When the sequences are within 1 bit of synchronisation the delay error voltage starts to rise. At this point the peak hold/comparator circuit changes state, switching over the states of SW1 and SW2. Switching SW1 causes the sequence $\overline{S_{i+1}}$ to revert to its normal noninverted state, and the discriminator characteristic changes to that shown in Fig. 3*b*. At the same time $-V_0$ is fed to the level shifter. $-V_0$ is twice the value of the peak hold voltage at change over, and this corresponds exactly to the change in mean level of the discriminator characteristics. The result is that the step offset which occurs in the original switched loop no longer occurs and there is no acceleration in search velocity after switchover.

Fig. 8 compares the experimental and theoretical acquisition trajectories of the modified switched 2Δ and 4Δ DLLs. It is clear that there is now negligible difference in performance between experimental and theoretical loops.

The modified loop requires little more hardware than the switched loop because, for automatic operation of the

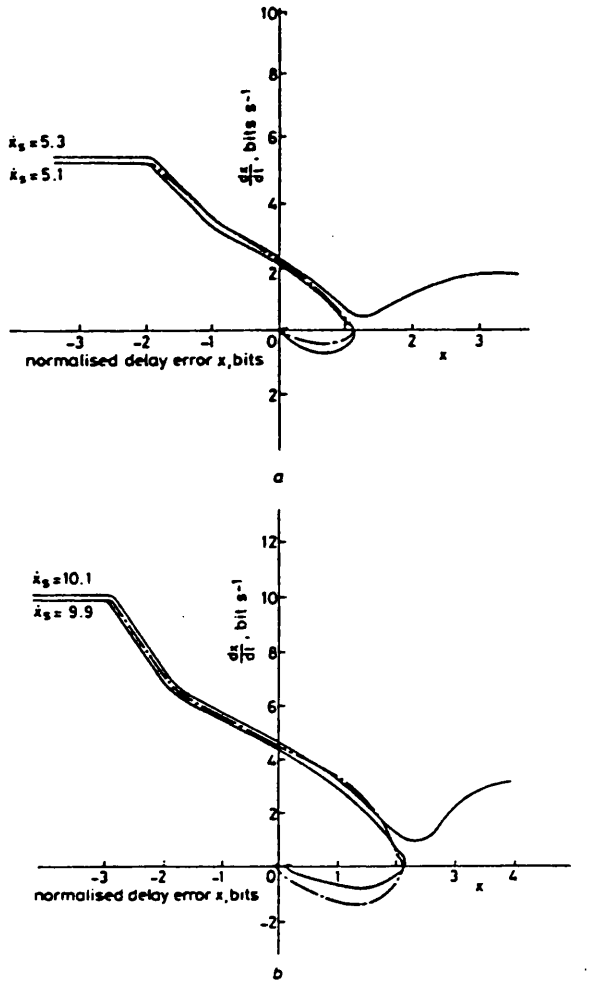

Fig. 8 *Theoretical and experimental acquisition trajectories of the modified switched delay lock loop*

——— experimental results
— — — theoretical results
ω_n = 1 rad s^{-1}
ζ = 0.707
a 2Δ variant
b 4Δ variant

loop, the peak hold/comparator circuit would be required anyway.

The modification has an associated benefit. Offsetting the VCO to cause the loop to search the sequence epochs can cause a small amount of loop stress [18] which prevents exact phase synchronisation if the loop gain is small. For systems with a high loop gain, loop stress is not a problem. If, however, very accurate phase synchronisation is required, it is necessary to remove the loop stress. The addition of the offset voltage $-V_0$ can be used to counter the built-in loop stress of the DLL.

The maximum initial search rate is dependent upon the relative phase between the sequences when S_{i+1} is inverted. Fig. 9 shows the effect of the switchover position of $\overline{S_{i+1}}$ on the maximum search rate of 2Δ and 4Δ DLLs, corresponding to the acquisition of lock. The phase reference is with respect to the in-lock condition. It is clear that the maximum search rate is achieved when the codes are

switched over at the peak negative value of the discriminator characteristics. Although not shown, this was found to be true for all the loops tested, including the asymmetric $(n-m)\Delta$ DLLs, except the switched 1Δ loop. This is because at this switchover position the discriminator characteristic has no positive slope. If the loop is switched at any other relative phase, the discriminator characteristic has a region of positive slope, and a consequent acceleration of the search process, during pull-in.

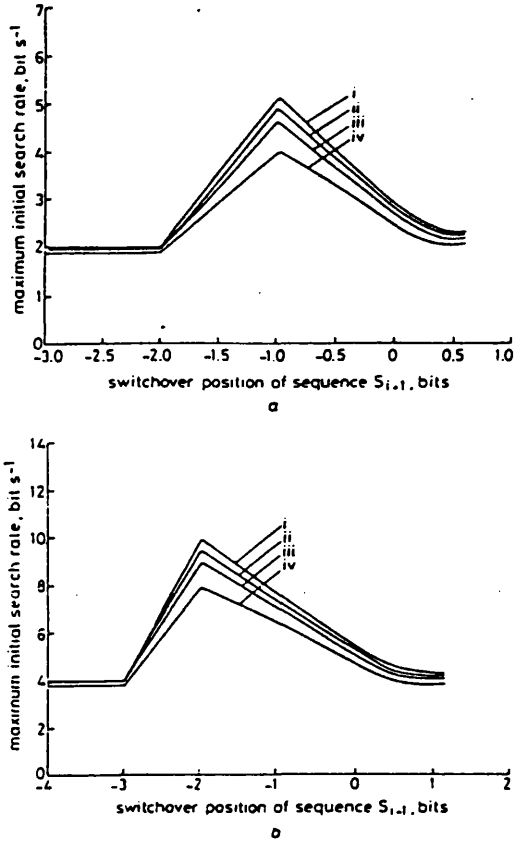

Fig. 9 *Effect of the switchover position of the sequence $\overline{S_{i-1}}$ on the maximum search rate*

a 2Δ DLL
b 4Δ DLL
Effect of loop gain
(i) = ∞
(ii) = 20
(iii) = 10
(iv) = 5
ω_n = 1 rad s^{-1}
ζ = 0.707

Also shown in Fig. 9 is the effect of loop gain G on the maximum search rate as a function of switchover position. It is apparent that reducing gain reduces the maximum initial search rate. ω_n and ζ are maintained constant at 1 rad/s and 0.707, respectively.

Similarly, increasing the damping ratio is also expected to increase the maximum initial search rate, from which lock may be ultimately achieved. Fig. 10A shows the effect of damping ratio on the maximum initial search rate of a standard DLL in 2Δ and 4Δ configurations. Theoretical and experimental results are in excellent agreement. Although increasing ζ can worsen the noise bandwidth, for damping ratios in the range 0.3–1.2 the noise bandwidth increases by 40% compared with its lowest value. However, increasing the damping ratio to 1.2 during initial acquisition can increase the maximum initial search velocity by a further 54% relative to its value for $\zeta = 0.707$ and so the trade off is beneficial. A corresponding improvement in initial search rate is found when damping ratios in excess of 0.707 are used on the modified switched loop detailed in Section 3.2, but not with the switched loop described in References 15 and 16 where increasing ζ actually worsens the performance. Fig. 10B shows the effect of damping ratio on the initial search rate of the modified switched loop found experimentally. The increase in maximum search rate, compared with a standard 2Δ DLL is now very impressive. Fig. 11 shows a further modification to the DLL where the active filter is switched so

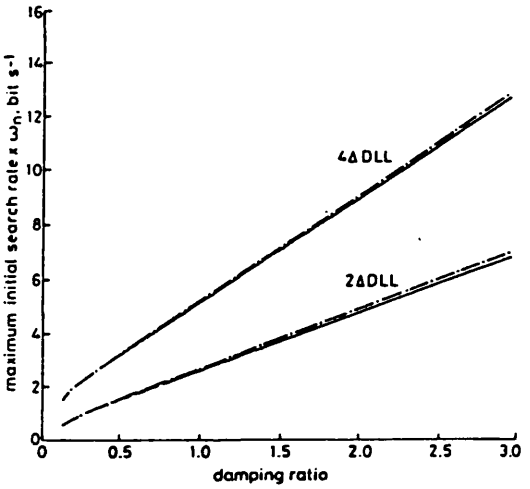

Fig. 10A *Comparison of the theoretical and experimental values of maximum initial search rate as a function of damping ratio for standard 2Δ and 4Δ DLLs*

——— theoretical predicted result (loop gain = ∞)
— — — experimental result (loop gain > 40)

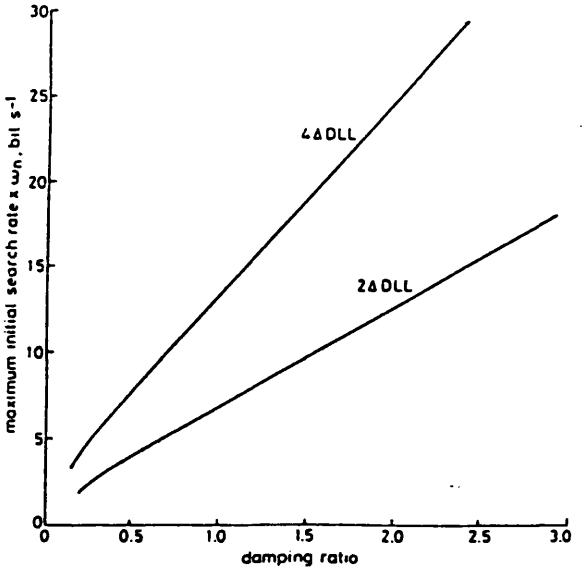

Fig. 10B *Effect of damping ratio on the maximum initial search rate of switched 2Δ and 4Δ DLLS*

These are experimental results
loop gain > 40

that the damping ratio may be changed back to 0.707 after lock without affecting ω_n. The basic loop may be switched

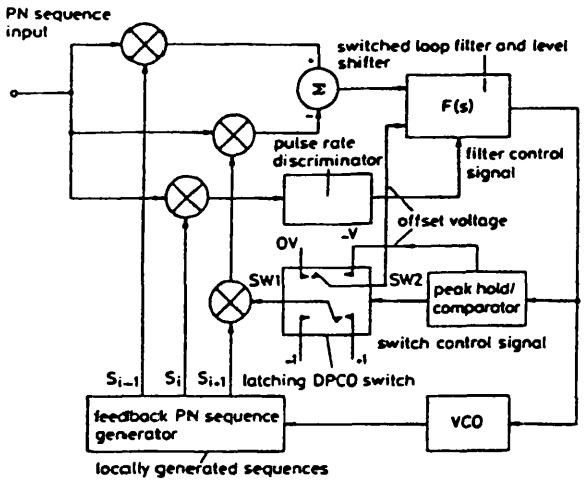

Fig. 11 *Schematic diagram of a switched 2Δ DLL in a ranging receiver using a switched active filter to control the damping ratio to achieve improved initial search velocity*

or unswitched. The pulse ratio discriminator is used as an in-lock indicator which is used to control the state of the damping ratio of the loop. An advantage of this technique, compared with changing ω_n [2], is that ζ may be changed abruptly with no tendency for the loop to lose lock. However, it must be stated that ζ must be switched over when the trajectory is in the lower quadrant of the phase plane or after final phase lock, otherwise loss of lock may result if $\dot{x}_s$ is close to $\dot{x}_{smax}$.

3.3 *Effect of the width of the discriminator characteristics on the maximum search rate of a modified switched-DLL*

It is clear that increasing the width of the discriminator characteristic increases the maximum initial search rate of both the standard and the switched DLLs. The solution to eqn. 11 was obtained for the maximum initial search rate of the general asymmetric $(n - m)\Delta$ switched DLL. It was found that the maximum search rate may be expressed as

$$\dot{x}_{max} \simeq (2.22m + 2.6n + 0.273)\omega_n \text{ bit s}^{-1} \quad (12)$$

for the case of optimum switchover position, $G \rightarrow \infty$ and $\zeta = 0.707$.

This may be contrasted with eqn. 3 for the unswitched loop. Whereas a large value of n, relative to m, reduces the maximum search rate of the standard DLL, for the case of the switched loop, widening the loop invariably increases the maximum initial search rate, because there is no positive slope to the characteristics.

A secondary, but equally important, aspect of the switched loop is that by using an initial search rate less than the maximum given by eqn. 12, but which is greater than for the standard loop, the probability of acquisition will be greater when the loop is operated in noisy conditions.

4 Effect of initial search rate on the pull-in time of standard and switched DLLs

It is a straightforward task to modify the numerical solution technique of eqn. 11 so that the pull-in time of the loop can be found. Pull-in time is defined here in the inset diagram of Fig. 12. Fig. 12 shows the effect of initial search rate on the pull-in time of switched and standard DLLs.

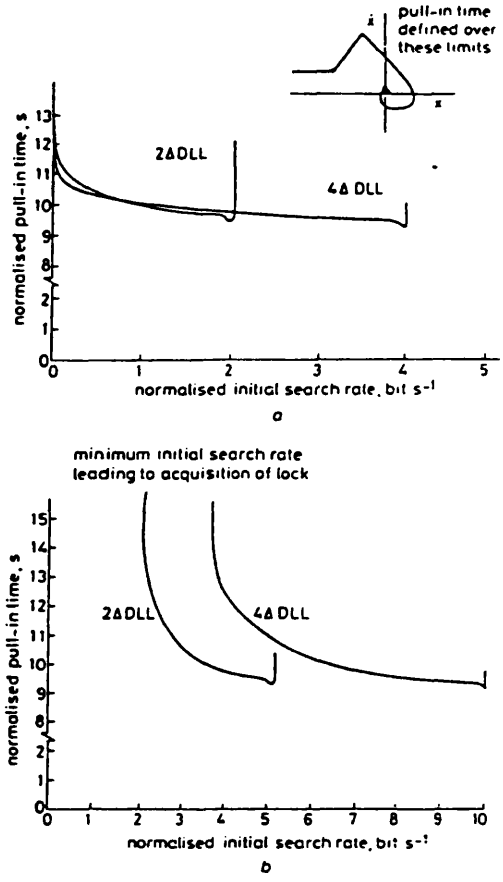

Fig. 12 *Effect of the initial search velocity on the pull-in time of 2Δ and 4Δ DLLs*

a Standard configuration
b Switched configuration
($G = \infty$, $\zeta = 0.707$)

The characteristics are similar for each type of loop, and the pull-in times are approximately the same, even for wide-Δ loops. The reason for this is that, although the initial search rate of a wide-Δ loop is large, the trajectory is correspondingly larger. The shape of the characteristics is particularly interesting. For the standard DLL, for very slow initial search rates, the pull-in time will be slow, irrespective of any loop acceleration. As the initial search rate is increased the pull-in time is reduced. However, the reduction does not follow a simple hyperbolic path because, as the initial search rate is increased, the acquisition trajectory increases in size. For normalised initial search rates above 1 bit/s the pull-in time remains relatively constant as the acquisition trajectory increases in proportion to the search velocity. For initial search velocities close to the maximum allowed, expansion of the acquisition trajectory in the upper quadrants of the phase plane ceases, giving rise to the small dip in the characteristics. However, for further, very small increases in search velocity, careful examination of the acquisition trajectories reveals that the trajectory expands significantly in the lower quadrant of the phase-plane only. This results in an increase in the pull-in time. As the initial search rate becomes extremely close to the maximum, pull-in becomes a very lengthy process.

For the case of the switched loops it is seen that there is a minimum search velocity which is necessary to ensure lock. For search rates above this minimum, the characteristics are similar to those of the standard DLL, although somewhat 'softer' in this case because the switched loop does not accelerate, which obviously slows down the pull-in time.

The reason for the minimum initial search rate is illustrated in Fig. 13 for the 2Δ loop. At low search rates the

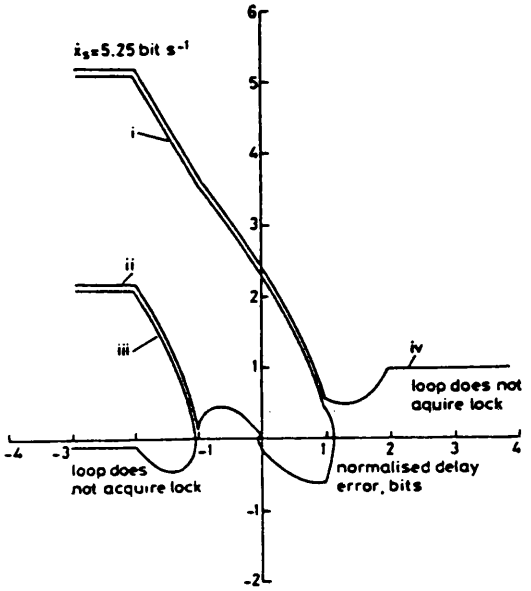

Fig. 13 *Acquisition trajectory of a modified switched loop for initial search velocities below and above the minimum allowed*

ω_n = 1 rad s^{-1}
ζ = 0.707
(i) close to maximum initial search rate
(ii) close to minimum initial search rate
(iii) just below minimum initial search rate
(iv) initial search rate just exceeds maximum allowed

trajectory is such that $\dot{x}$ reduces to 0 before x exceeds -1 bit, i.e. the epoch search stops or reverses before the codes come into coarse synchronisation. If the initial search velocity is just larger than the minimum, Fig. 13 shows that the trajectory just exceeds $x = -1$. The loop then switches over and the loop is forced to pull in.

If the initial search rate is larger than the maximum allowable, Fig. 13 shows that lock cannot be achieved.

5 Application of the switched DLL to a data modulated spread-spectrum system using data feedback

5.1 Introduction

The delay lock loops thus far described have been intended for use in ranging receiver applications. Data modulated direct-sequence spread-spectrum systems commonly use sequence inversion keying in which the data is modulo-2 added to the high-speed PN sequence. To achieve the necessary processing gain, the data rate is much less than the chip rate of the PN sequence. Generally, each data bit has the same period as one entire PN sequence period and is clocked coherently with the start of each sequence. However, the data may be transmitted asynchronously if desired. The effect of modulated data on a DLL synchroniser is to change the polarity of the N-shaped discriminator characteristic whenever the data changes polarity. The data rate is much higher than the loop filter bandwidth, and, as a consequence, the mean value of error signal fed to the VCO is zero if the data is assumed to be random. A common technique of overcoming this problem is to use an envelope detector in each arm of the DLL to maintain the polarity of the individual early and late correlations. A requirement of these detectors is that they should demodulate the data linearly (rather than square law), otherwise the loop has reduced gain at the optimum position of lock [19]. Although such techniques are viable for simple 1Δ and 2Δ DLLs they become less viable as the size of the loop increases, involving more separate correlations.

Davis and Al-Rawas [13] and Ormondroyd and Shipton [19] have separately proposed data feedback techniques in standard DLLs to remove the need for envelope detection. In this technique, an estimate of the data is obtained from the spread-spectrum data correlator. This is fed back to the data modulated PN sequence applied to the DLL synchroniser where it is modulo-2 added to produce a 'clean' PN sequence devoid of modulation. It will be apparent that the data correlator first requires the local PN sequence to be in phase with the received data modulated signal before it can supply an accurate data estimate to the synchroniser. However, the DLL idles at a slightly different frequency to that of the received sequence so that the loop can perform an epoch search when out of lock. If the epoch search is sufficiently slow, the data estimate can be obtained as the two sequences slide past each other through phase synchronisation. This can be fed to the synchroniser, and the data modulation removed. The loop then 'snaps' into synchronisation. The acquisition and in-lock performance of this loop is given in Reference 19. The penalty of this type of crude data feedback DLL is a reduction in the maximum allowable initial search rate. In general V_{max} would be much less than that given by eqn. 1. In wide-Δ loops the problem is less acute because there is a correspondingly longer time to feed the estimate back to the DLL during pull-in.

This acquisition problem exists because the data estimate can only be made when the locally generated sequence S_i comes within ± 1 bit of synchronisation of the received sequence, dictated by the correlation function of the PN sequence. If a reliable data estimate can be made before the loop starts to acquire lock, then there should be no reduction in the maximum initial search rate. Thus, for a general $(n - m)\Delta$ DLL it is necessary for a reliable data estimate to be available for $(n + m + 2)$ bits. This may be achieved quite easily with minimum extra hardware by performing multiple data correlations in parallel using several early and late local sequences generated by the feedback shift register. Fig. 14 shows the extended data correlator characteristics needed, compared with a standard correlator. It is clear that the data estimate is available to the DLL over a range of delay errors beyond that of the normal correlator. It is not necessary for this new

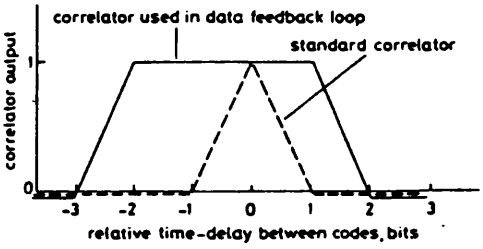

Fig. 14 *Extended data correlation characteristics necessary to employ the data feedback technique*

correlator characteristic to be symmetrical because the loop acquires lock during the search procedure and delay errors of $+2\Delta$ bit are not achieved in a 2Δ DLL when it is pulling into lock. However, it is obvious that the range over which the data can be recovered may be extended to the limit set by the length of the feedback shift register.

5.2 DLL using data feedback

The technique is shown in Fig. 15. The DLL incorporates the data correlator as well as the synchronisation loop.

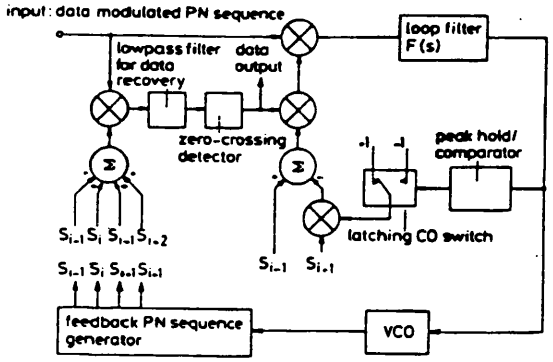

Fig. 15 *Application of the switched DLL to a data modulated pn sequence using data feedback*

The spread-spectrum data correlator is incorporated in the DLL

which may be of any type described earlier. Considering the data correlator section the lowpass filter on the data correlator has a cut-off frequency equal to half the data rate and the zero-crossing detector is used to restore the shape of the data bits.

It will be seen that the configuration of the switched 2Δ DLL is slightly different to that shown earlier, in that the S_{i-1} correlation is not performed until after the summing operation. This is permissible because the multiplication operation is linear, and its effect is to keep the number of multiplier ICs to a minimum. In this loop configuration the composite locally generated sequence, $(S_{i+1} + S_{i-1})$ is first modulated by data which is then correlated against the data-modulated received signal, using the loop filter to perform the integration process. The discriminator characteristics are identical to those shown in Fig. 3.

5.3 Experimental performance of the switched DLL with data feedback

In this set of experiments two types of data source were used. The first type of data was clocked synchronously with the PN sequence and had a data bit period equal to the sequence period. The second type of data had the same nominal data rate, but was clocked asynchronously with respect to the PN sequence. The PN code was a 1023 bit maximal length sequence clocked at 1 MHz in the transmitter. For the purpose of these tests a standard unswitched DLL is compared with the switched DLLs outlined in Sections 3.1 and 3.2. The loop natural frequency ω_n was set at 1 rad/s and the damping ratio $\zeta = 0.707$. The lowpass filter used to remove the data estimate from the data correlator was set, in the first instance, equal to the data rate (977 bit/s) to minimise pulse distortion. The data source was generated from a maximal length sequence generator.

Table 1 compares the values of maximum initial search velocity found for the types of loop listed. It will be seen that data has no effect on the maximum initial search velocity when data feedback is used, and that, in every case, the maximum initial search velocity was the same as the theoretically predicted value.

Table 1: Comparison of the normalised maximum initial search rate (rad s^{-1}) for standard and switched variants of the delay lock loop with synchronous and asynchronous data

	Standard loop	Switched loop	Modified switched loop
No data	2.0	3.6	5.1
Synchronous data	2.0	3.6	5.1
Asynchronous data	2.0	3.6	5.1

For the case of a 4Δ DLL used with data feedback, it is necessary to widen the data correlator if maximum initial search velocity is to be achieved. In this case six data correlations would be performed from sequences $S_{i-3} \rightarrow S_{i-2}$, inclusive. However, this requires no more hardware, except for extra summing junctions in the summing amplifier.

6 Conclusions

The paper has outlined details of a modified delay lock loop which has a performance which compares extremely well with theoretical calculations. The modified loop can achieve acquisition of lock from initial search rates which are 2.4 times higher than standard delay lock loops, yet has no significant effect on the pull-in time. Finally, a technique of data feedback has been applied to standard and switched DLLs, and it has been found that neither the synchronous nor asynchronous data have any effect on the pull-in properties of the loops described.

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Richard F. Ormondroyd was born near Sheffield, United Kingdom, in 1950. He received the B.Eng. and Ph.D. degrees in Electronic and Electrical Engineering from the University of Sheffield in 1971 and 1975, respectively. His Ph.D. research topic was a study of the electrical properties of amorphous chalcogenide glasses. In 1975, he was appointed as a Lecturer in the School of Electrical Engineering, University of Bath, United Kingdom, where his immediate research interests were the application of spread-spectrum techniques to communications systems. He became a Senior Lecturer at Bath University in 1985. His current research activities include spread-spectrum synchronisers, and optoelectronics.

Layth A. Al-Rawas was born in Mosul, Iraq, in 1949. He received the B.Sc. degree in Electrical Engineering from the University of Mosul, Iraq in 1969, and the M.Phil. degree in Electronic and Electrical Engineering from the City University, London, United Kingdom, in 1978. He is currently working towards the Ph.D. degree in spread spectrum systems in the School of Electrical Engineering, University of Bath, United Kingdom.